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1-Ghz CMOS Analog Signal Squaring Circuit

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1-GHZ CMOS ANALOG SIGNAL SQUARING CIRCUIT

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Engineering

By

Lizhong He

B.S., *Taiyuan University of Technology, China*, 2011

2016

WRIGHT STATE UNIVERSITY

WRIGHT STATE UNIVERSITY

GRADUATE SCHOOL

<u>Aug 4, 2016</u>

I HEREBY RECOMMEND THAT THE THESIS PREPAREDUNDER MY SUPERVISION BY <u>Lizhong He</u> ENTITLED "<u>1-GHZ CMOS ANALOG SIGNAL SQUARING CIRCUIT</u>" BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE Of Master of Science in Electrical Engineering

_____
Chien-In Henry Chen, Ph.D.
Thesis Director

_____
Brian Rigling, Ph.D.
Department Chair

Committee on Final Examination
_____
Chien-In Henry Chen, Ph.D.

_____
Yan Zhuang, Ph.D.

_____
Jiafeng Xie, Ph.D.

_____
Robert E.W.Fyffe,Ph.D.
Vice President for Research and
Dean of the Graduate Schoo

Abstract

He,Lizhong.M.S.Egr, Department of Electrical Engineering, Wright State University, 2016."1-Ghz CMOS Analog Signal Squaring Circuit"

In analog signal processing the squaring circuit represents the core for implementing an analog signal having a value representing the square of the input signal. For example, calculating the square of input signal is necessary in adaptive processing of an input signal based on its instantaneous root mean square value. In this thesis, a new 1-Ghz analog signal squaring circuit (squarer) designed in 180 nanometer CMOS process is presented. It is implemented by CMOS components including current source, current mirror, differential amplifier, low-pass filter, and voltage output buffer. A gain control amplifier and a 10-bit ADC are set up to evaluate the dynamic performance of the CMOS signal squarer. The measured results show a wide sweep capability of analog signal frequency up to 1 GHz with good linearity and spurious-free dynamic range.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Acknowledgement

At first, I want to deeply thank to my thesis advisor Dr. Henry Chen, he helps me a lot, not only in the research, but also in many parts of my life. Without his help I can't finish my research. Secondly, I want to thank professors in Electrical Engineering Department, I learned a lot in their classes. Thirdly, I want to thank staffs of the Electrical Engineering Department for their direct and indirect assistance in my research. Finally, I deeply thanks to Drs. Jiafeng Xie and Yan Zhuang for their time to be my thesis committee members.

1   INTRODUCTION

1.1 Background

With the increased requirements for the performance of signal preprocessor, such as stability, amplitude, frequency range and others, signal preprocessor becomes more important than it was before. The performance of signal preprocessor directly impacts the result of the following signal analysis and process, such as the working time and results of ADC or DAC[1]. Signal preprocessor can be divided into different types, including the charge / voltage converter, current / voltage converter, frequency / voltage converter, impedance converter, frequency converter, and others. This complementary metal-oxide-semiconductor (CMOS) signal squarer is an application circuit in signal preprocessor.

Complementary referred to the typical CMOS design approach is to use complementary symmetry of p-type and n-type metal oxide semiconductor field effect transistor (MOSFET) component circuits. In circuit design, CMOS circuit technology is usually used for static RAM, microcontrollers, microprocessors, and other digital logic circuit.[2] In some situations, this technology is used in CMOS analog circuits design, such as a data processor, a picture sensor and highly integrated transceivers for communication.

The CMOS devices has two important characteristics, one is high noise and another one is low static power consumption. CMOS devices only produce power when transistor is turned on. Therefore, CMOS devices don't engender excess heat generated by other forms of CMOS devices. High-density logic functions can be allowed on a chip for CMOS, so CMOS circuit becomes the most commonly used design technique in IC chips.[3] CMOS device power

consumption is a major concern in chip design.[4] In CMOS circuits, power consumption is divided to two parts:

1. Static power dissipation

Gate-source threshold voltage is a property for NMOS and PMOS transistors. When the threshold voltage is bigger than V_{GS}, the threshold current of transistor is considered small. The main constitute material of CMOS transistors is silicon dioxide, which is a good insulator. The electrons can pass through the insulation layer to cause a tunnel current, which becomes important especially for 130 nanometer or thinner gate oxide transistors. In modern circuit, the leakage circuit is very small in comparison with the threshold current and the tunnel current.[5]

2. Dynamic power dissipation

Dynamic power dissipation is divided into two types: 1) charging/discharging power, and 2) short-circuit power.

(1) Charging/discharging power

In a complete cycle of CMOS logic gate, CMOS circuit power consumption occurs at various load control switch when the capacitor is charged or discharged.

(2) Short-circuit power

There is a transition period where both PMOS and NMOS transistors are turned on, which induces a short-circuit power. The short-circuit power is dependent on the input signal rise and fall times, the transistor size and the load capacitance.[6]

1.2 Research Motivation

In the electronic apparatus, frequency squarer is typically used in communication and signal processing circuits. Frequency squarer produces an analog signal having a value representing the square of the input signal. It's a nonlinear circuit and the input

signal is modulated to produce harmonics. A band-pass filter is designed to filter out the harmonics as well as unwanted harmonics from the output.

Most signal squaring circuit can't work properly at high frequency in Ghz. Two signal squaring circuit techniques, "A 5Mb/s UWB-IR transceiver front-end for wireless sensor networks in 0.13 mm CMOS" [6] and "A Low-Power and Flexible Energy Detection IR-UWB Receiver for RFID and Wireless Sensor Networks" [7] can work in GHz, however SFDR is in general not high enough. In this paper, a new analog signal squaring circuit is proposed and designated to work for analog input signal frequency in 1-Ghz range while keep SFDR of the squared signal output high. For low frequency input signal it can be 50 db and for high frequency input signal it can be 40 db.

1.3 Thesis Organization:

My thesis organization is depicted in Fig. 1.1.

```
┌─────────────────────────────┐
│  CMOS Current Sink Source and │
│  Current Mirror analog Signal │
│  Frequency Square Generator   │
└─────────────────────────────┘
              │
              ▼
      ┌──────────────┐
      │ Introduction │
      └──────────────┘
              │
              ▼
      ┌──────────────────┐
      │ Introduction of each │
      │ Element of Circuit  │
      │     Design          │
      └──────────────────┘
              │
   ┌──────┬──────┬──────┬──────┬──────┐
   ▼      ▼      ▼      ▼      ▼
┌────────┐┌────────┐┌────────┐┌────────┐┌────────┐
│Current ││Current ││Differen││Low Pass││Output  │
│Source  ││Mirror  ││tial    ││Filter  ││Buffer  │
│        ││        ││Amplfier││        ││        │
└────────┘└────────┘└────────┘└────────┘└────────┘
                        │
                        ▼
              ┌──────────────────┐
              │ High Frequency analog │
              │ Frequency Square Generator │
              └──────────────────┘
                        │
              ┌─────────┴─────────┐
              ▼                   ▼
        ┌──────────┐        ┌──────────┐
        │Circuit   │        │Simulation│
        │work      │        │Results   │
        └──────────┘        └──────────┘
              │                   │
              └─────────┬─────────┘
                        ▼
                 ┌──────────┐
                 │Compare the│
                 │results    │
                 └──────────┘
                        │
                        ▼
                 ┌──────────┐
                 │Conclusion and│
                 │Future Work   │
                 └──────────┘
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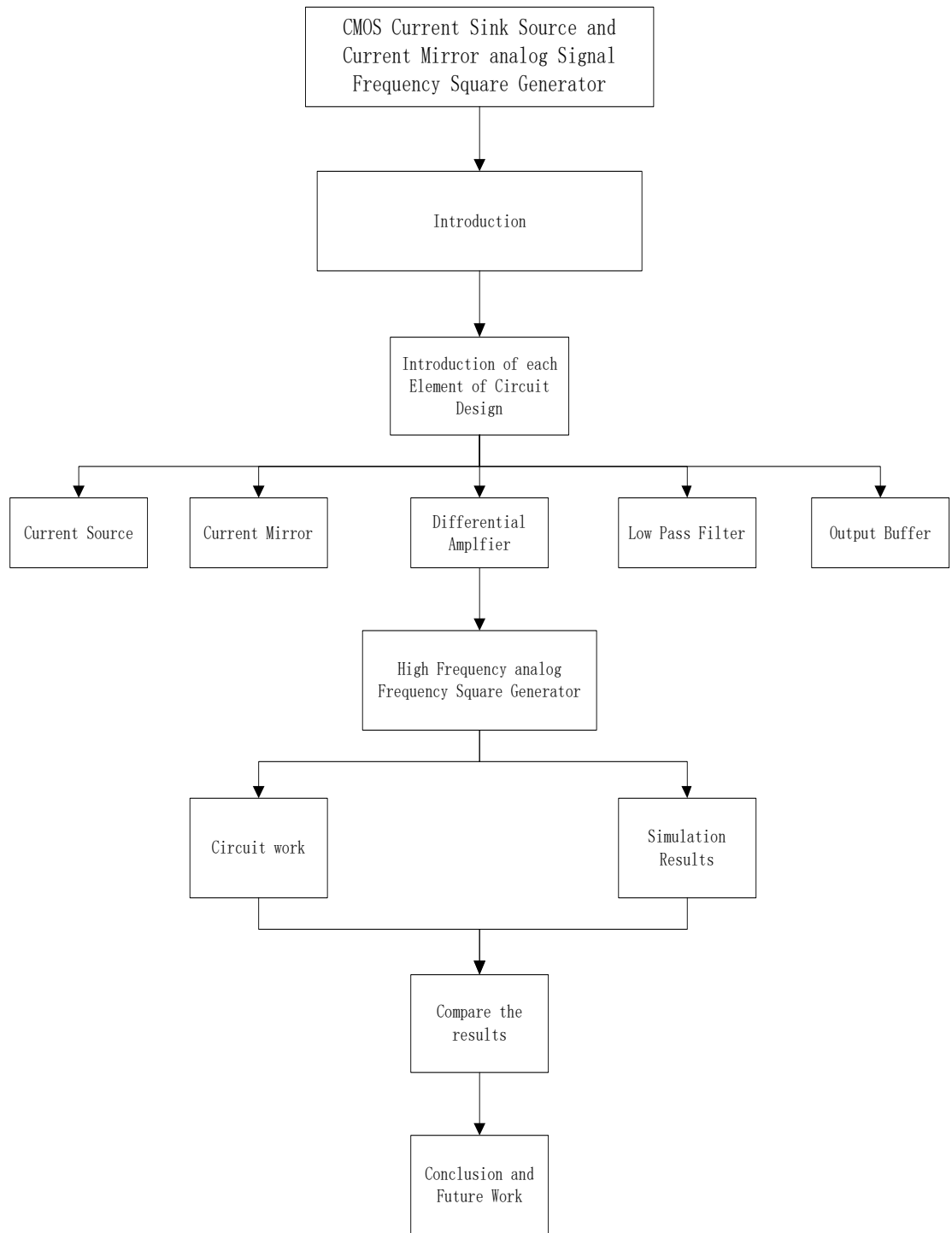
Figure 1.1 Thesis organization

2   CMOS Signal Squaring Circuit

2.1 Current Source Principle

Current source is an electronic circuit providing current independent of voltage. Ideal current source can be formulated by mathematical model. Independent current source is defined as if the current source can independently designate current without considering any other variables in the circuit.[8] Conversely, controlled current source is defined as if a current source is depended on values of other voltage or current in the circuit. The resistance of an ideal current source is infinity.[9] The circuit can determine the voltage for current source completely. If a short circuit connect to current source, the current source's voltage is zero and thus it delivers zero power. When a load resistor is connected to current source, if the load resistor approaches infinity, the voltage across the circuit close to infinity (open circuit). Therefore, in reality an ideal current source can provide unlimited energy. Ideal physical current source does not exist. A real current source is defined by two characteristics: 1) its internal resistance and 2) its compliance voltage. [10] Compliance voltage current source can be provided to the maximum load voltage.

At a given load current range, some types of the actual current sources exhibit virtually unlimited internal resistance . However, when these current sources reached the compliance voltage, it will suddenly stop as a current source state.

Current source resistance is much bigger than load impedance, so change the load impedance will not change the current source circuit. Series resistance is meaningless in the current source circuit, because it does not change the current source load, and it will not change the voltage across the load. Current source has

three characteristics: 1) constant current output, 2) infinite DC resistance and 3) infinity AC resistance.[11]

2.1.1 Current source

In the CMOS circuit design, a MOS diode resistor is often used in designing a current source. The schematic is shown in Fig. 2.1 in which the MOS diode operates in saturation.
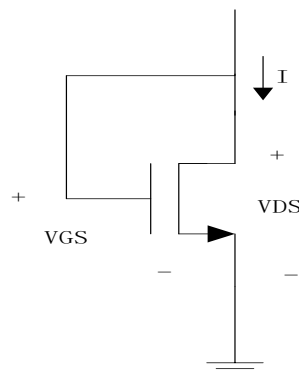

Figure 2.1 Current source

The current through the current source is:

$$i_d = \frac{K}{2}\left(\frac{W}{L}\right)(v_{GS} - V_T)^2(1 + \lambda v_{DS})$$

The relationship between the current I_d and the voltage V_{DS} and V_{GS} is shown Fig. 2.2:
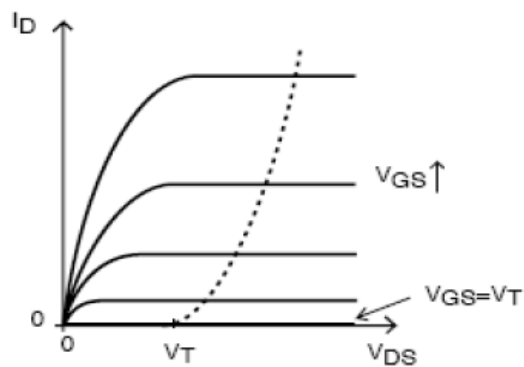

Figure 2.2 I_d vs. V_{DS} and V_{GS}[12]

2.1.2   Current sink source

Current sink source design principle is similar to the current source except replacing the NMOS transistors with PMOS transistor and the PMOS operates in saturation.

2.2 Current Mirror

A current mirror is defined as a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading.[13] Conceptually, an ideal current mirror is an ideal inverting current amplifier. Current mirror has three main parameters. 1) the transfer rate (transfer radio), also called the current amplification factor, 2) the AC output resistance, determined by the output current and voltage, and 3) the lowest working voltage, i.e., the minimum voltage to make the current mirror work.[14]

2.2.1   NMOS Current Mirror
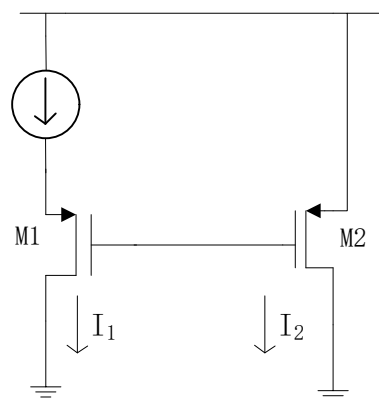
A NMOS current mirror is shown in Fig. 2.3：

Figure 2.3 NMOS Current mirror

In NMOS current mirror, the current I_2 can be calculated as follows:

$$I_2 = I_1 * \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}}$$

where I_1 is the current

source

, W_2 and L_2 is the width and length of the transistor M2, and W_1 and L_1 is the length and width of the transistor M1.   By controlling W_2/W_1 , a desirable I_2 is obtained

when $L_1 = L_2$.

2.2.2   PMOS Current Mirror

A PMOS current mirror is shown in Fig. 2.4:
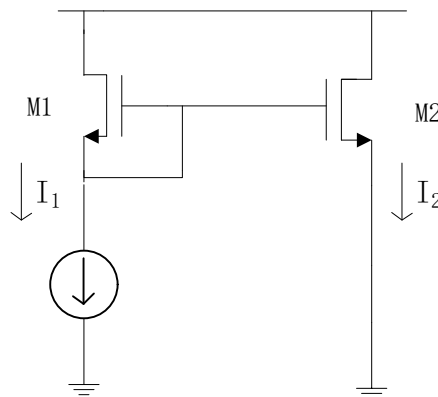
Figure 2.4 PMOS current mirror

PMOS current mirror principle is basically same with the NMOS current mirror, except that the current source in the bottom portion, and for current magnitude PMOS current mirror through the PMOS transistor transformation instead of NMOS transistors. In the circuit design, designers need to choose NMOS current mirror or PMOS current mirror based on different situations.

2.3 Differential Amplifier

The differential amplifier is commonly used in many CMOS circuit designs. It

amplifies the difference of two input voltage v_1 and v_2 when operating in the differential mode signal state[15] or zoom in two input voltage average value when operating in the common mode signal state[16].   The differential amplifier is shown in Fig. 2.5.   It has two operations:
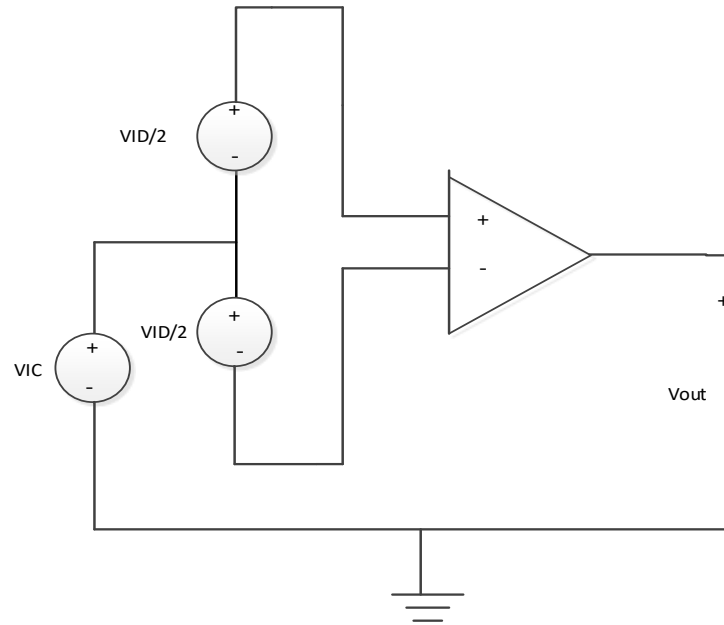
Figure 2.5 Differential Amp

(1) Common signal mode

When the differential amplifier operates in common mode, its input voltage v_{IC} v_{IC} equals to the average of v_1 and v_2 as shown in Fig. 2.5.

In this case the two input signals are amplified.

(2) Differential signal mode

For differential signal mode, the input signal equal to the difference of v_1 and v_2. v_{ID} represents the input signal as shown in Fig. 2.5.   In this case, differential amp amplified the difference between two input signals.

The performance of the differential amplifier is evaluated by two important parameters[17]:

(1) Common mode rejection ratio (CMRR)

The common mode rejection ratio is defined as how well: 1) the differential amplifier rejects the common mode input voltage and 2) the differential amplifier amplifies the differential-input voltage. It is calculated as $CMRR = \frac{A_{VD}}{A_{VC}}$ where A_{VD} is the differential signal gain and the A_{VC} is the common mode signal gain.

A higher value of CMRR will lead to a better performance of differential amplifier.

(2) Input common mode range (ICMR)

Input common mode range is defined as the scope of common-mode voltages in which the differential amp can touch and enlarge the input signal difference with the same gain. Usually, ICMR is a range for all MOS transistors operate in saturation.[18]

2.4 Low-Pass Filter

Low-pass filter is a filter that passes input signal whose frequency is below the cut-off frequency and attenuates input signal whose frequency is above the cut-off frequency.

2.4.1   RC Low-Pass Filter

A simple low-pass filter is RC filter, which connects a resistor in serial with an output capacitor. The output capacitor exhibits reactance and blocks high-frequency signals as it functions like a short circuit. The interrupt frequency, also called the turn over frequency or cut off frequency, is formulated as follows:

$$f_c = \frac{1}{2\pi\tau} = \frac{1}{2\pi RC}$$

where R and C are resistance and capacitance values. The cut off frequency is a reciprocal of the time constant τ.

$$w_c = \frac{1}{\tau} = \frac{1}{RC}$$

Low pass filter behavior can be interpreted as the time for capacitor charge or discharge through the resistor. At low frequencies, it has enough charging time to charge the capacitor before the input signal switches its polarity; the output voltage is same as the input voltage. At high frequencies, it only has little time to charge the capacitor before the input signal switches its polarity; the output voltage is small enough to be neglected. [19]

2.4.2   RLC Low Pass Filter

A RLC low-pass filter is comprised of resistor, inductor and capacitor connected in series or parallel connection. The main difference between the RLC low-pass filter and RC low-pass filter is that RLC low pass filter has minimum impedance when it's at the resonance frequency, but the RC low pass filter has smaller impedance with higher frequency.

2.5 Output Buffer Circuit

An output buffer provides impedance transformation, which is mainly classified to two designs: 1) voltage output buffer and 2) current output buffer. [20]

2.5.1   Voltage Output Buffer

An ideal voltage output buffer has infinity input resistance and zero output resistance. However, a real voltage output buffer has high input impedance and low

output impedance.　A good linearity and fast output response is critical to the voltage output buffer performance[21].　If the voltage amplification factor is unity, the voltage output buffer is called the unity gain amplifier buffer and its output tracks the input voltage. [22]

2.5.2　Current Output Buffer

An ideal current output buffer has zero input resistance and infinity output resistance. However, a real current output buffer has low input impedance and high output impedance.[23]　A good linearity and fast output response is critical to the current output buffer performance. If the current amplification factor is unity, the current output buffer is called the unity gain current amplifier buffer and its output tracks the input current.[24]

3   1-Ghz CMOS Signal Frequency Squarer

3.1 Introduction:

The proposed 1-Ghz CMOS signal frequency squarer is designed by a current source, a PMOS current mirror, a differential amplifier, a low-pass filter, and a voltage output buffer. A gain control amplifier and a 10-bit ADC are used to evaluate the dynamic performance of signal frequency.
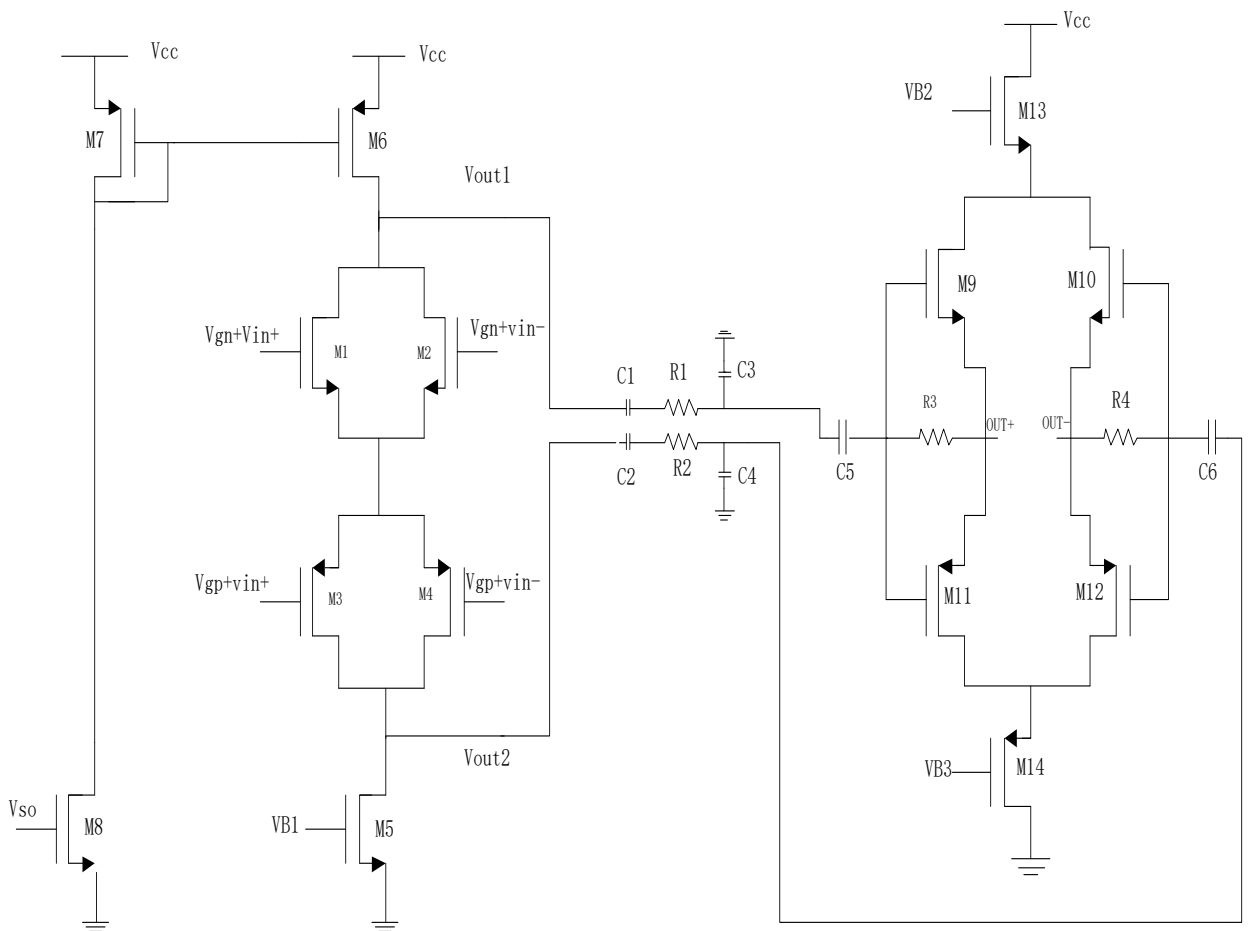

Figure 3.1 CMOS Frequency Squarer

The part of differential Amp (Fig. 3.2) is used to square the input signal frequency. We can get the small signal model for this part like Fig. 3.3.
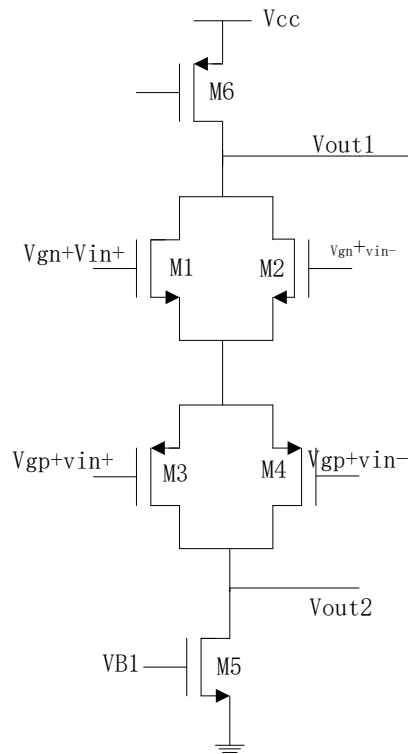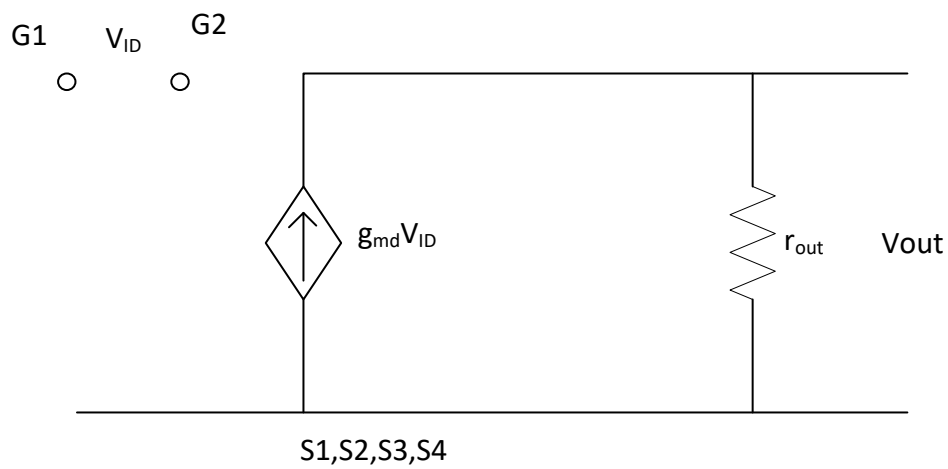
Figure 3.2 Differential Amp

Figure 3.3 Differential Amp small signal model

In the small signal model, the $V_{ID}=V_{GN}+(v_{in+}+v_{in-})/2$ and r_{out} is the equivalent output resistance. Then, from Figure 3.1.2 the following current equations are derived.

$$I_{D1} = 0.5k_n(V_{GN} + v_{in+} - Vs - V_{THN})^2 + I6$$

$$I_{D2} = 0.5k_n(V_{GN} + v_{in-} - Vs - V_{THN})^2 + I6$$

$$I_{D3} = 0.5k_p(V_{GN} + v_{in+} - Vs - |V_{THp}|)^2 + I6$$

$$I_{D4} = 0.5k_p(V_{Gp} + v_{in-} - Vs - |V_{THp}|)^2 + I6$$

$$I_{D1} + I_{D2} = I_{D3} + I_{D4} = I_{D5}$$

$$k_n = u_n c_{ox}\left(\frac{W}{l}\right) k_p = u_p c_{ox}\left(\frac{W}{l}\right)$$

So, Vout1=Vcc - $(I_{D1} + I_{D2})$*Zn

$$= [Vcc - k_n(V_{GN} - Vs - V_{THN})^2 * Zn - kn * v_{in+}^2 * Zn - 2I_6 * Zn]$$

Vout2 = $(I_{D3} + I_{D4}) * Zp$

$$= k_p(V_{GP} - Vs - V_{THN})^2 * Zp + kp * v_{in+}^2 * Z_p + 2I_6 * Zn$$

In Fig. 3.4 the output Vout2 includes input AC signal square, without using the proposed current sink source and current mirror. From the output waveform, the dynamic range of Vout2 is about 7 mV, which is too weak for the 10-b ADC and next stage use. So, in order to increase the dynamic range of Vout2, a current sink source and a current mirror are designed and used before the differential amp. Form Fig. 3.5 the dynamic range of Vout2 is increased to the 839 mV, which is about 120 times of the original dynamic range of 7 mV.
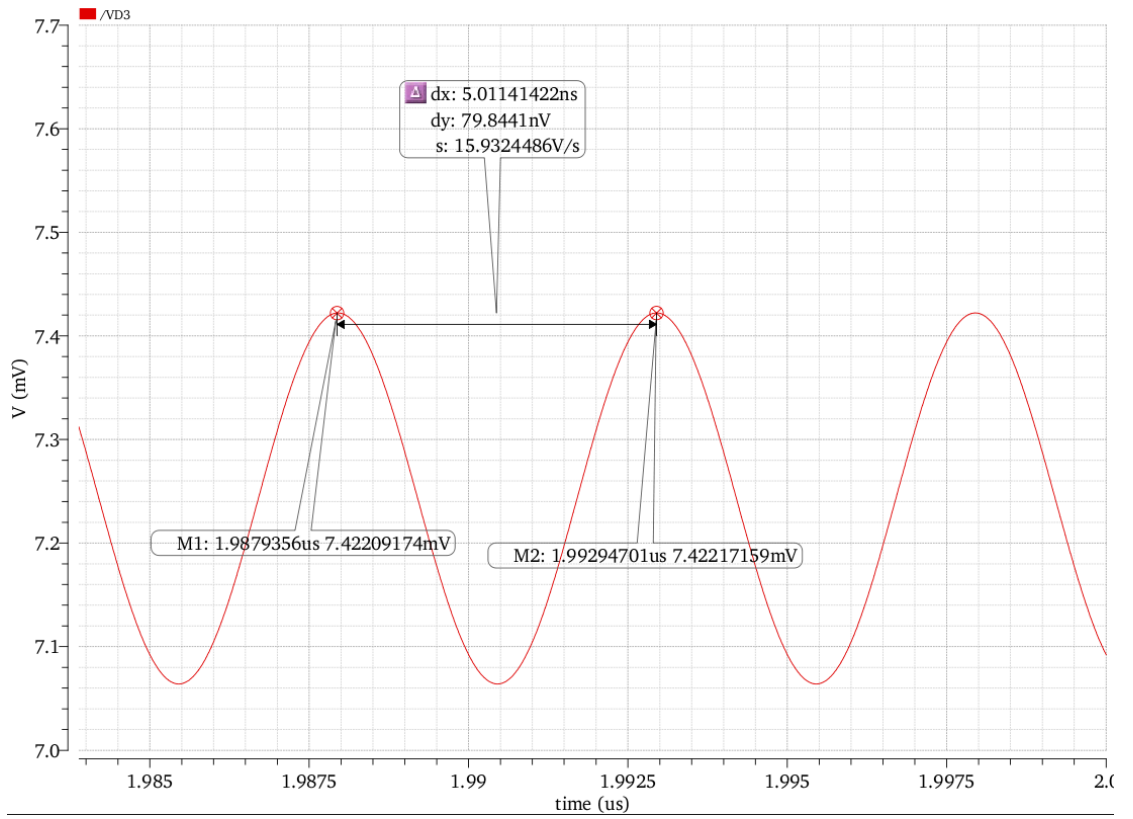
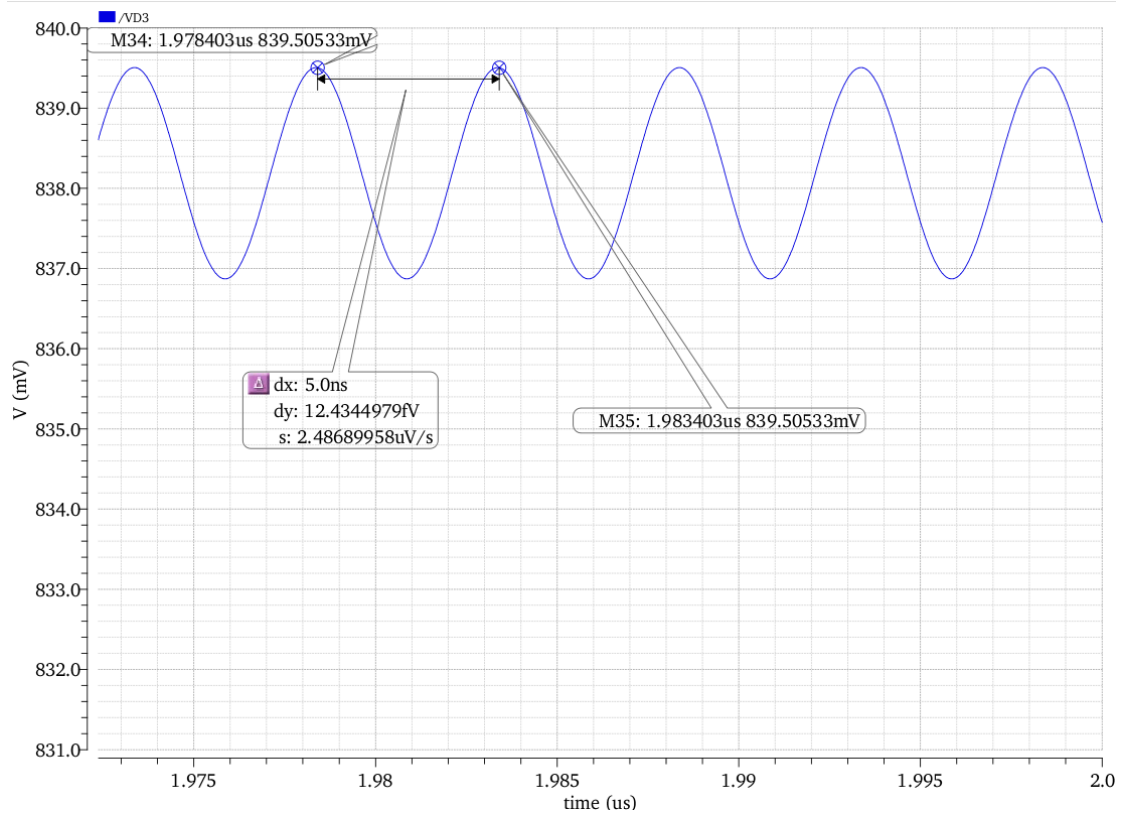Figure 3.4 The Vout2 before using the proposed current sink source and current mirror

Figure 3.5 The Vout2 after using the proposed current sink source and current mirror

The transistor sizes of the differential amp are given in Table 3.1.

Table 3.1 The transistor sizes of the differential amp

M1	30u/180n
M2	30u/180n
M3	10u/180n
M4	10u/180n

Table 3.2 The transistor sizes of the current source and current mirror

M6	15u/180n
M7	10u/180n
M8	10u/180n

Table 3.3 The capacitance values

C1	1pf
C2	1pf
C3	1pf
C4	1pf

Table 3.4 The resistance values

R1	100Ω
R2	100Ω

In order to evaluate dynamic performance of the signal squarer, a test bed is set up in Fig. 3.6. The square output of the frequency squarer is fed to a gain control amp, which adjust the square output dynamic range and the DC offset voltage to meet the 10-bit ADC specifications.
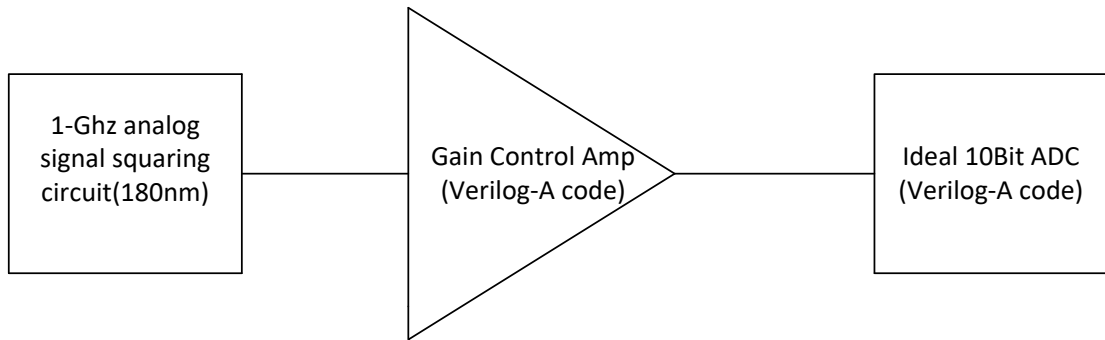
Figure 3.6 Test bed to evaluate the signal squarer

3.2 ADC Design

A 10-b ADC is created in Verilog-A code. The code is blow:

```
// Verilog A for reseach_va, adc10bits, Verilog-a

`include "constants.vams"

`include "disciplines.vams"

module adc10bits(vd9, vd8, vd7, vd6, vd5, vd4, vd3, vd2, vd1, vd0, vdec, vin, vclk);

electrical vd9, vd8, vd7, vd6, vd5, vd4, vd3, vd2, vd1, vd0, vdec, vin, vclk;

parameter real trise = 0 from [0:inf);

parameter real tfall = 0 from [0:inf);

parameter real tdel = 0 from [0:inf);

parameter real vlogic_high = 5;

parameter real vlogic_low    = 0;

parameter real vtrans_clk        = 2.5;

parameter real vref            = 1.0;

`define NUM_ADC_BITS 10

    real unconverted;

    real halfref;

    real decb;

    real vd[0:`NUM_ADC_BITS-1];

    real co[0:`NUM_ADC_BITS-1];
```

```verilog
    integer i;

    analog begin

        @ ( initial_step ) begin

halfref = vref / 2;

        end

        @ (cross(V(vclk) - vtrans_clk, 1)) begin

            unconverted = V(vin);

            for (i = (`NUM_ADC_BITS-1); i>= 0 ;i = i - 1) begin

vd[i] = 0;

                co[i] = 0;

                if (unconverted >halfref) begin

vd[i] = vlogic_high;

                    co[i] = 1;

                    unconverted = unconverted - halfref;

            end else begin

vd[i] = vlogic_low;

                    co[i] = 0;

            end

                unconverted = unconverted * 2;

            end

        end

    decb                                                                    =
512*co[9]+256*co[8]+128*co[7]+64*co[6]+32*co[5]+16*co[4]+8*co[3]+4*co[2]+2*co[1]+co[0];

        //

        // assign the outputs

        //

        V(vd9) <+ transition( vd[9], tdel, trise, tfall );
```

```
        V(vd8) <+ transition( vd[8], tdel, trise, tfall );

        V(vd7) <+ transition( vd[7], tdel, trise, tfall );

        V(vd6) <+ transition( vd[6], tdel, trise, tfall );

        V(vd5) <+ transition( vd[5], tdel, trise, tfall );

        V(vd4) <+ transition( vd[4], tdel, trise, tfall );

        V(vd3) <+ transition( vd[3], tdel, trise, tfall );

        V(vd2) <+ transition( vd[2], tdel, trise, tfall );

        V(vd1) <+ transition( vd[1], tdel, trise, tfall );

        V(vd0) <+ transition( vd[0], tdel, trise, tfall );

        V(vdec) <+ decb/1023;

`undef NUM_ADC_BITS

    end

endmodule
```

3.3 Gain Control Amplifier

A gain control amp is created in Verilog-A code. The code is blow:

```
`include "constants.vams"

`include "disciplines.vams"

module amp(sigin, sigout);

input sigin;

output sigout;

electrical sigin, sigout;

//parameter real gain = 0.5/(vin_high - vin_offset);

real vin_high,vin_offset;

real gain;

analog begin

    // peak input voltage so far
```

```
        vin_high=max(V(sigin),vin_high);

        // average mid-point so far (in effect)

        vin_offset=idt(V(sigin),0)/$realtime;

        // max is to ensure that you don't end up with divide by zero

        // and massive gain at start of simulation (adjust 0.1 to a reasonable

        // value)

        gain=0.5/max(vin_high-vin_offset,0.1);

        V(sigout) <+ gain*V(sigin) + 0.5*gain - gain*vin_offset;

    end

    endmodule
```

In order to test my circuit output, I use a 10 bit ideal ADC to test the circuit, but for the ideal ADC, the input signal range should be 0 to 1V, the offset DC voltage should be 0.5V, and the amplitude should be 0.5V. In case of 100Mhz analog input signal, the Fig. 3.7 is the square output wave form before the gain control, the DC offset voltage is 1.1995V, and the dynamic range is 14.25mv. It's far away for the ideal ADC dynamic range. The Fig.3.8 is the square output wave form after the gain control amplifier for 100Mhz analog input signal, the dc offset voltage from 1.1995V move to the 0.5V, and the dynamic range is increased from 14.25mv to 1V, so it's ready for 10bit ADC to do the FFT analysis.
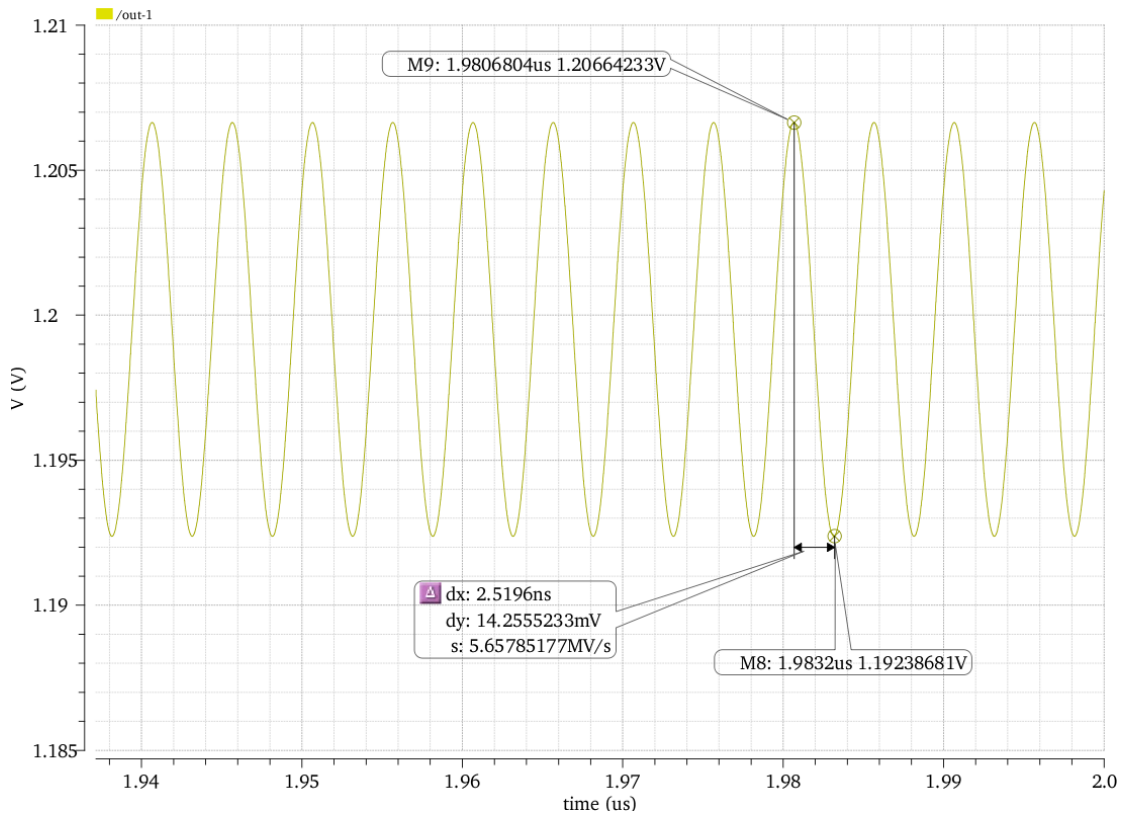
Figure 3.7 The square output waveform before the gain control amplifier for 100Mhz analog
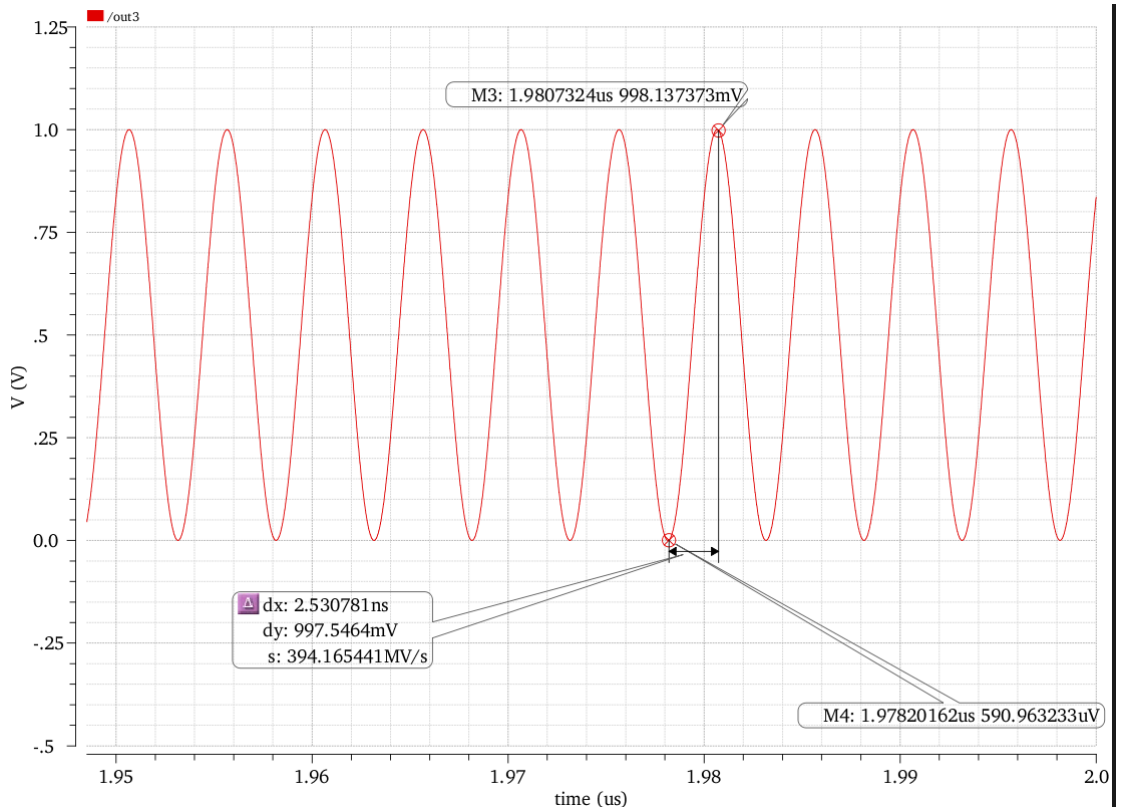
input signal

Figure 3.8 The square output waveform after the gain control amplifier for 100Mhz analog

input signal

Based on the different input signal frequency, the gain control amplifier is used to make the square output's offset voltage is 0.5V, and the dynamic range is 1V. The amplification coefficient is different for different input frequency. The summary of amplification coefficient based on the simulation results is shown in table 3.5.

Table 3.5 Amplification coefficient of the gain control amp

Input Frequency (Mhz)	Gain coefficient
100	70
200	116
300	177
400	250
500	339
600	447
700	565
800	695
900	848
1000	925

3.4 Experimental Results

3.4.1   100-Mhz input analog signal simulation results

Applying 100 Mhz input signal, the differential amplifier input and the square output waveforms are shown in Fig. 3.9 where the yellow, green, light blue and blue waveforms are the four input signals $V_{GN}+v_{in+}$, $V_{GN}+v_{in-}$, $V_{GP}+v_{in+}$, $V_{GP}+v_{in}$; the purple waveform is the square output waveform. The square signal waveform (200Mhz) shown in Fig. 3.10 is after the square signal output after the low-pass filter, the voltage buffer amplifier and the gain control amplifier.
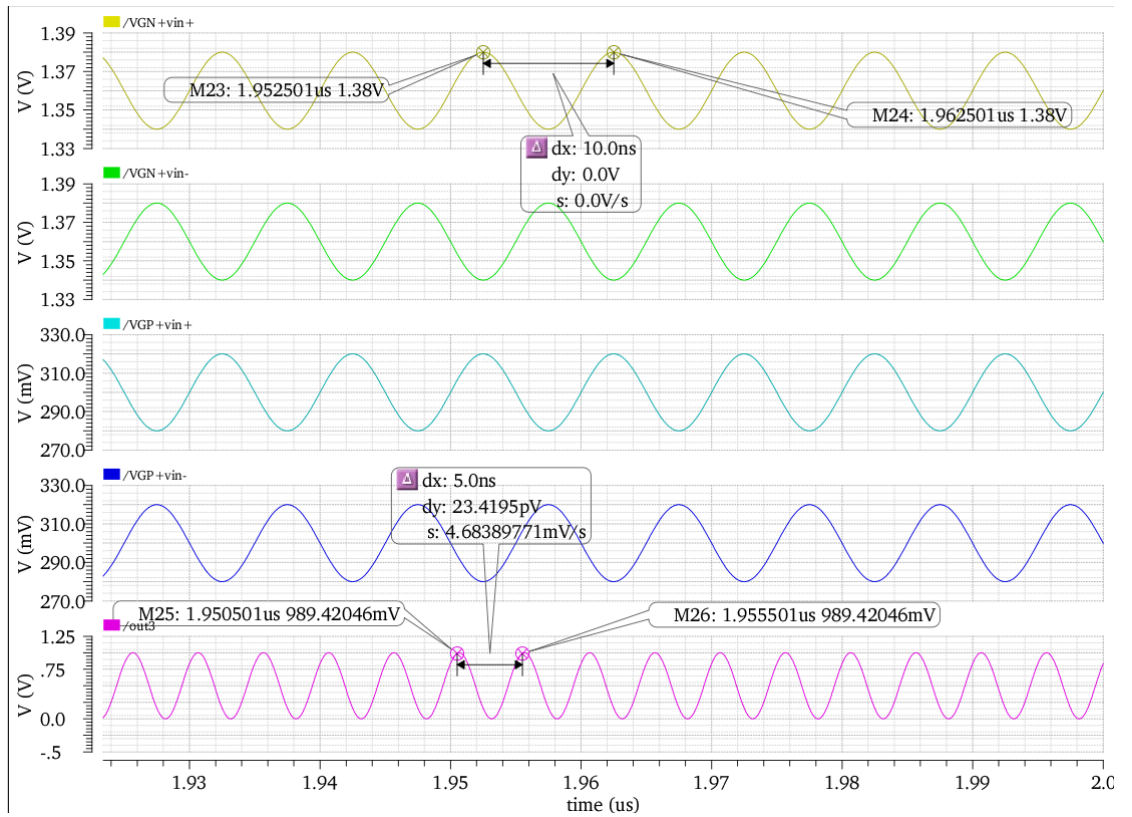
Figure 3.9 The differential amplifier four input signals $V_{GN}+v_{in+}$, $V_{GN}+v_{in-}$, $V_{GP}+v_{in+}$, $V_{GP}+v_{in}$

and the square output waveform for 100Mhz analog input signal
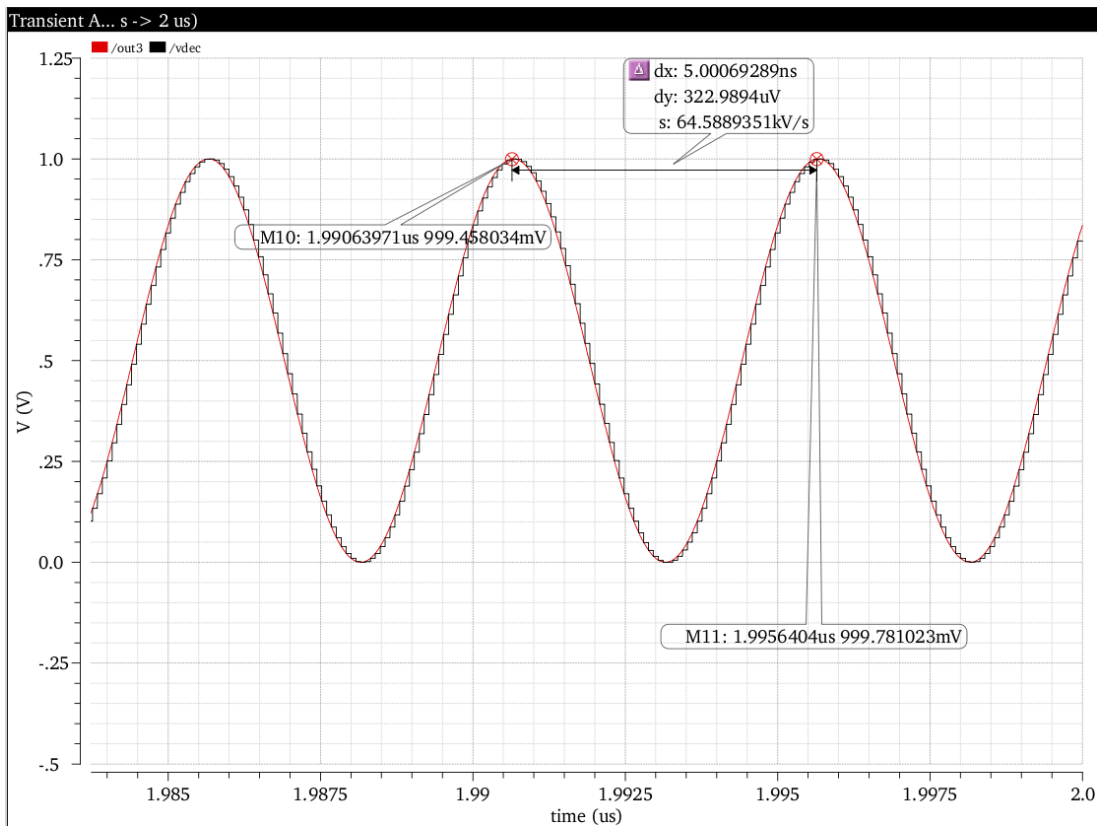

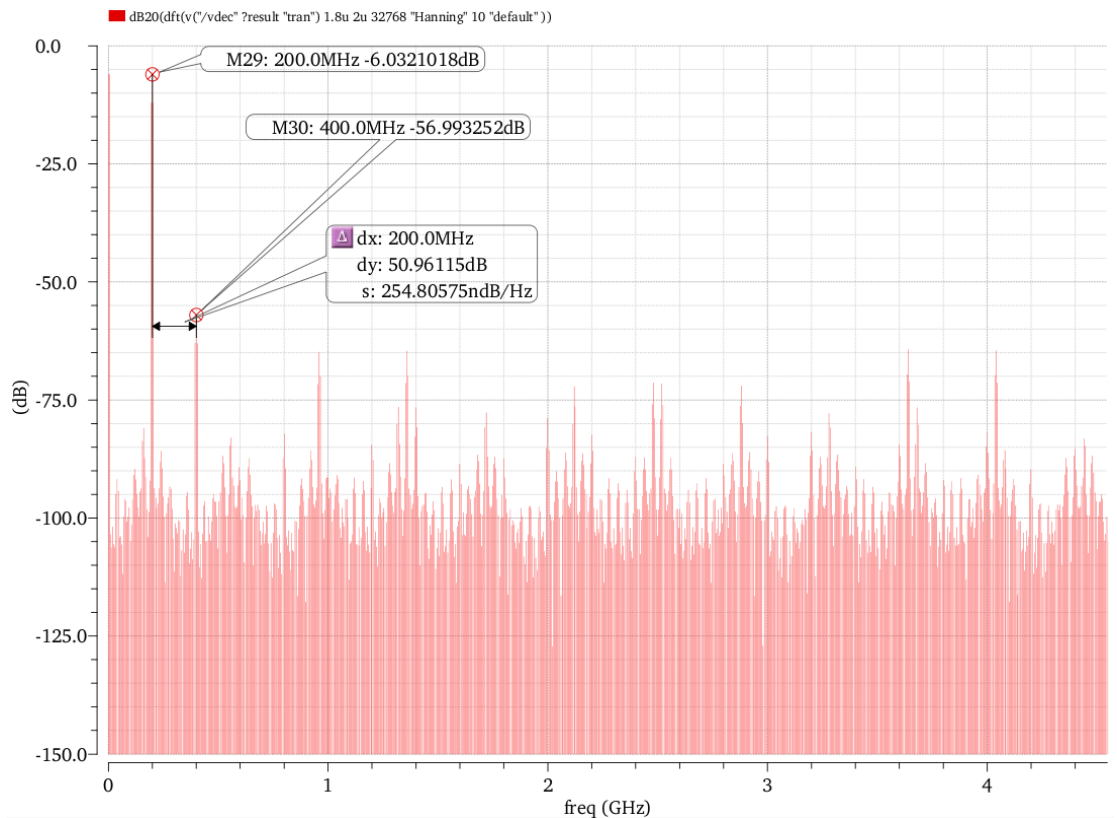Figure 3.10 The test bed output square signal waveform (200Mhz)

Figure 3.11 FFT spectrum of the test bed output square signal waveform (200Mhz) after the

10-b ADC

The FFT spectrum of the test bed output square signal waveform (200Mhz) after the 10-b ADC is shown in Fig. 3.11.   The SFDR is 50.96db.

3.4.2   500-Mhz input analog signal simulation results

Applying 500 Mhz input signal, the differential amplifier input and the square output waveforms are shown in Fig. 3.12 where the yellow, green, light blue and blue waveforms are the four input signals $V_{GN}+v_{in+}$, $V_{GN}+v_{in-}$,$V_{GP}+v_{in+}$, $V_{GP}+v_{in}$; the purple waveform is the square output waveform.   The square signal waveform (1Ghz) shown in Fig. 3.13 is after the square signal output after the low-pass filter, the voltage buffer amplifier and the gain control amplifier.

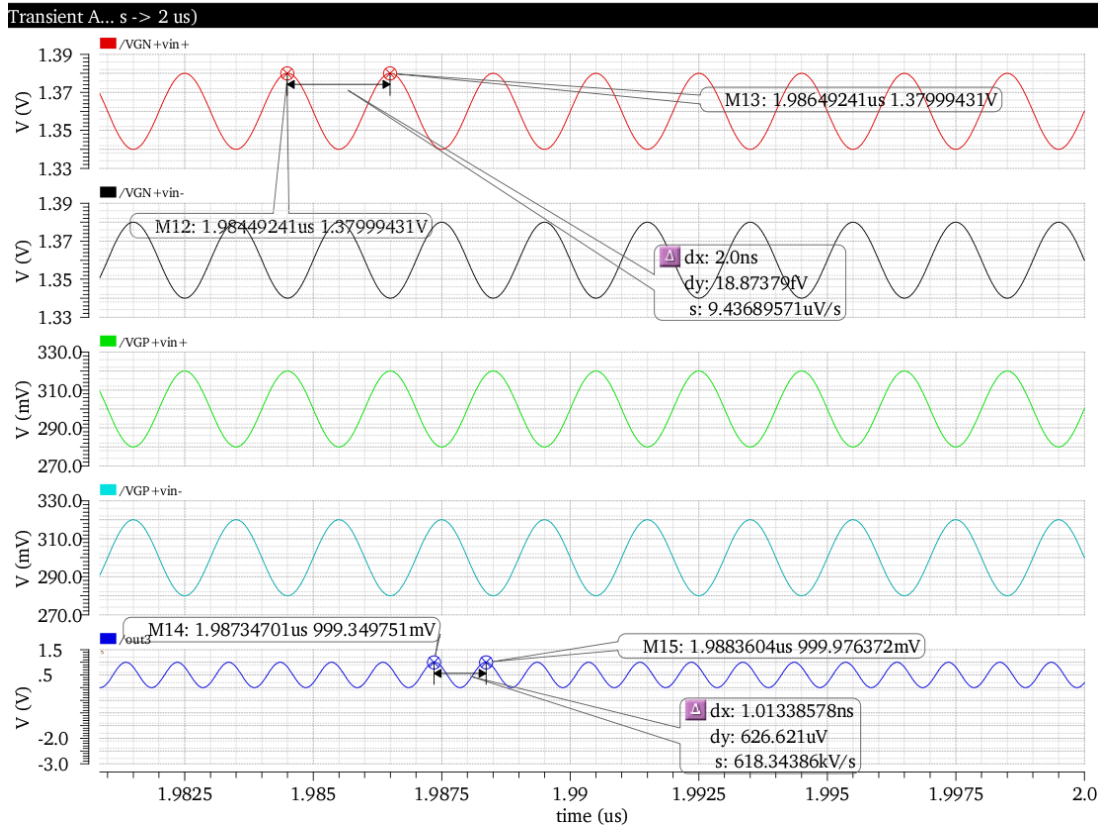Figure 3.12 The differential amplifier four input signals $V_{GN}+v_{in+}$, $V_{GN}+v_{in-}$, $V_{GP}+v_{in+}$,

$V_{GP}+v_{in}$ and the square output waveform for 500Mhz analog input signal
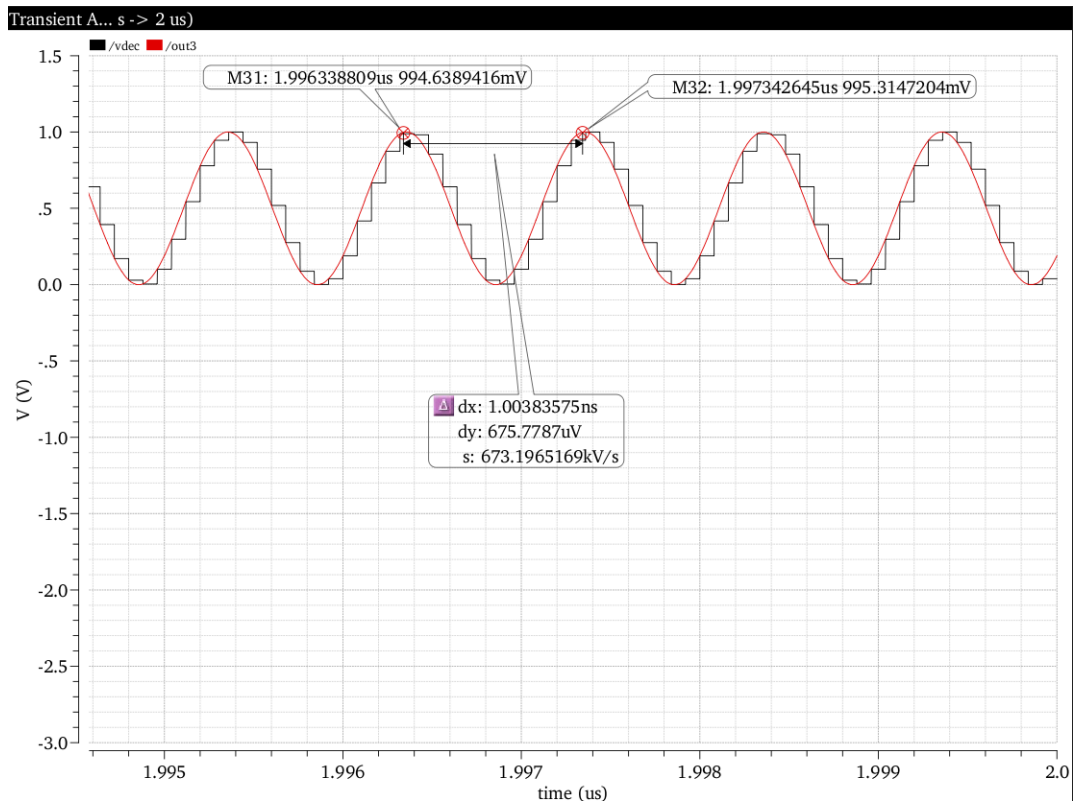
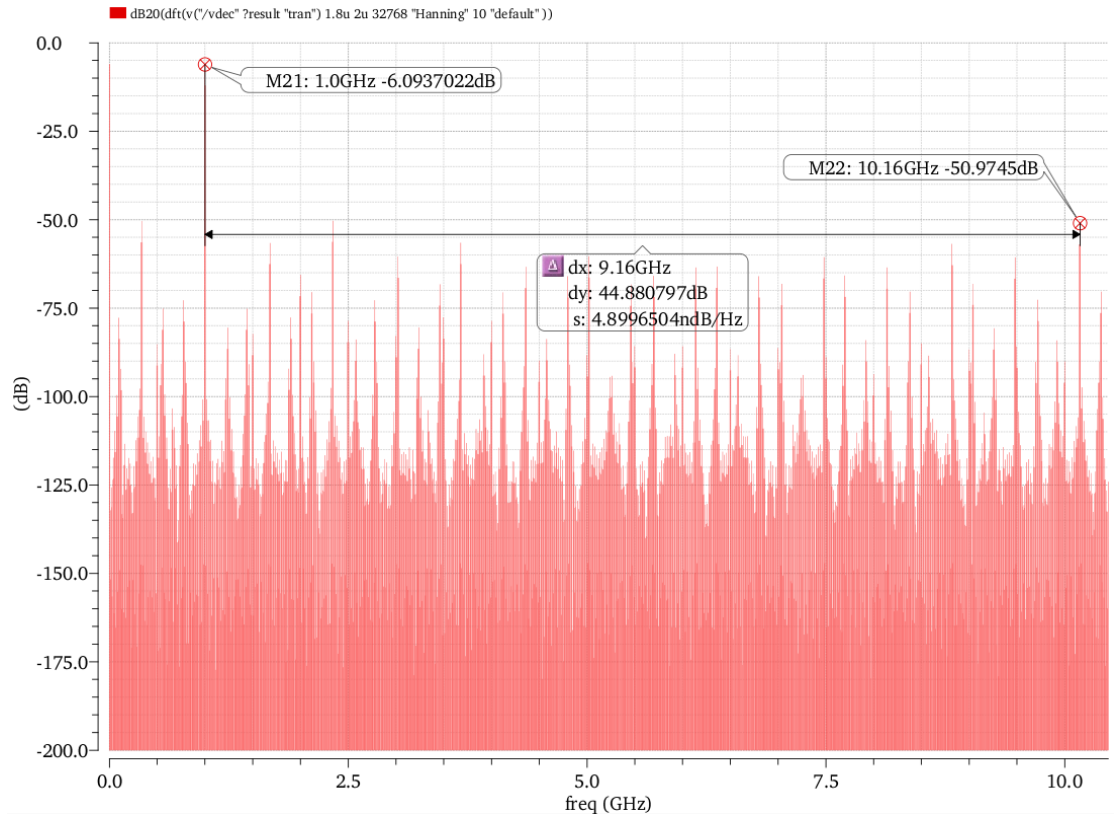Figure 3.13 The test bed output square signal waveform (1Ghz)

Figure 3.14 FFT spectrum of the test bed output square signal waveform (1Ghz) after the

10-b ADC

The FFT spectrum of the test bed output square signal waveform (1Ghz) after the

10-b ADC is shown in Fig. 3.14. The SFDR is 44.88db. Compare with the SFDR value

for 200Mhz in Fig. 3.9, the value has 6.08db damping from 50.96db. It means the

output for 500Mhz input signal is less stability and more noise than the output for

100Mhz input signal.

3.4.3   1-Ghz input analog signal simulation results

Applying 1 Ghz input signal, the differential amplifier input and the square output

waveforms are shown in Fig. 3.15 where the yellow, green, light blue and blue

waveforms are the four input signals $V_{GN}+v_{in+}$, $V_{GN}+v_{in-}$, $V_{GP}+v_{in+}$, $V_{GP}+v_{in}$; the

purple waveform is the square output waveform.   The square signal waveform (1Ghz)

shown in Fig. 3.16 is after the square signal output after the low-pass filter, the

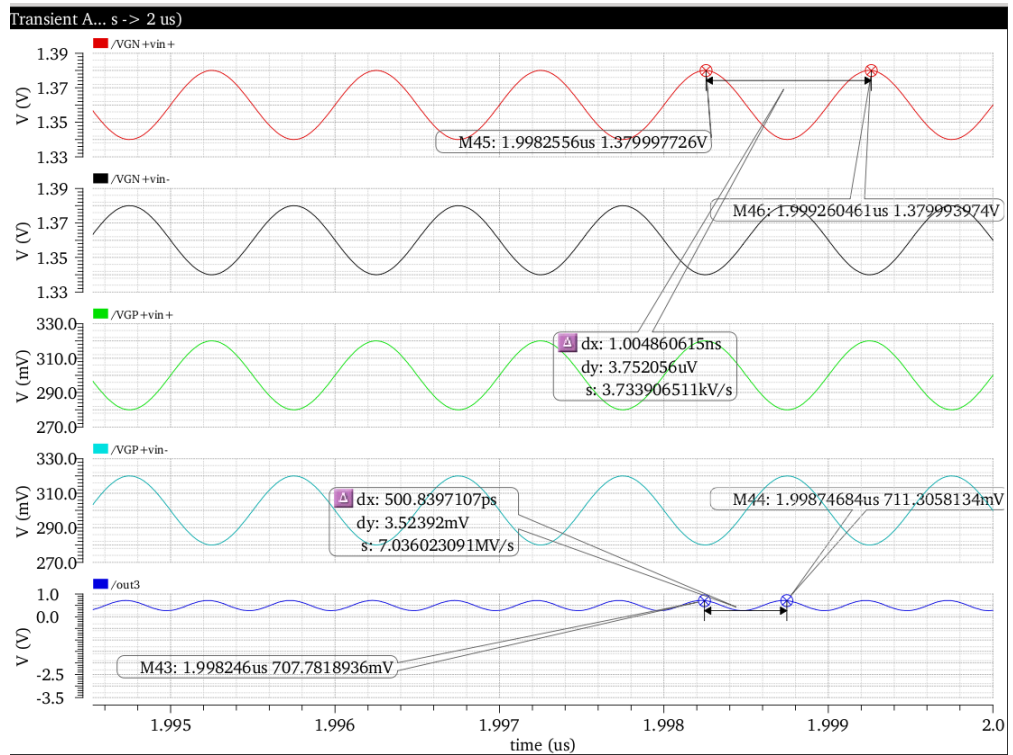voltage buffer amplifier and the gain control amplifier.

Figure 3.15 The differential amplifier four input signals $V_{GN}+v_{in+}$, $V_{GN}+v_{in-}$, $V_{GP}+v_{in+}$,

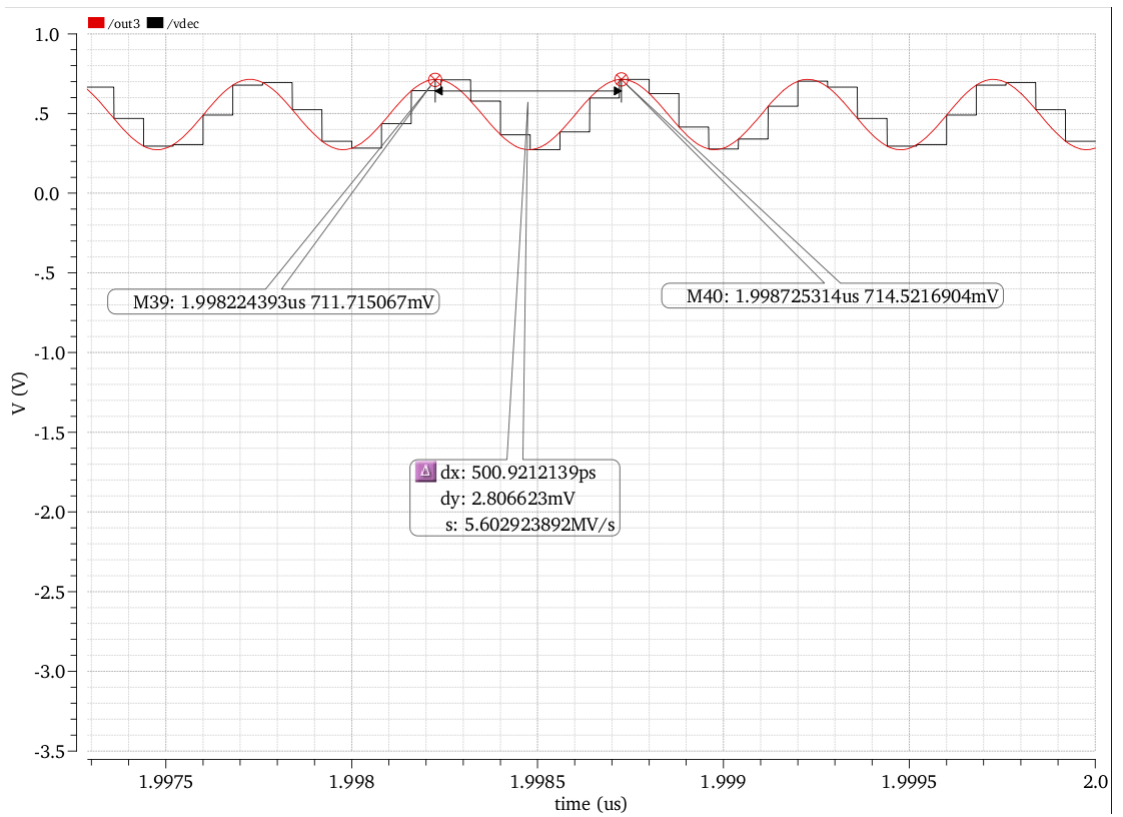$V_{GP}+v_{in}$ and the square output waveform for 1GMhz analog input signal

Figure 3.16 The test bed output square signal waveform (2Ghz)
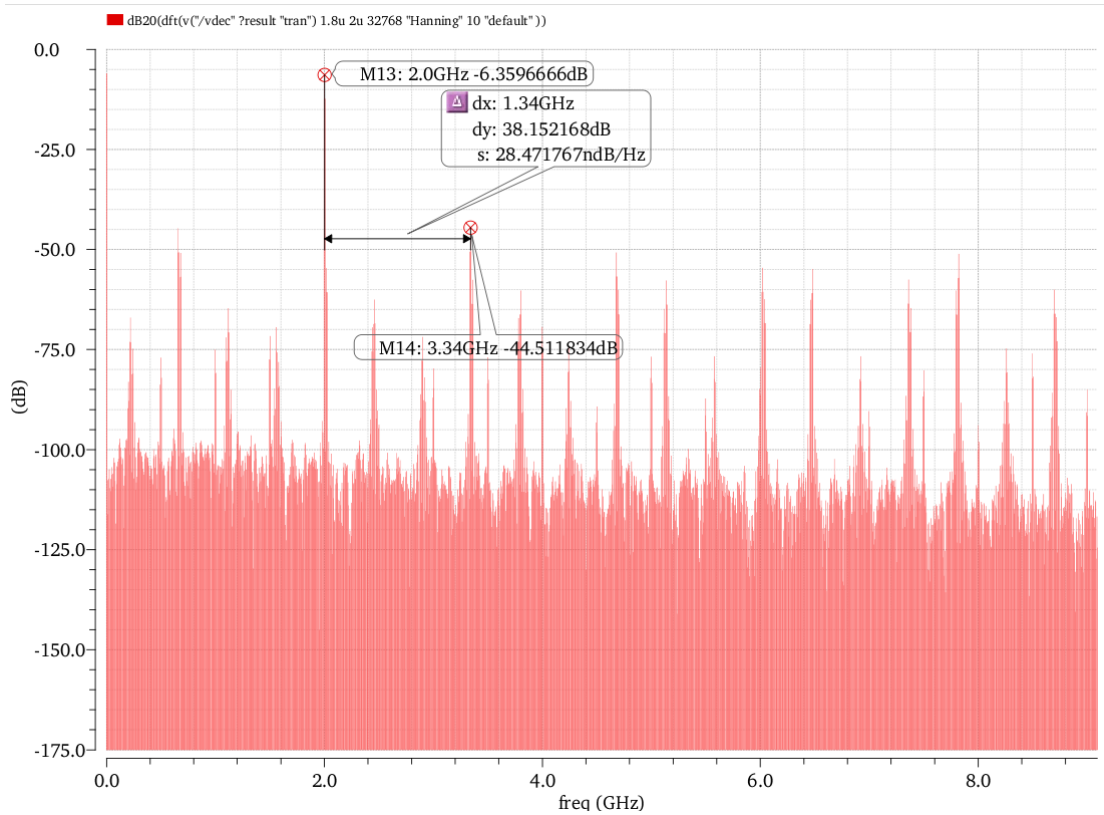

Figure 3.17 FFT spectrum of the test bed output square signal waveform (2Ghz) after the

10-b ADC

The FFT spectrum of the test bed output square signal waveform (2Ghz) after the 10-b ADC is shown in Fig. 3.17. The SFDR is 38.15db. The output waveform is clear and stable.

3.5 Simulation Results

This chapter first shows the circuit design of signal squarer and explains its operation principle and limitation. Next, Cadence software is used to evaluate the performance   The input signal frequency were varied from 100Mhz to 1Ghz. Table 3.6 shows SFDR for different input signal frequency.   SFDR decreases from 50.96db for 100Mhz to 38.15db for 1Ghz input signal.   The signal squaring circuit can work properly for a maximum input analog signal frequency up to 1.32Ghz.

Table 3.6 Input Frequency with output SFDR value

Input Signal Frequency	Output SFDR
100Mhz	50.96db
200Mhz	51.44db
300Mhz	48.68db
400Mhz	46.83db
500Mhz	44.88db
600Mhz	42.65db
700Mhz	41.94db
800Mhz	40.77db
900Mhz	39.07db
1Ghz	38.15db

The sign squaring circuit of [6,7] is based on differential amplifier design of Fig. 3.18. Table 3.7 shows SFDR comparison with [6,7].
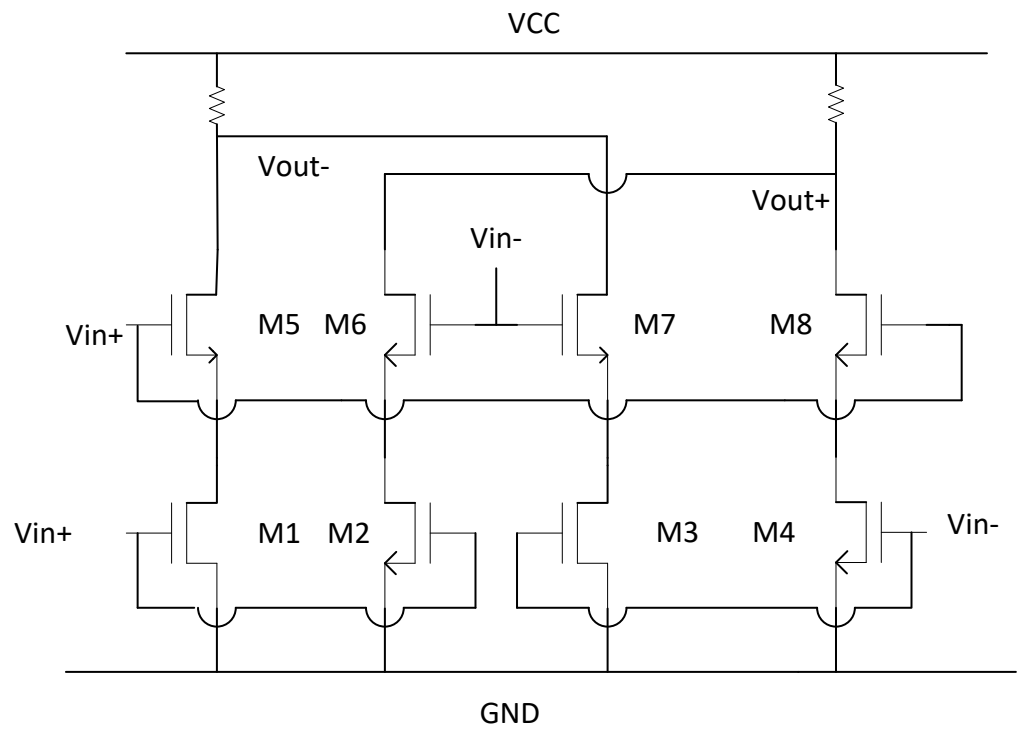
Figure 3.18   Differential amplifier based signal quaring circuit

Table 3.7 SFDR comparison

	[6]	[7]	This work
Frequency band(Ghz)	3	6	1.3
CMOS technology(nm)	180	90	180
Support voltage(V)	1.8	1	1.8
Average SFDR(db)	35.34	29.65	44.72

4   CONCLUSION

4.1 Conclusion

In this research, the proposed analog signal squaring circuit maintains good linearity and achieves high SFDR for input signal frequency up to 1-Ghz. Three design challenges were observed.   They are:

(1) The roll of current source and current mirror is important, which provides a stable DC bias voltage at an analog input signal to ensure that the next stage difference amplifier can function properly to square the input signal.   If the DC bias voltage of the input signal is not in the correct range, the signal squaring function can not be achieved.

(2) The roll of differential amplifier is important, which achieves squaring function of the analog input signal. The challenge of this part design is to optimize transistor sizes and V_{bias} values for M5 and M6.   Numertical simulation runs were conducted and based on these results the differential amplifier is optimized to generate clear and stable output waveforms.

(3) The roll of low pass filter is important, which reduces noise at the squared output signal.   And, through the output buffer a clear and stable output waveform is obtained.   In the test bed, a gain control amplifier is used to control the dynamic range of the squared output signal, which is fed to the 10-b ADC.   Thereafter, FFT analysis is conducts using Cadence toolset.

4.2 Future work

My future research includes:

(1) Increase input signal frequency range from 1 Ghz to 2 ~ 3 Ghz.   Improve my current differential amplifier design to function in a wider bandwidth while keep

linearity and high SFDR for the squared output waveform.

(2) Design new current sink source and current mirror circuit to provide DC bias voltage to the wide bandwidth differential amplifier and reduce the input noise.

(3) Design a new noise reduction filter in a wider bandwidth for the signal squaring output to improve the linearity and SFDR.

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