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A Reconfigurable SPICE-Based CMOS LNA Design in 90 Nm Technology using ADS RFIC Dynamic Link

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A Reconfigurable SPICE-Based CMOS LNA Design in 90 nm Technology Using ADS RFIC Dynamic Link

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering

by

Pushpak Vasanth RayuduArja
B.Tech., Acharya Nagarjuna University, India, 2013

2015
Wright State University

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December 17, 2015

I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Pushpak Vasanth RayuduArja ENTITLED A Reconfigurable SPICE-Based CMOS LNA Design in 90 nm Technology Using ADS RFIC Dynamic Link BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Electrical Engineering.

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ABSTRACT

Arja, Pushpak Vasanth Rayudu. MSEE, Department of Electrical Engineering, Wright State University, 2015. *A Reconfigurable SPICE-Based CMOS LNA Design in 90 nm Technology Using ADS RFIC Dynamic Link.*

In this thesis, a reconfigurable dual band CMOS LNA with a switching-type circuit topology is proposed. The reconfigurable dual-band LNA can be tuned to operating frequency of either 1.575 GHz for global positioning system (GPS) or 2.4GHz for WLAN 802.11b standards. The simulated results performed power gain of 11.2 dB and 12.4 dB, noise figure of 3.4 dB and 2.9 dB, input return loss(S11) of -25.26 dB and -21.4 dB, third-order input intercept point of -3.12 dBm and -2.137 dBm and the design dissipates 8.9 mW and 4.68 mW of power at 1.2 V power supply at the two frequency bands 1.575 GHz and 2.4 GHz, respectively.

A simple but efficient design methodology for a low noise amplifier is also presented in this thesis. This employs a design metric(cut off 'or' transit frequency, ft) to achieve optimum performance based on quick first order design space exploration. The simulated results for the two designs with input frequency of 2.4 GHz show power gain of 26 dB and 20.3 dB, and noise figure of 1.5 dB dB and 2.48 dB, an input return loss (S11) of -32.57 dB and -26.63 dB and the 1 dB compression point of -3.12 dBm and -2.137 dBm and the design dissipates 6 mW and 600 uW of power at 1.2 V power supply at the higher (24 GHz) and lower (5 GHz) transit frequencies, respectively.

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Dedicated to
My Parents

Introduction

Wireless communication applications are massively evolving. Countless intensive explorations on CMOS radio frequency (RF) front end circuits are being carried out, in response to the demand for a low power and low cost with high performance wireless front end. The low-noise amplifier (LNA) is a critical block in the receiver chain used to amplify very weak signals without adding a lot of noise, as the name implies. By employing an LNA, the overall outcome of noise figure resulting from the subsequent stages of the receiver chain can be minimized by having sufficient gain of the LNA. While the LNA itself also adds some noise to the received signal, it is very crucial that this LNA injected noise is as minimum as possible to facilitate proper retrieval of the signal in the later stages of the system [1].

Fig. 1.1 represents the simplified block diagram of an RF Narrow-Band Receiver [2] [6]. An antenna is present as a first block it receives the input message signal. The band select filter is used to select the desired narrow bandwidth from the signal received by the antenna. A LNA then amplifies the filtered low level input signal. The amplified signal may consist undesirable frequency components due to the non-linear components of the LNA. Typically due to the limitations in the implementation of ADC it operates at a lower

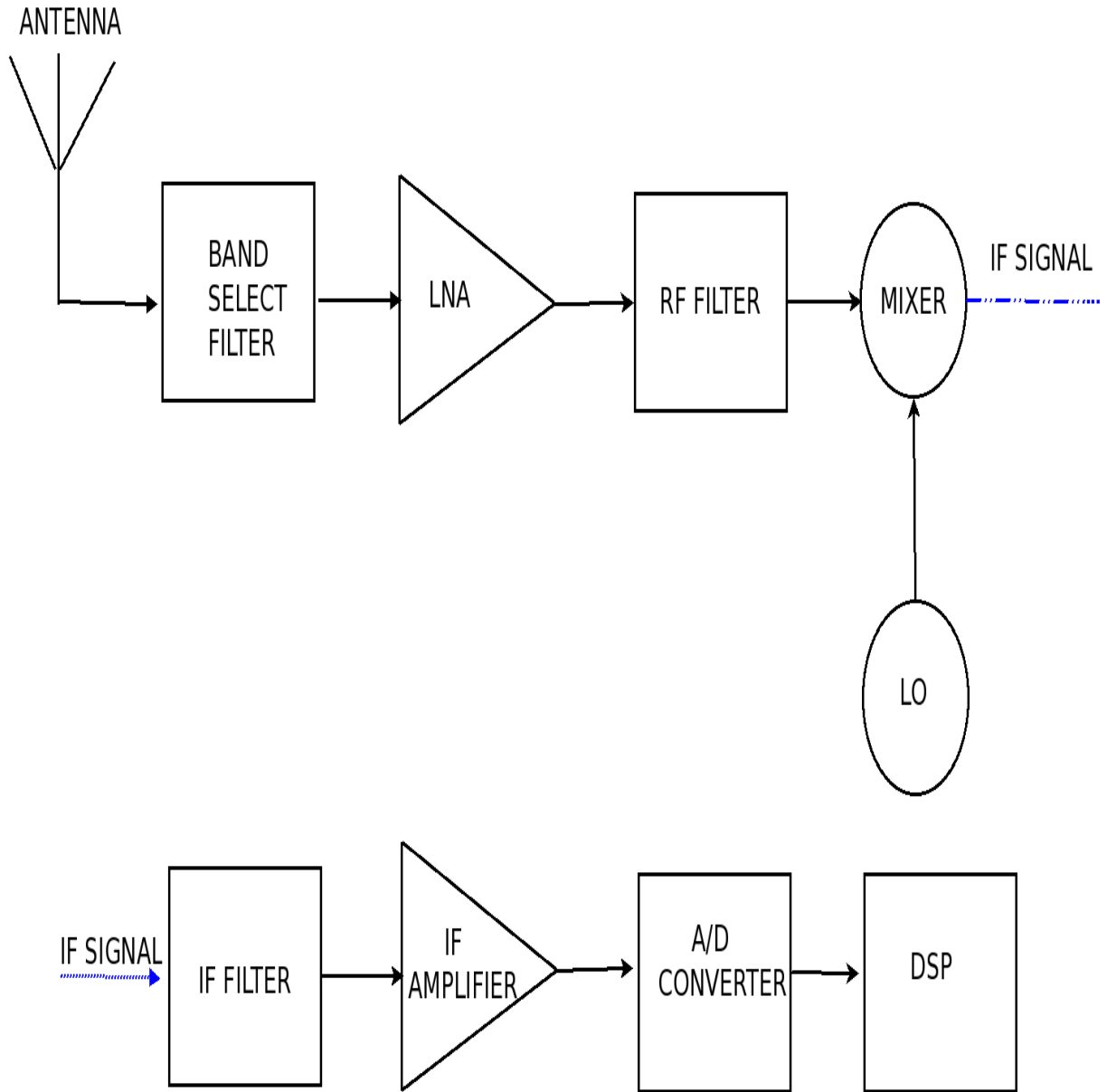


Figure 1.1: Simplified Narrow-Band RF Receiver [1] [2].

frequency range comparable to the input RF range, therefore one needs a mixer to down convert the received RF signal. Therefore, the high Radio Frequency filtered signal is then down converted into an intermediate frequency with the aid of an local oscillator and a mixer in order to facilitate the operation of the analog to digital converter(ADC). This is also referred to as demodulation. The digital signal processor is then used to process the IF

or Base-Band signal.

1.1 Motivation

Let's consider an amplifier shown in Fig. 1.2 with a power gain A_p and an input referred additive noise N_a . Furthermore, let's also suppose that its input and the output are matched to 50Ω .

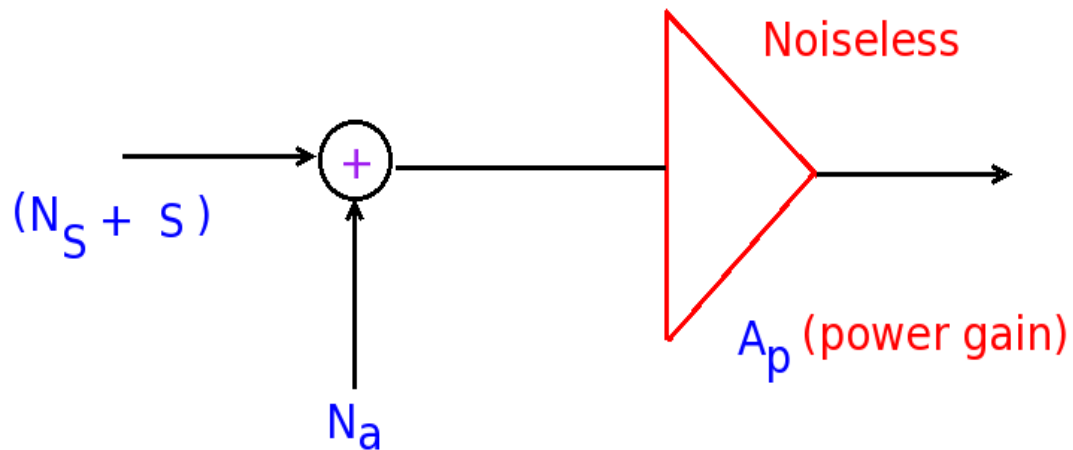


Figure 1.2: Simplified Narrow-Band RF Amplifier [2] [1].

The noise factor is defined as follows:

$$F = \frac{\text{Total output noise power}}{\text{Total output noise power due to source alone}} \quad (1.1)$$

If we consider the above case shown in Fig. 1.2 the noise factor of the above single stage turns out to be,

$$F = \frac{A_p(N_s + N_a)}{A_p N_s} \quad (1.2)$$

$$= 1 + \frac{N_a}{N_s} \quad (1.3)$$

Here, N_a and N_s are the signal power of input referred additive noise and noise power due to source, respectively. And A_p is the power gain. Let the signal power at the input be S .

The next step is to cascade several of these amplifiers as represented in Fig. 1.3.

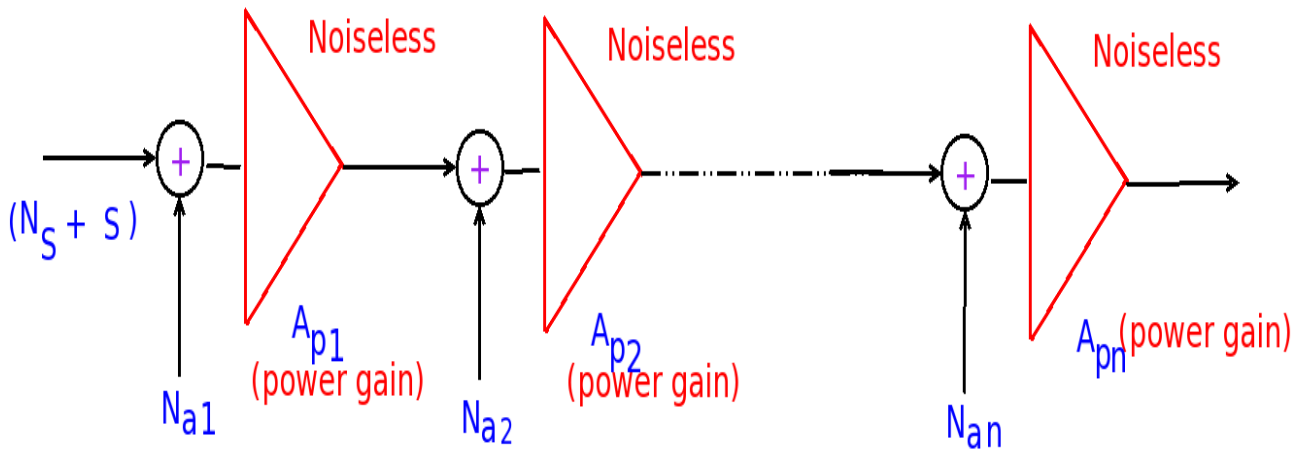


Figure 1.3: Cascaded Amplifier stages [1] [2] .

Now, let's apply the basic definition of the noise figure and figure out the total noise figure of the overall cascade structure.

$$N_{out} = (N_s + N_{a1}) \prod_{i=1}^n A_{pi} + N_{a2} \prod_{i=2}^n A_{pi} + \dots + N_{an} A_{pn} \quad (1.4)$$

Now, the output noise power due to N_s alone is given by Eq. (1.5),

$$N_{out}(N_s) = N_s \prod_{i=1}^n A_{pi} \quad (1.5)$$

So the noise figure for overall topology turns out to be (1.6),

$$F = \frac{N_{out}}{N_{out}(N_s)} \quad (1.6)$$

$$F = 1 + \frac{N_{a1}}{N_s} + \frac{N_{a2}}{A_{p1}N_s} + \dots + \frac{N_{an}}{\prod_{i=1}^n A_{pi}N_s} \quad (1.7)$$

Bearing in mind that the noise factor is measured at the output. Lets modify the above Eq. (1.7) a little as shown by Eq. (1.9), Here $F_1, F_2, F_3, F_4, \dots, F_n$ are the noise factors measured(or defined)for each individual cascaded blocks if one assume them being at the input block and themselves alone being the entire system(only that particular cascaded system is present)

$$F = 1 + (F_1 - 1) + \frac{(F_2 - 1)}{A_{p1}} + \frac{(F_3 - 1)}{(A_{p1}A_{p2})} + \dots + \frac{(F_n - 1)}{\prod_{i=1}^n A_{pi}} \quad (1.8)$$

$$F = F_1 + \frac{(F_2 - 1)}{A_{p1}} + \frac{(F_3 - 1)}{(A_{p1}A_{p2})} + \dots + \frac{(F_n - 1)}{\prod_{i=1}^n A_{pi}} \quad (1.9)$$

From the above expression we can conclude that the noise factor of the first stage amplifier directly adds, which should be obvious by now. But for the later stages it should Be intuitively appealing that the source noise is already gained till that stage and when compared with the noise generated by the preceded system alone with the already gained source noise it appears to be too small and the same is manifested in the above expression as, noise factor being degraded by a factor of the total gain products till that stage.

As the low-noise amplifier (LNA) is the first stage amplifier in the communication system's receiver chain it thus poses a design challenge.

1.2 Objective

- A design methodology for a reconfigurable LNA which can operate in two frequency bands (2.4 , 1.57 Ghz) is proposed.
- RFIC Dynamic link is used to obtain the component values for the proposed reconfigurable design.
- A SPICE based design methodology for a LNA is also proposed in this thesis for an efficient and accurate design.

1.3 Organization of thesis

The following section in this Chapter 1 describes the basic concepts employed in characterizing the performance of LNA. Chapter 2 deals with few existing reconfigurable LNAs and then explains the proposed design methodology for a multi-standard reconfigurable LNA. Chapter 3 discusses a simple design approach which is based on SPICE plots for the design of an efficient LNA. And Chapter. 4 concludes this thesis work.

1.4 Basic Concepts in LNA Design

As the low noise amplifier is a critical block in the receiver chain, proper metrics should be chosen and studied carefully in order to characterize its performance. This section deals

with general concepts that prove essential for analysis and design of low noise amplifier.

1.4.1 Impedance Matching and Noise Figure

1.4.2 S-Parameters

The impedance matrix (Z parameters) and admittance matrix (Y parameters) are usually employed in characterizing the impedance and admittance of a two port network operating at low frequencies. But for a network operating at high frequencies these two methodologies are inadequate. However, one can employ Scattering or S-parameter analysis. In such case the relationship between the reflected, incident power waves and the S-parameter matrix is given by the S-parameter matrix (1.10) [3]:

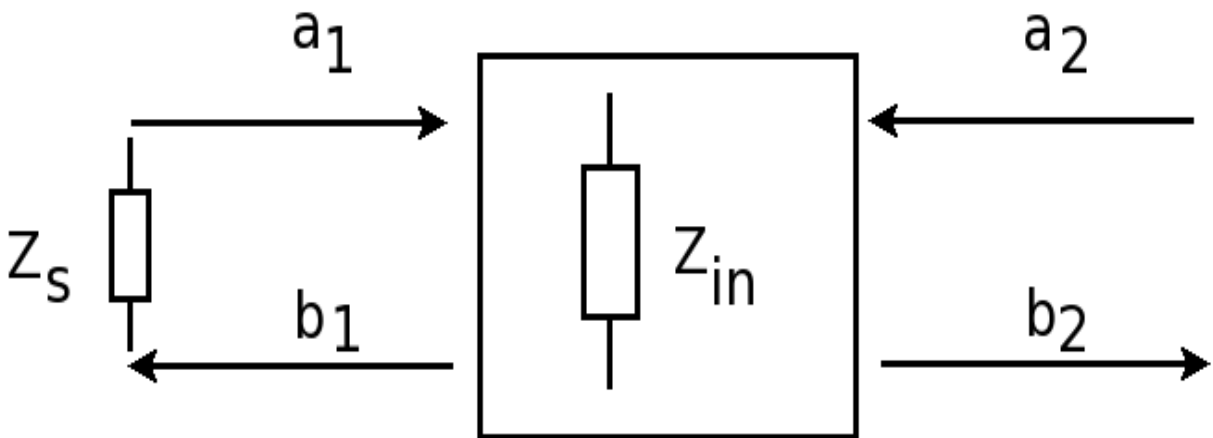


Figure 1.4: S-parameter for two port network [3].

Here, a_1 and a_2 are incident waves; b_1 and b_2 are reflected waves. Two-port network shown in Fig. 1.4 represents incident waves a_1, a_2 and reflected waves b_1, b_2 used in s-

parameter analysis.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \times \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (1.10)$$

Equation representation of the matrix (1.10) is as follows:

$$b_1 = S_{11}a_1 + S_{12}a_2 \quad (1.11)$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \quad (1.12)$$

$$S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} \quad (1.13)$$

$$S_{12} = \left. \frac{b_1}{a_2} \right|_{a_1=0} \quad (1.14)$$

$$S_{21} = \left. \frac{b_2}{a_1} \right|_{a_2=0} \quad (1.15)$$

$$S_{22} = \left. \frac{b_2}{a_2} \right|_{a_1=0} \quad (1.16)$$

Each 2-port S-parameter has the following generic descriptions:

- S_{11} is the input port voltage reflection coefficient
- S_{12} is the reverse voltage gain
- S_{21} is the forward voltage gain

- S_{22} is the output port voltage reflection coefficient.

1.4.3 Reflection Coefficient (S_{11})

The ratio of the reflected signal, b_1 , to the incident signal, a_1 in (1.13), is the reflection coefficient which can also be expressed as (1.17) [4].

$$\text{Reflection Coefficient}(S_{11}) = \frac{Z_{in} - Z_s}{Z_{in} + Z_s} \quad (1.17)$$

The amount of reflection done to the incident signal is indicated by S_{11} in (2.9). Here, Z_{in} is the input impedance of the amplifier and Z_s is the source impedance. If the source impedance is not matched with the load impedance, what comes into picture is the reflection. Signal which is incident into the amplifier gets reflected and goes back and produces multiple reflections. As the output resistance of the antenna is 50Ω , one need to match the input of the LNA to 50Ω to have the amplification done to the complete incident signal.

The second thing which might happen is, usually there exists a band select filter in between the antenna and the LNA. The design complexity with the band select filter arises from the fact that it will be off chip typically. Furthermore it is going to assume well 'matching' at the input and the output of itself. Now if the output is not well matched the characteristics of the filter changes and the losses may be different. Due to this, the filtering action might be different.

Bottom line is, one need to match the input of the LNA to 50Ω to make sure that the above problems are minimized. Proper techniques need to be figured out in order to get

50Ω input impedance. Furthermore, 50Ω impedance match also allows to simultaneously the conjugate power match, because impedance is purely real. Resulting in optimal power transfer, hence satisfying the system specifications.

Let's look at some cases in which impedance matching is done in various ways.

Direct resistor matching

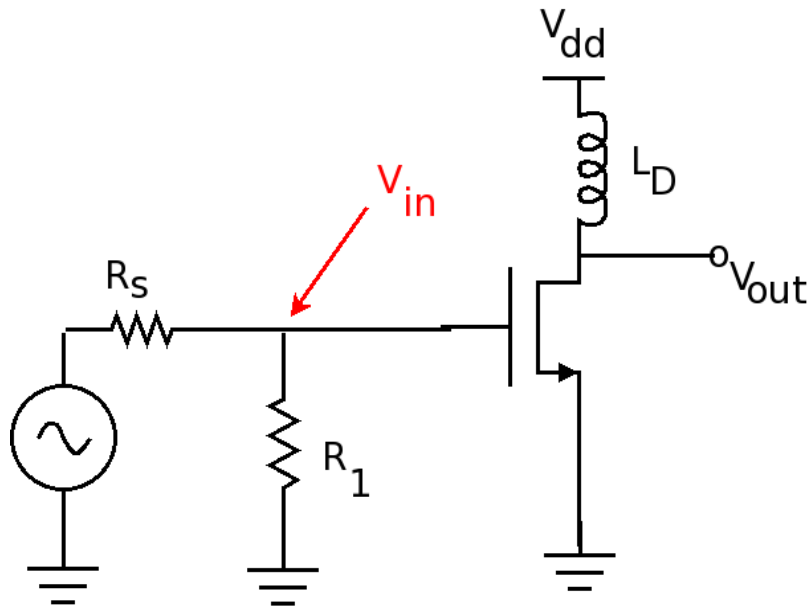


Figure 1.5: Resistor input match with common source stage [5].

If the input is simply terminated with a resistor of 50Ω (R_1) and considering the input gate capacitance is low at the operating frequencies as shown in Fig. 1.5. Then the noise factor due to this termination is given by the following expression (1.18) [5].

$$F = 2 + \frac{4\gamma}{\alpha} \cdot \frac{1}{g_m R_s} \quad (1.18)$$

$$NF_{min} = 3 \text{ dB} \quad (1.19)$$

Where, g_m is the transconductance, R_s is the source resistance, γ and α are constants in Eq. (1.18)

For low frequencies, a capacitor acts as a high impedance and fairly R_s is equal to R_1 in a broadband range. But the disadvantage is that the input voltage is dropped by half. This kind of termination adds a minimum of 3 dB noise figure as shown in (1.19), which is not accepted in sub-dB applications.

Common gate amplifier

Considering a common gate configuration as shown in Fig. 1.6, the impedance matching can be done by choosing $R_s = 1/g_m$. But in this case, the power dissipation would be high as we need a high value g_m to get $1/g_m = 50 \Omega$. The minimum noise figure in this case is higher than that of the resistive terminated common source amplifier.

Then the noise factor due to this termination is given by the following expression (1.21) [5].

$$F = 1 + \frac{\gamma}{\alpha} + \frac{4R_s}{R_D} \quad (1.20)$$

Here, R_s is the input source signal, R_D is the parasitic resistance of the drain inductor L_D [5].

$$NF_{min} = 2.2 \text{ dB} \quad (1.21)$$

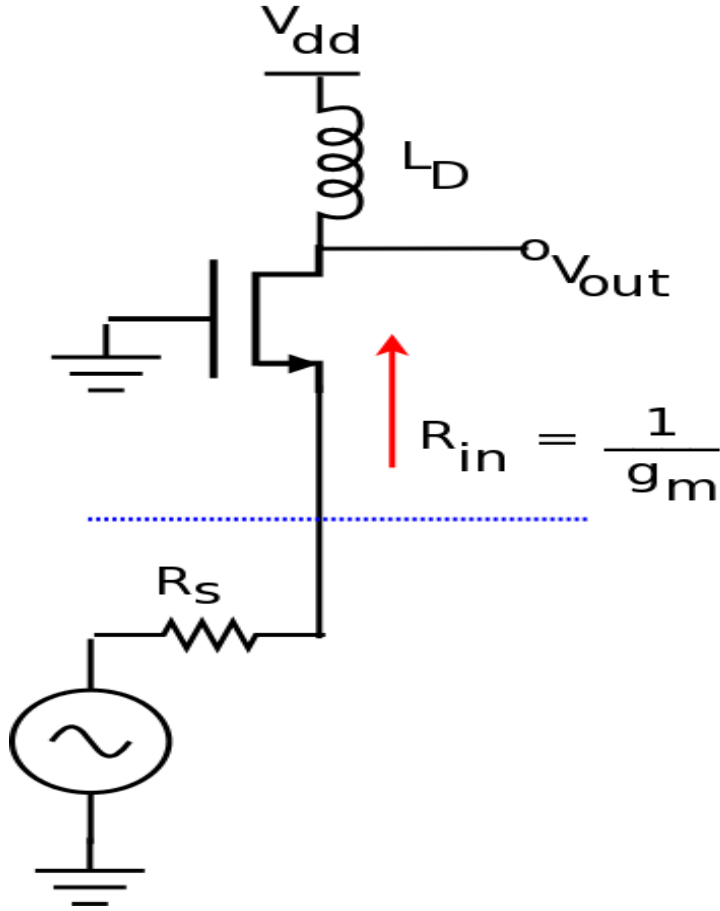


Figure 1.6: Resistor input match with common gate stage.

Inductive source degenerated common source amplifier

Typically, many narrow band LNA designs utilize inductively source degenerated common source topology as seen in Fig. 1.7, as it has been proven to be a finer choice for obtaining optimum noise and good resistive input matching simultaneously.

The input impedance for this configuration is given by (1.22) [6]

$$Z_{in} = \frac{(g_{m1})L_s}{C_{gs1}} + j \left[\omega_H(L_s + L_g) - \frac{1}{\omega_H(C_{gs1})} \right] \quad (1.22)$$

Where, C_{gs1} is the gate to source capacitance of M_1 in Fig. 1.7. By Tuning L_g , L_s and

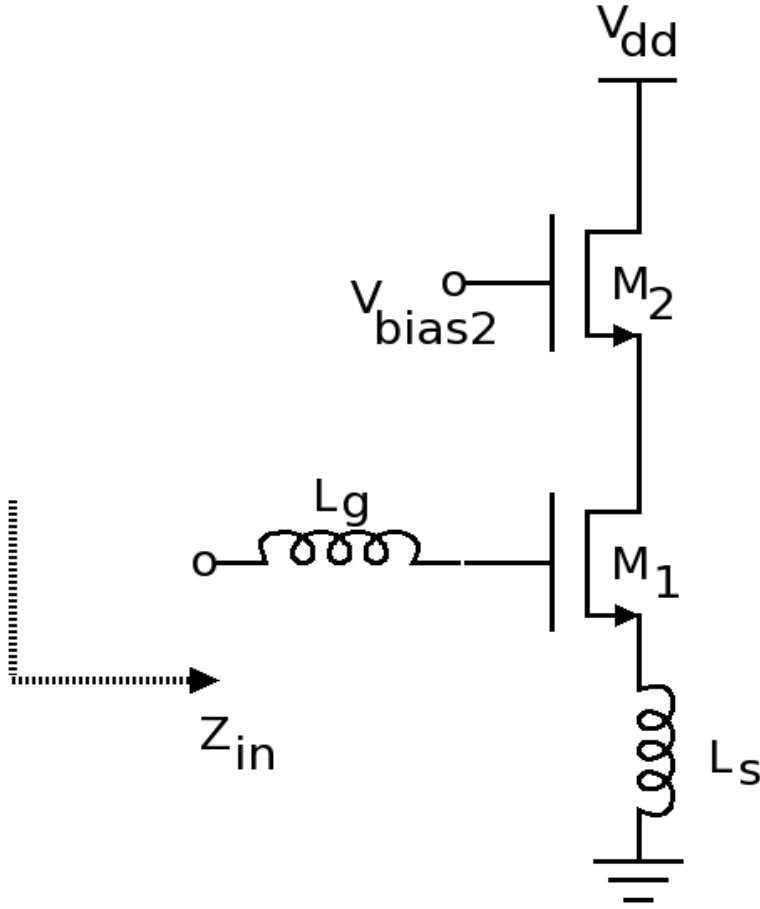


Figure 1.7: Schematic of the conventional LNA input stage.

C_{gs1} such that the imaginary term equals to zero at the input frequency. One can get the real term equal to 50Ω without actually using any resistor. This also provides simultaneous power matching. This kind of configuration is most widely employed for designing the narrow band LNAs.

The noise factor due to this configuration is given by the following expression (1.23).

$$F = 1 + \gamma g_m R_s \left(\frac{\omega_o}{\omega_T} \right)^2 \quad (1.23)$$

The minimum noise figure of this topology can be as low as 0.5 dB [6]. Comparing the minimum noise factors obtained in (1.19), (1.21) with that of the common source tells that

it is preferable to choose common source for the narrow band designs.

1.4.4 Linearity

Linearity is another key metric in the LNA design. The relation between input and output of a non-linear system is generally approximated as follows [6].

$$x_{out}(t) = A_1x_{in}(t) + A_2x_{in}^2(t) + A_3x_{in}^3(t) + \dots \quad (1.24)$$

Consider a two tone signal given by (1.25).

$$x_{in}(t) = x_1\cos(\omega_1t) + x_2\cos(\omega_2t) \quad (1.25)$$

Linearity is usually characterized by using two parameters, third order intercept point, IIP3 and 1dB compression point, P1dB. Generally, a two tone signal shown in (1.25) is considered as an input with ω_1 and ω_2 as fundamental frequency terms. and then applied to the non-linear system modeled by equation (1.24). The square terms and cubic terms on expansion results in frequency components which are not harmonics of the fundamental tones and are known as inter modulation components [6].

If the system considered is a complete linear system, then the output consists only terms represented by (1.26)

$$A_1x_{in}(t) = A_1[x_1\cos(\omega_1t) + x_2\cos(\omega_2t)] \quad (1.26)$$

But usually the systems considered cannot be completely linear and contains the following square and cubic terms shown in (1.27) and (1.28) [6].

The minimum noise figure in this case can go as low as 1 dB based on the chosen cut off frequency, which will be explained in much detailed in further sections.

$$\begin{aligned}
 A_2 x_m^2(t) &= \frac{A_2 x_1^2}{2} [\cos(2\omega_1 t) + 1] \\
 &+ \frac{A_2 x_2^2}{2} [\cos(2\omega_2 t) + 1] \\
 &+ A_2 x_1 x_2 [\cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t]
 \end{aligned} \tag{1.27}$$

$$\begin{aligned}
 A_3 x_m^3(t) &= \frac{A_3 x_1^3}{4} [\cos(3\omega_1 t) + 3\cos(\omega_1 t)] \\
 &+ \frac{A_3 x_2^3}{4} [\cos(3\omega_2 t) + 3\cos(\omega_2 t)] \\
 &+ \frac{3}{4} A_3 x_1 x_2^2 [2\cos(\omega_1 t) + \cos(2\omega_2 + \omega_1)t + \cos(2\omega_2 - \omega_1)t] \\
 &+ \frac{3}{4} A_3 x_1^2 x_2 [2\cos(\omega_2 t) + \cos(2\omega_1 + \omega_2)t + \cos(2\omega_1 - \omega_2)t]
 \end{aligned} \tag{1.28}$$

The output voltage contains the following frequency components:

- fundamental components ω_1 and ω_2 ;
- harmonics of the fundamental components $2\omega_1, 2\omega_2, 3\omega_1, 3\omega_2, \dots$
- intermodulation products $\omega_2\omega_1, \omega_1 + \omega_2, 2\omega_1\omega_2, 2\omega_2\omega_1, 2\omega_1 + \omega_2, 2\omega_2 + \omega_1, 3\omega_1 2\omega_2, 3\omega_2 2\omega_1, \dots$

It can be observed from (1.27) and (1.28) that the second order intermodulation terms has components at $\omega_1 + \omega_2$, and $\omega_1 - \omega_2$ frequencies. While, the third order intermodulation terms has components at $2\omega_1 \pm \omega_2$, and $2\omega_2 \pm \omega_1$ frequencies.

IIP3

Out of all these frequencies, the third-order inter modulation (IM) components is of importance due to the fact that they lie closer to the fundamental frequency components and it is not possible to filter them out. Measuring the relative strength of these signals is helpful in categorizing the effect of these IM products on the desired output.

If the input amplitude increases the output amplitude of the IM components increases more sharply as they are proportional to A^3 in Eq. (1.28). ($A = x_1 = x_2$, being the amplitude of the two input tones in expression (1.25)). As a result if the amplitude of the input is allowed to raise without imparting any constraint.

$$A_{IIP3} = \sqrt{\frac{4}{3} \left| \frac{A_1}{A_3} \right|} \quad (1.29)$$

At a particular value of the input amplitude represented as (A_{IIP3}) amplitude of the IM components eventually matches with that of the fundamental tones at the output. The magnitude of that A_{IIP3} given by (1.29) serves as an upper limit for the input magnitude. On the other hand, if the input magnitude, A is excessively small, then the output IM components become comparable with the noise floor of the output spectrum.

A1dB

Depending upon the sign of the amplitude, A_3 in Eq. (1.27) in the third order term of the expanded series, it causes either expansion or compression to the overall gain. Usually it

is negative. As a result when the input amplitude increases, the output amplitude reaches saturation, causing amplitude gain compression. The point at which the amplitude gain of the amplifier deviates from the extrapolated ideal linear amplifier by 1 dB is called the 1-dB compression point.

To calculate the input 1-dB compression point, we equate the compressed gain, $A_1 + \frac{3}{4}A_3A_{in,1dB}^2$, to 1 dB less than the ideal gain, A_1 [6] :

$$20\log\left|A_1 + \frac{3}{4}A_3A_{in,1dB}^2\right| = 20\log|A_1| - 1\text{dB}. \quad (1.30)$$

It follows that,

$$20\log\left|1 + \frac{3}{4}\frac{A_3}{A_1}A_{in,1dB}^2\right| = -1\text{dB}. \quad (1.31)$$

$$A_{1dB} = \sqrt{\frac{4}{3}\frac{A_1}{A_3}} \quad (1.32)$$

1.4.5 Noise Analysis

For the noise analysis purpose, let's consider the standard CMOS noise model as shown in Fig. 1.8 [7]. The dominant noise source in CMOS devices is the channel thermal noise. This source of noise is commonly modeled as a shunt current source in the output circuit of the device. [8] [9] [10].

The noise figure of the LNA can be computed by carefully examining the input equiv-

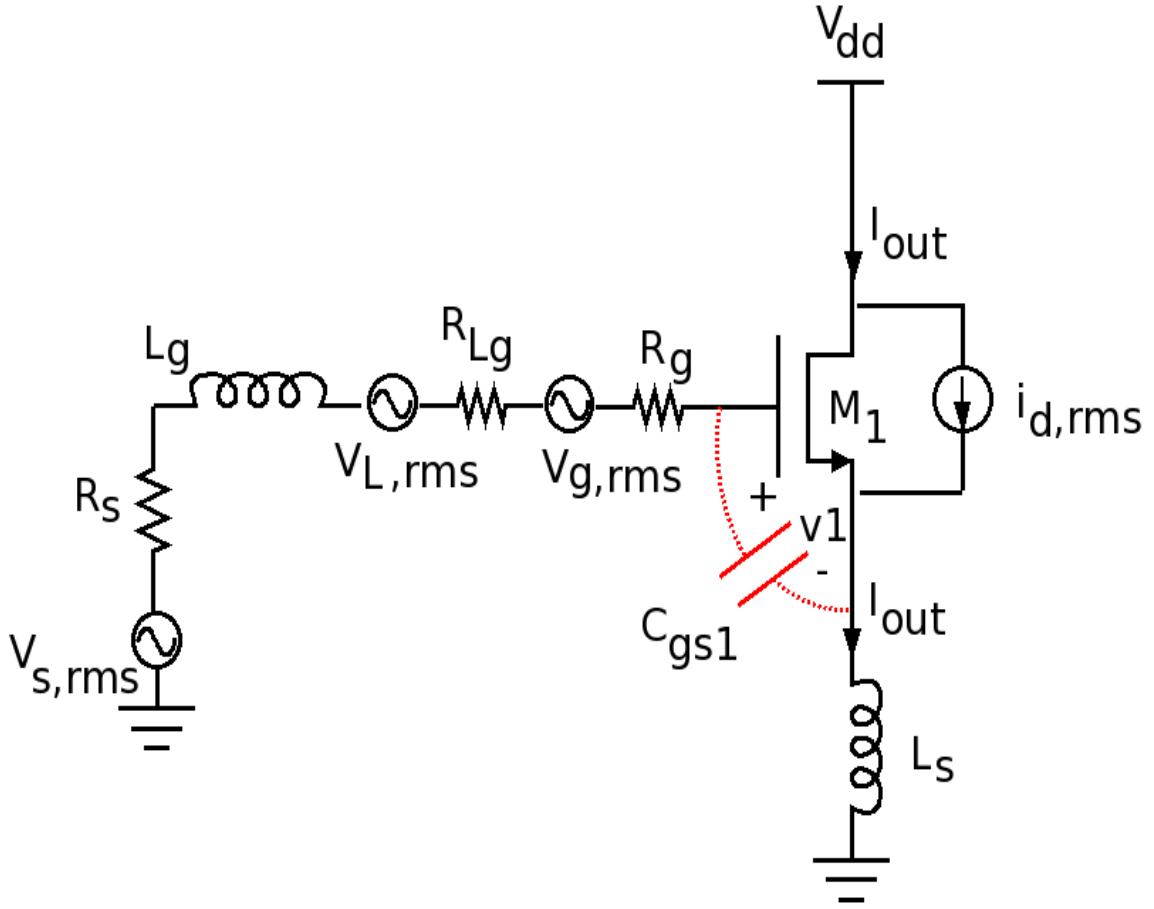


Figure 1.8: Common source input equivalent circuit model for noise calculations

alent circuit shown in Fig. 1.8. In this equivalent circuit, the channel thermal noise is represented by $i_{d,rms}$, the gate resistance of the MOSFET (M1) is represented by R_g , the input source resistance is represented by R_s and R_{Lg} represents the parasitic resistance of the inductor L_g .

Let $V_{s,rms}$, $V_{L,rms}$ and $V_{g,rms}$ be the root mean squared noise source representing the noise due to the $50\ \Omega$ input source resistance, parasitic resistance of the inductor L_g and gate resistance of the MOSFET M1, respectively.

Careful observation into the input section of Fig. 1.8 indicates that the inductor L_g , L_s forms a series resonant circuit with the gate-source capacitance C_{gs1} of M1, therefore the

effective transconductance is given by (1.33) [7]. Where Q_{in} is the effective of the amplifier input circuit, R_s and R_{Lg} represents the parasitic resistance of the inductor L_g , ω_T is the angular cut-off frequency and ω_o is the angular input frequency.

$$G_m = g_{m1} Q_{in} = \frac{g_{m1}}{\omega_o C_{gs} (R_s + R_{Lg} + R_g + \omega_T L_s)} \quad (1.33)$$

$$= \frac{\omega_T}{\omega_o (R_s + R_{Lg} + R_g + \omega_T L_s)} \quad (1.34)$$

R_{Lg} and R_g can be neglected as they would be very small relative to $(R_s + \omega_T L_s)$. Therefore,

$$G_m = g_{m1} Q_{in} = \frac{\omega_T}{\omega_o (R_s + \omega_T L_s)} \quad (1.35)$$

As the output drain current is proportional to the input voltage on C_{gs} of M1, output current due to these three resistive noise sources in a 1 Hz bandwidth is given by

$$\overline{I_{out1}^2} = \overline{I_{out,R_s}^2} + G_m^2 (V_{L,rms}^2 + V_{g,rms}^2) \quad (1.36)$$

Let I_{out,R_s} be the output drain current due to the 50 Ω input source resistance alone.

$$\overline{I_{out,R_s}^2} = G_m^2 (V_{s,rms}^2) \quad (1.37)$$

$$\overline{I_{out1}^2} = G_m^2 (V_{s,rms}^2 + V_{L,rms}^2 + V_{g,rms}^2) \quad (1.38)$$

$$\overline{I_{out1}^2} = G_m^2 4KT (R_s + R_{Lg} + R_g) \quad (1.39)$$

As the source is inductively degenerated by L_s . Output drain current, $\overline{I_{out2}^2}$ due to the channel thermal noise of the MOSFET M1 alone in a 1 Hz bandwidth in this configuration is given by

$$I_{out2} = \frac{I_{d,rms}}{1 + \frac{g_{m1}L_s}{C_{gs}R_s}} \quad (1.40)$$

But for a series resonance $\frac{g_{m1}L_s}{C_{gs}} = R_s$ at resonant frequency, resulting

$$I_{out2} = \frac{I_{d,rms}}{2} \quad (1.41)$$

$$I_{d,rms} = \sqrt{4KT\gamma g_{do}} \quad (1.42)$$

$$\overline{I_{out2}^2} = \frac{I_{d,rms}^2}{4} = KT\gamma g_{do} \quad (1.43)$$

The total noise factor for an amplifier can be defined as (1.44) evaluated at, T = 290

K. [8] [9]

$$F = \frac{\overline{I_{out1}^2} + \overline{I_{out2}^2}}{\overline{I_{out,R_s}^2}} \quad (1.44)$$

$$F = \frac{G_m^2 4KT(R_s + R_{Lg} + R_g) + KT\gamma g_{do}}{G_m^2 4KTR_s} \quad (1.45)$$

$$F = 1 + \frac{R_{Lg}}{R_s} + \frac{R_g}{R_s} + \frac{\gamma g_{do}}{4G_m^2 R_s} \quad (1.46)$$

$$F = 1 + \frac{R_{Lg}}{R_s} + \frac{R_g}{R_s} + \gamma g_{do} R_s \left(\frac{\omega_o}{\omega_T} \right)^2 \quad (1.47)$$

where γ is around 2/3 for long channel. Note that γ value is relatively higher in sub-micron technology, typically [11]. Expression (1.47) is used in this thesis to formulate the design methodology.

Reconfigurable LNAs

2.1 Introduction

Over the past few years, proliferating demand for wireless local-area networks(WLAN's) has stimulated the introduction of new WLAN standards to meet various application requirements [6]. If each frequency band is to be implemented with one set of special hardware, area would be large, as a result the total cost would turn out to be too expensive. As, multiple sets of hardware in parallel would be needed to provide access for each frequency band of operation. Furthermore, predicaments faced in designing a reconfigurable multi-band LNA primarily arose from the fact that it has to dispense different functions such as input impedance matching at different operating frequency standards, low noise figure, sufficient power gain and adequate linearity. Further arduousness is reciprocal reliance of all these functions. As a result, many accommodations should be done to obtain decent overall accomplishment of required specifications.

One of the technical deadlocks in realizing a multi-standard receiver is realization of a low-noise amplifier as it is an essential module in the receiver chain. Its primary function is amplification of the received signal from an antenna with as little 'self added noise' as

possible [6].

2.2 Prior Work on Reconfigurable LNAs

Many efforts were put into the design of reconfigurable low-noise amplifiers so far. An approach using common drain amplifier was discussed [12]. Here reconfigurability is achieved as follows. The design is tuned by changing the value of the inductor L_g . This is achieved by employing an amplifier to provide the necessary scaling for the inductor L_g as shown in Fig. 2.1. The input impedance can be expressed as following [12].

$$Z_{inA} = \frac{j\omega L_g}{1 + g_{m(M_{s1})}R_A} + \frac{R_A}{1 + g_{m(M_{s1})}R_A} + Z_{LNA} \quad (2.1)$$

As shown in Fig. 2.1, in the above expression (2.1), the scaling factor $1 + g_{m(M_{s1})}R_A$ can be nicely exploited to scale the inductance of L_g . Where $g_{m(M_{s1})}$ is the transconductance of the transistor M_{s1} . The capacitor C_c is chosen to be large so that it acts as short at high frequencies and the inductor RFC is chosen to be large so that it acts as a open circuit at high frequencies. R_A is the resistance of transistor M_A biased such that it operates in the triode region, whose resistance value can be controlled by the gate-source voltage. Therefore, by tuning the transistor M_A gate voltage the inductance effective value can be tuned and the operating frequency can be changed at which the real input impedance equals to the

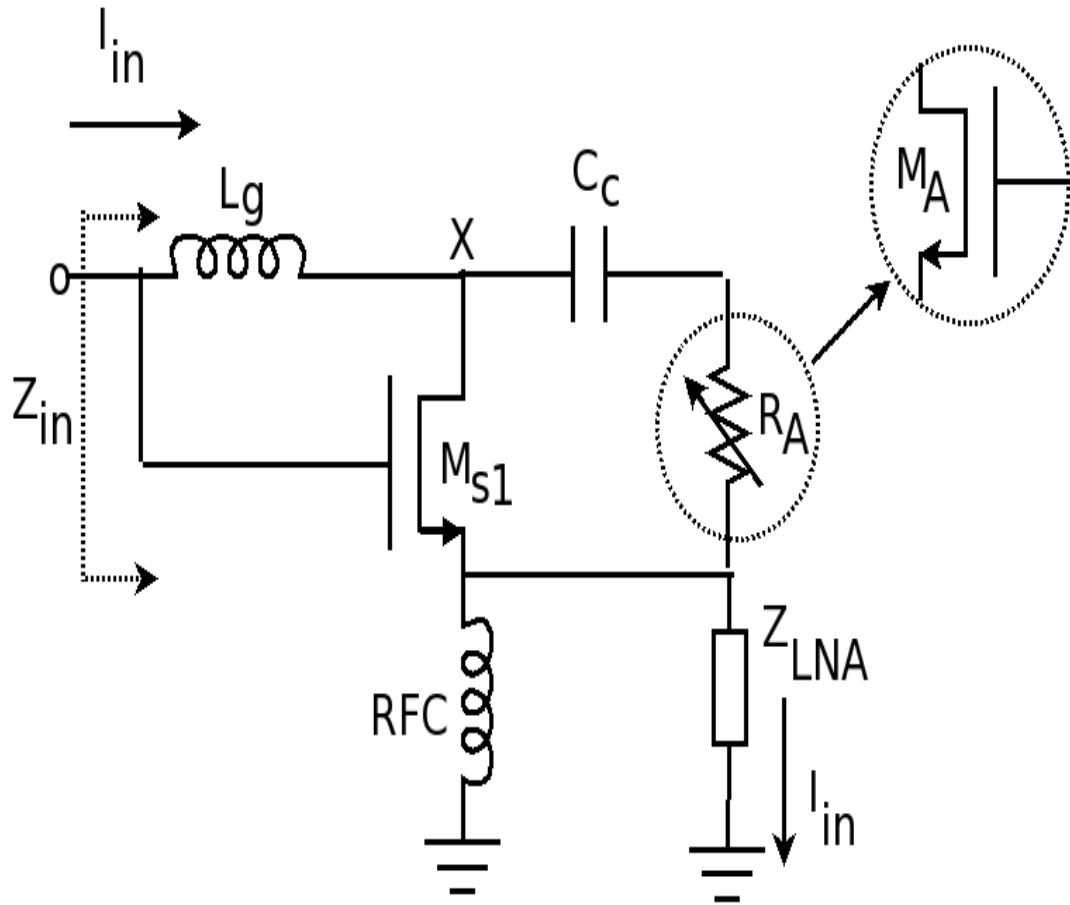


Figure 2.1: Tunable floating inductor architectures based on a common drain configuration [12].

required value. Here the limiting factor is that tuning cannot be performed to achieve broad range of frequency coverage, which is a bottle neck in this particular implementation.

So far many contributions were made to bring about reconfigurable dual-band LNA's by switching capacitors [13], [14], and switching inductors [15], [16]. Nevertheless, most of the designs still need additional passive components to provide the required dual band operation. An approach was presented in [17], with reduced number of inductors to achieve continuous reconfigurability but within a narrow bandwidth. The proposed approach in this thesis can achieve discrete reconfigurability over a significant wide range. In general,

reconfigurability in any design can be adopted through tuning. Though both discrete and continuous tuning techniques [18] [19] [20] [21] can be used to meet the requirement, discretely tuned design strategies have drawn more attention than the continuously tuned ones owing to the fact that the former designs can be easily reconfigured by means of switching (ON/OFF) passive components

2.3 Proposed Design: A Dual-Band Reconfigurable LNA for Multi-Standard Receiver using 90 nm CMOS Technology

The proposed reconfigurable dual band LNA design as shown in Fig. 2.2 uses an inductively degenerated cascode topology with LC tank band pass filter to allow a good trade-off between high gain, low noise, and low power consumption [6], [22]. Reconfigurability in the design is achieved through switching and modulating the transconductance of M_1 . This thesis primarily focuses on the design methodology of a CMOS LNA for reconfigurable front-end architectures. A unique circuit topology for the reconfigurable dual-band LNA operating at 1.575 or 2.4-GHz is presented. With the proposed design technique, the required LNA performance can be achieved at different frequency bands with a potentially reduced hardware cost.

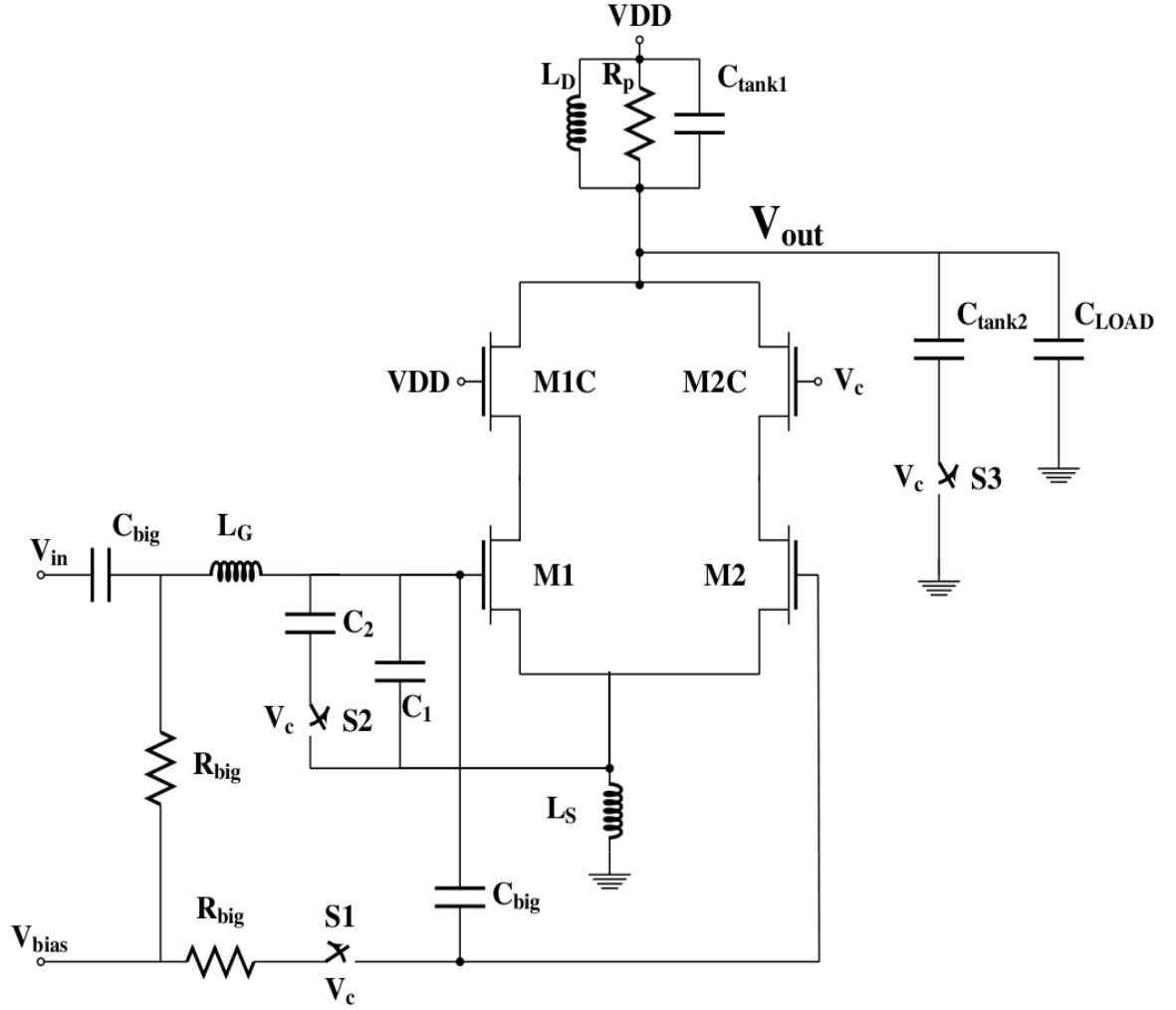


Figure 2.2: Schematic of the Proposed Reconfigurable Dual Band LNA.

2.3.1 Design Description of Reconfigurable LNA.

The complete schematic of the proposed design is shown in Fig. 2.2. A cascode amplifier is built by M1, M1C and M2, M2C, respectively. M1C and M2C are used for decoupling input and output signals, increasing the output impedance and the reverse isolation. To minimize Miller input capacitance effect, M1C and M2C are chosen to be the same as M1 and M2 (same geometry), respectively [6]. In this design, the capacitors C_1 and C_2 are chosen to achieve dual band operation and to decouple the LNAs power gain from noise

[23]. Same bias voltage V_{bias} is given for both M1, M2. The proposed design has the ability to operate in two modes of operations 1.575 GHz, called from now on as lower band and 2.4 GHz, called from now on as upper band. Mode of operation can be easily set through switching. Complete design methodology for reconfigurable operation is described in the following sub-sections.

2.3.2 Design Operation at Higher Band (2.4 GHz) Mode

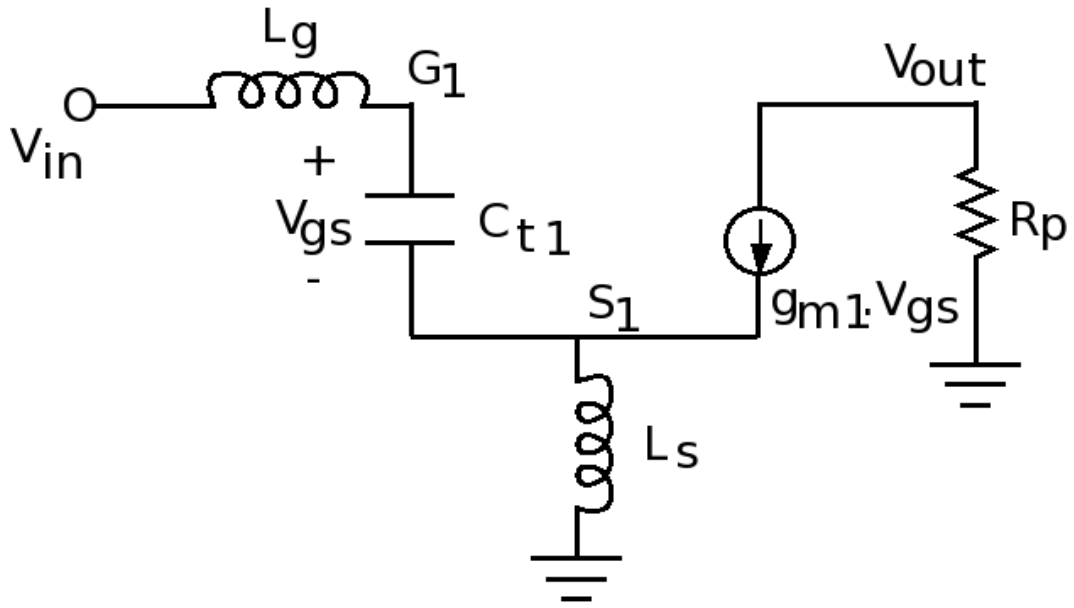


Figure 2.3: Simplified small signal model of the proposed LNA.

By default, the design starts to operate at 2.4 GHz when V_c in Fig. 2.2 is set to 0 V. Switches S1, S2 and S3 are OFF. Capacitors C_1 , C_{tank2} and transistors M2 and M2C are floating. The simplified small signal equivalent model is shown in Fig. 2.3, where $C_{t1} = C_1 + C_{gs1}$ and R_p is the equivalent output resistance at resonance. As the LNA input impedance is fixed, the design procedure is adopted from the well-known input matching

technique [24]. The input impedance at the higher operating frequency ω_H can be expressed without much loss of generality by (2.2). The gate resistance is neglected to simplify the analysis.

The input impedance in Fig. 2.3 takes the form of a series-resonant network

$$Z_{in,H} = \frac{(g_{m1})L_s}{C_1 + C_{gs1}} + j \left[\omega_H(L_s + L_g) - \frac{1}{\omega_H(C_1 + C_{gs1})} \right] \quad (2.2)$$

To provide a resistive or real input impedance of 50 Ω , the imaginary part in (2.2) must be set equal to zero as (2.3) at the higher band operating angular frequency ω_H .

$$\omega_H(L_s + L_g) + \frac{1}{\omega_H(C_1 + C_{gs1})} = 0 \quad (2.3)$$

$$\omega_H = \frac{1}{\sqrt{(L_s + L_g)(C_1 + C_{gs1})}} = \frac{1}{\sqrt{L_t C_t}} \quad (2.4)$$

where,

$$L_t = L_g + L_s \quad (2.5)$$

$$C_{t1} = C_1 + C_{gs1} \quad (2.6)$$

$$C_{gs1} = \frac{2}{3} C_{ox} W_{opt} L \quad (2.7)$$

$$g_{m1} = \frac{2I_D}{V_{ov}} \quad (2.8)$$

$$Z_{in,H} = \frac{(g_{m1})L_s}{C_1 + C_{gs1}} = \frac{(g_{m1})L_s}{C_{t1}} = 50\Omega \quad (2.9)$$

The power constrained optimized width for M1 can be estimated in (2.10) [25] [22].

$$W_{opt} \approx \frac{1}{3\omega_H L C_{ox} R_s} \quad (2.10)$$

The transistor M1 length, L is chosen to be the minimum possible channel length to get a minimum noise figure [22]. C_{ox} is the gate oxide capacitance per unit area. The real impedance is set equal to 50Ω as indicated in (2.9) by carefully choosing the related values as follows. Once the W_{opt} , power constrained transistor width is chosen, the total gate source capacitance C_{gs1} and the transconductance g_{m1} are found. The degeneration inductance L_s can be obtained from bond wire as it is unpreventable in packaging. The design assumes a typical value for L_s in the order of 0.5 to 1 nH [6]. Now C_1 and L_g can be found from (2.9) and (2.16).

$$\omega_H = \frac{1}{\sqrt{(L_D)(C_{tank1} + C_{LOAD})}} \quad (2.11)$$

The center frequency of the output LC tank circuit is given by (2.11). In this mode, L_D is resonated with C_{tank1} , C_{LOAD} and the parasitic capacitance present at the output node. C_{LOAD} effectively represents the total capacitance of the load. C_{tank1} is chosen to get an additional degree of freedom for tuning the design to operate at the required frequency. Optimum value for L_D is chosen to meet the minimum area constraint. Therefore, in this

case the parasitic resistance R_p of the inductor decreases, implying a reduction in the LNA gain. The gain of the circuit is given by (2.12) [9]

$$gain = (g_{m1})QR_p \quad (2.12)$$

Where Q is the quality factor of the input series resonant circuit formed by C_{t1} , L_g and L_s shown in Fig. 2.3. R_p is the parasitic resistance of the inductor, g_{m1} is the transconductance of transistor M_1

2.3.3 Design Operation at Lower Band (1.575 GHz) Mode

For the lower band selection V_c is set to V_{DD} . The simplified small signal equivalent model is shown in Fig. 2.4 Switches S1, S2 and S3 are turned ON. Capacitors C_{tank2} and C_2 , transistors M2 and M2C are enabled to shift the frequency of operation. The input impedance at this lower operating angular frequency ω_L gets transformed from (2.2) to (2.13). Also (2.4), (2.9) and (2.11) now become (2.15), (2.17) and (2.18), respectively.

$$Z_{in,L} = \frac{(g_{m1} + g_{m2})L_s}{C_t + C_2 + C_{gs2}} + j \left[\omega_L(L_t) - \frac{1}{\omega_L(C_{t1} + C_2 + C_{gs2})} \right] \quad (2.13)$$

where,

$$L_t = L_g + L_s \quad (2.14)$$

$$\omega_L = \frac{1}{\sqrt{L_t(C_{t2})}} \quad (2.15)$$

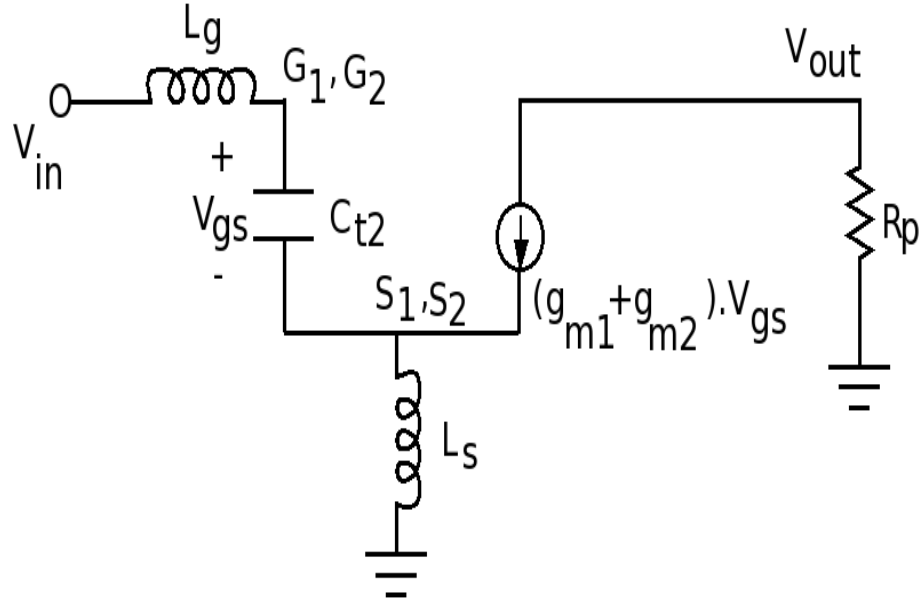


Figure 2.4: Simplified small signal model.

$$C_{t2} = C_{t1} + C_2 + C_{gs2} \quad (2.16)$$

$$Z_{in,L} = \frac{(g_{m1} + g_{m2})L_s}{C_{t2}} = 50\Omega \quad (2.17)$$

$$\omega_L = \frac{1}{\sqrt{(L_D)(C_{tank1} + C_{tank2} + C_{LOAD})}} \quad (2.18)$$

$$g_{m2} = K_n W_2 E_{SAT} \quad (2.19)$$

Where, K_n and W_2 in (2.19) are the gain factor and width of the transistor M2, respectively.

And E_{SAT} is the electric field strength [22].

$$C_{gs2} \approx \frac{2}{3} W_2 L C_{ox} \quad (2.20)$$

With (2.13), (2.15), (2.17) and (2.18) as primary governing equations, design approach is as follows. The value of $C_2 + C_{gs2}$ can be obtained from (2.15) as L_t , C_t and ω_L are known values. Therefore, the required additional transconductance g_{m2} in (2.17) can be obtained. However, g_{m2} found by (2.17) can also be expressed as (2.19). From (2.19), width W_2 of the transistor M2 can be found. Using the width W_2 , C_{gs2} can be obtained by (2.20). As C_{gs2} is obtained, C_2 can be determined using (2.15).

The beauty of the design lies in the following specific conclusions. The total capacitance at the input end increases from C_{t1} to $C_{t1} + C_2 + C_{gs2}$ in (2.16). Careful examination of (2.17) tells that the transconductance also gets increased by the amount g_{m2} . Thereby, giving the flexibility to set the real part of $Z_{in,L}$ to 50Ω . The MOS switches S1, S2 and S3 are optimized such that they do not effect the noise figure and other performance parameters too much [17].

In this mode, C_{tank2} is obtained accordingly from (2.18) to change the output operating frequency. The frequency of operation is switched from high to low (2.4 GHz to 1.5 GHz). The design is optimized at 1.575 GHz.

2.4 ADS RFIC Dynamic Dink

RFIC analysis is relatively easier using Advanced Design System (ADS). The first step is to create a schematic of the reconfigurable LNA in Cadence. The next step is to create a symbol and then export it to ADS via RFIC Dynamic link. Once the symbol is transferred the process model files should be added.

Flow chart of the overall simulation flow using Dynamic link is shown in the following Fig. 2.5

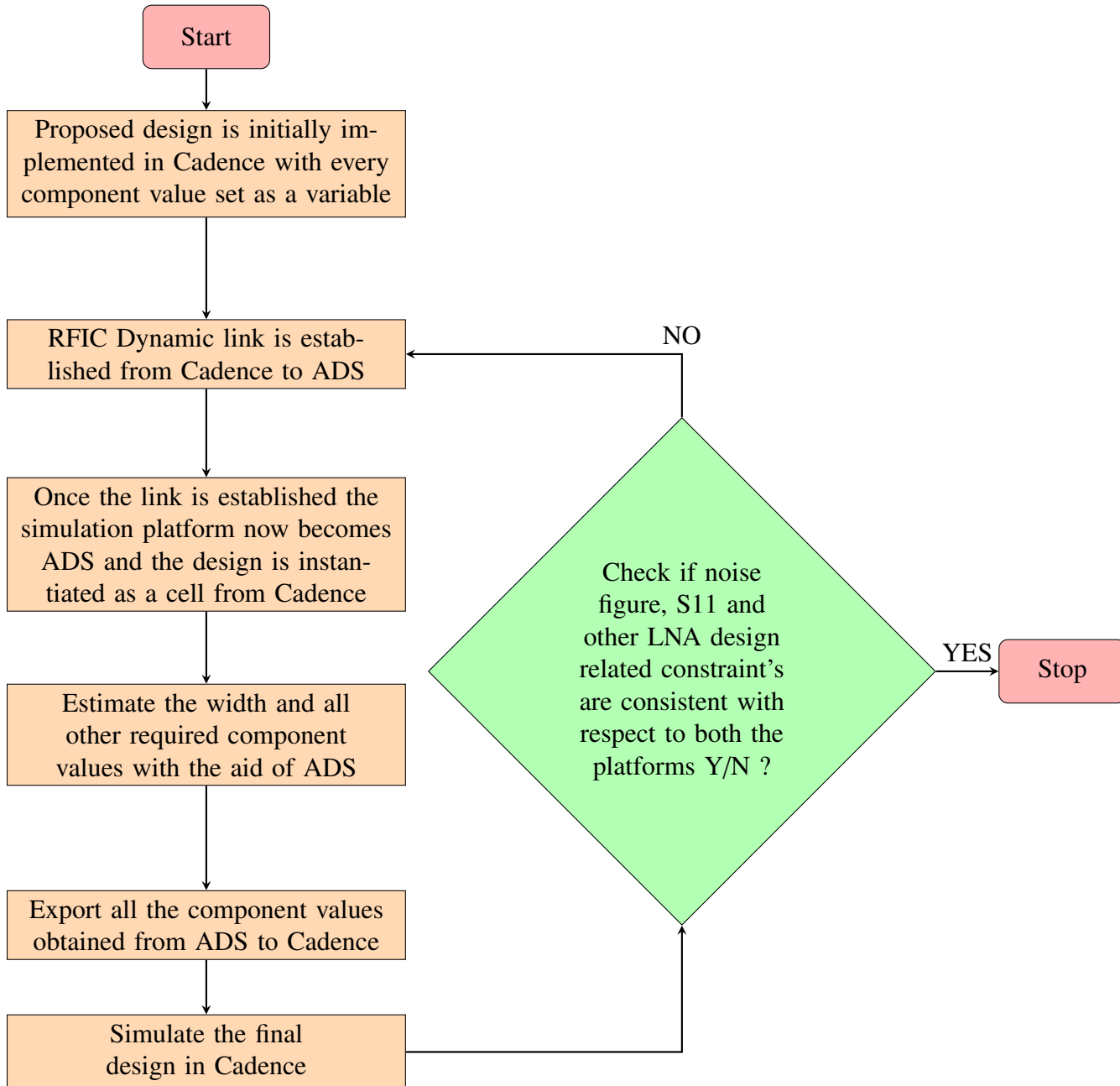


Figure 2.5: Flow chart of the overall simulation flow using Dynamic link.

The simulation sources and all other ports are then used from ADS and then the design is optimized to obtain the component values for all the components as shown in the Fig. 2.6.

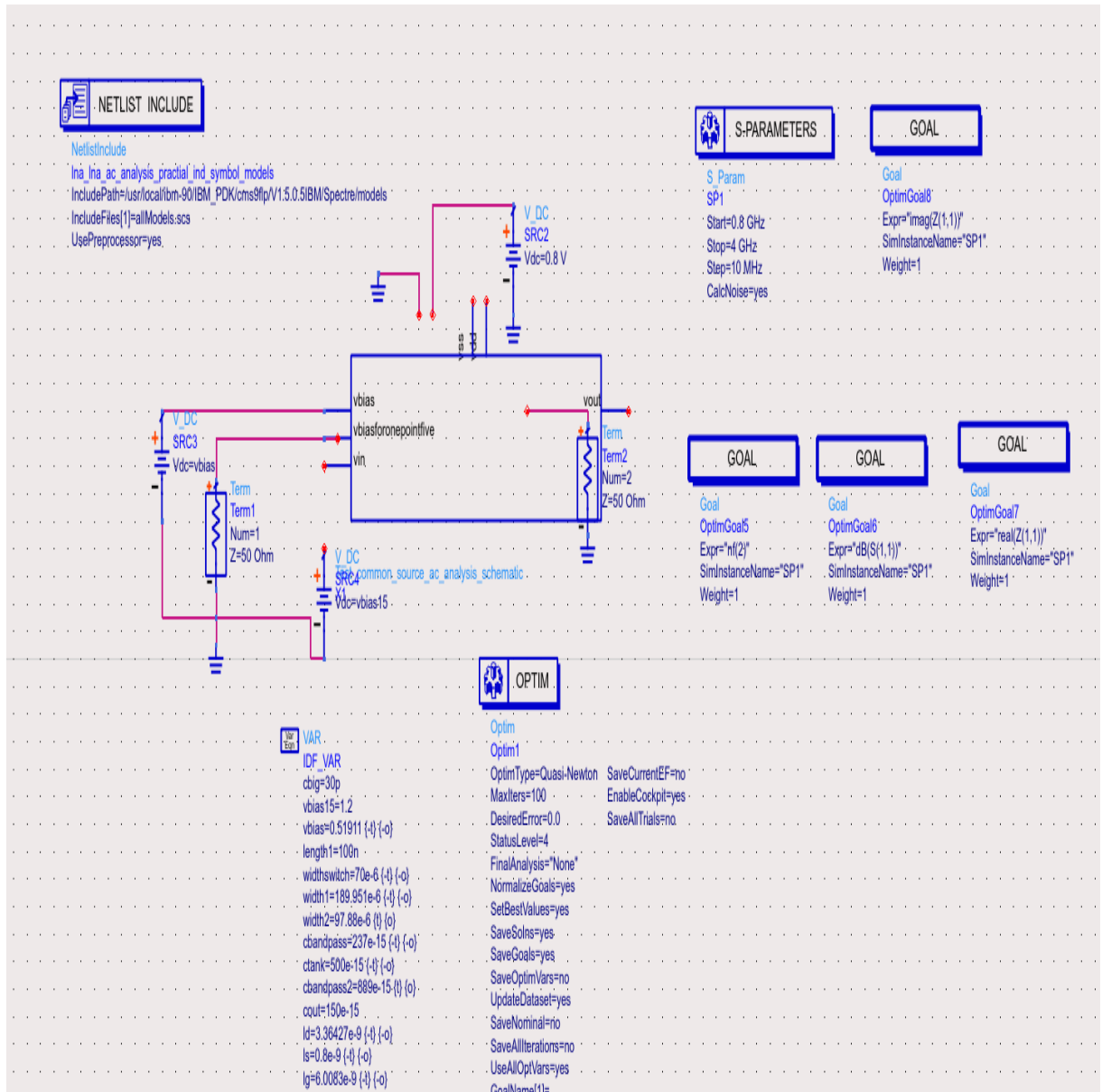


Figure 2.6: ADS simulation set up using LNA symbol exported from Cadence via RFIC Dynamic link.

Once the component values are obtained in ADS with the desired simulation results, the design is simulated again in Cadence to check for discrepancies, if any. But the simulation results obtained using ADS tools are consistent with the Cadence tools. The integration

of both these tools (ADS, CADENCE) is based on Inter Process Communication. This provides with many dynamic capabilities such as, RF simulation and analysis via ADS while maintaining the transistor-level hierarchy information in the Cadence database itself [26].

The final design schematic implemented in 90nm CMOS technology is shown in Fig. 2.7.

Note: Body connections for the MOSFET's was not shown in the figure for better clarity of the design.

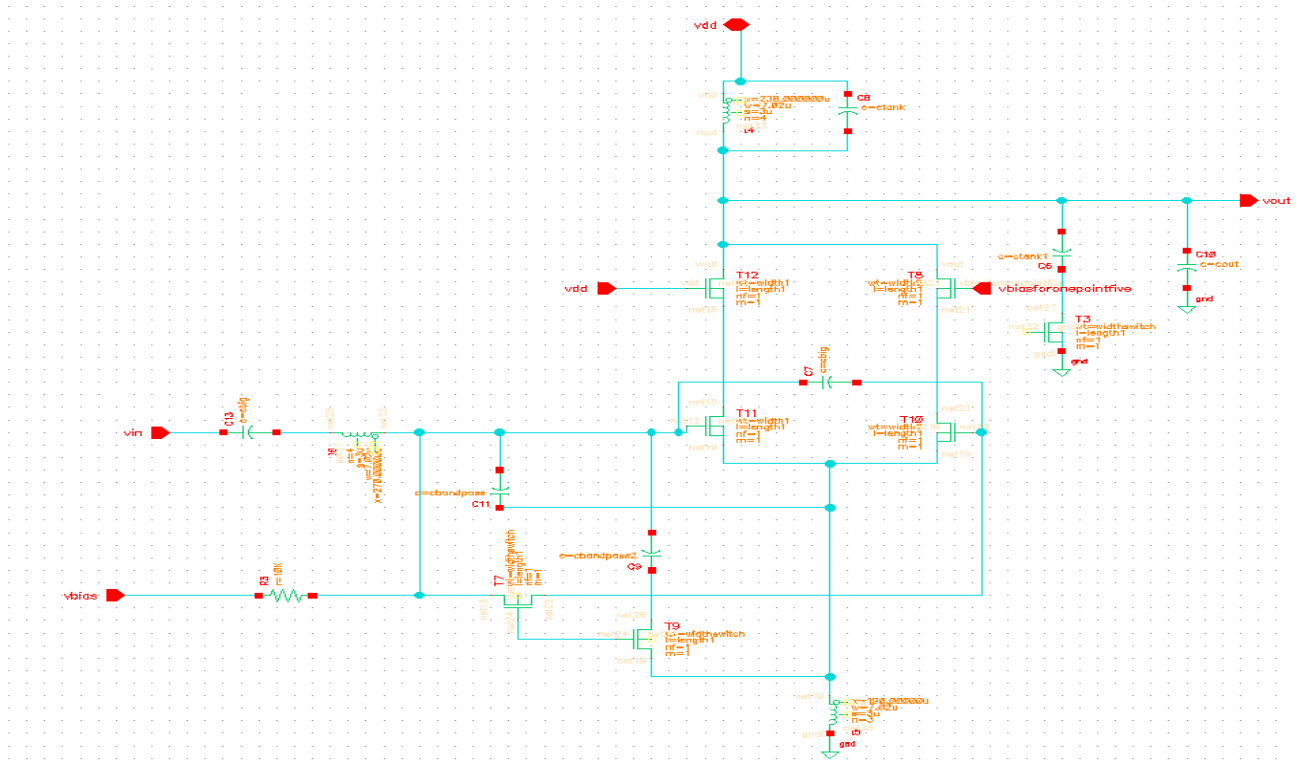


Figure 2.7: Final implemented LNA design in Cadence 90nm CMOS Technology.

2.5 Simulation Results of Reconfigurable LNA

The design simulations were carried out using Spectre RF from Cadence design suite. As power dissipation and area are chosen to be the primary constraints of the design. Width of the transistors was limited by (2.10). Therefore, transconductance obtained was relatively small which limited the power gain. Also optimum value for L_D is chosen to meet the minimum area constraint. Therefore, in this case the parallel parasitic resistance R_p decreases, again implying a reduction in the output power or equivalently in the LNA power gain. Fig. (2.8) represents the Bode plot of the power gain simulated for both configurations. The design exhibits a power gain of 11.2 dB and 12.4 dB at lower and upper bands, respectively. The -3 dB bandwidth is 561 MHz and 516 MHz for lower and upper bands, respectively.

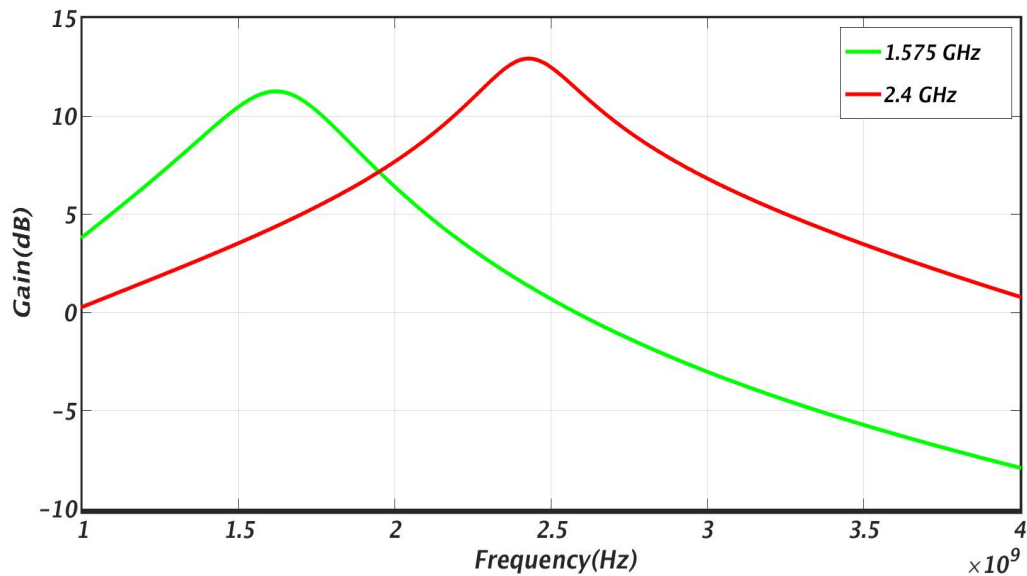


Figure 2.8: Simulated gain over two frequencies 1.575 GHz and 2.4 GHz

Plots of input return loss (S11) for both bands are shown in Fig. 2.9. The design exhibits input power loss of -25.26 dB and -21.4 dB at lower and upper bands, respectively. S11 remained well below -15 dB for entire -3 dB bandwidth for both standards.

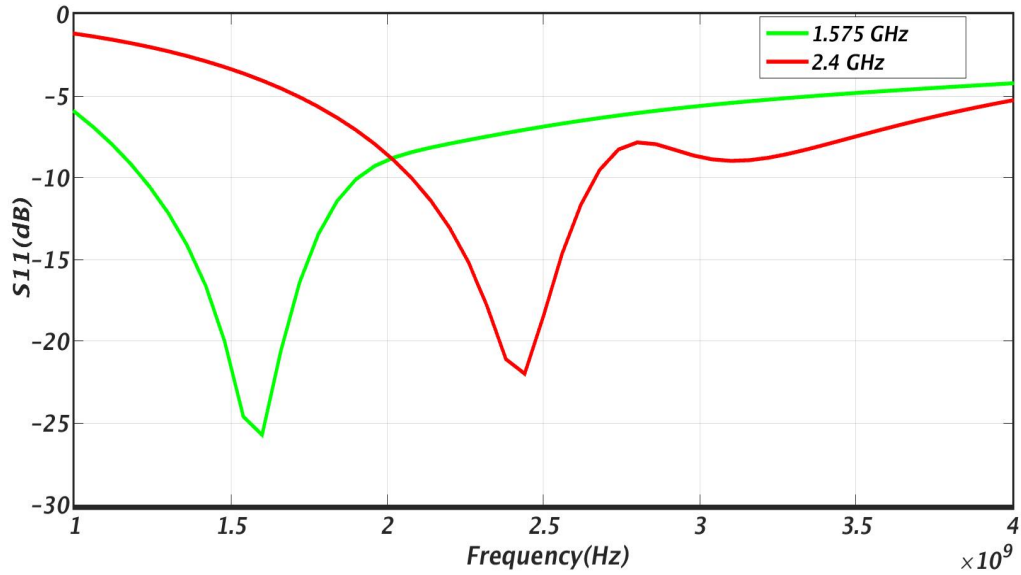


Figure 2.9: Simulated S11 over two frequencies 1.575 GHz and 2.4 GHz

The simulated plot in Fig. 2.10 shows that the lower band achieves 3.4 dB of noise figure and upper band of 2.9 dB noise figure. The power consumption turned out to be 8.9

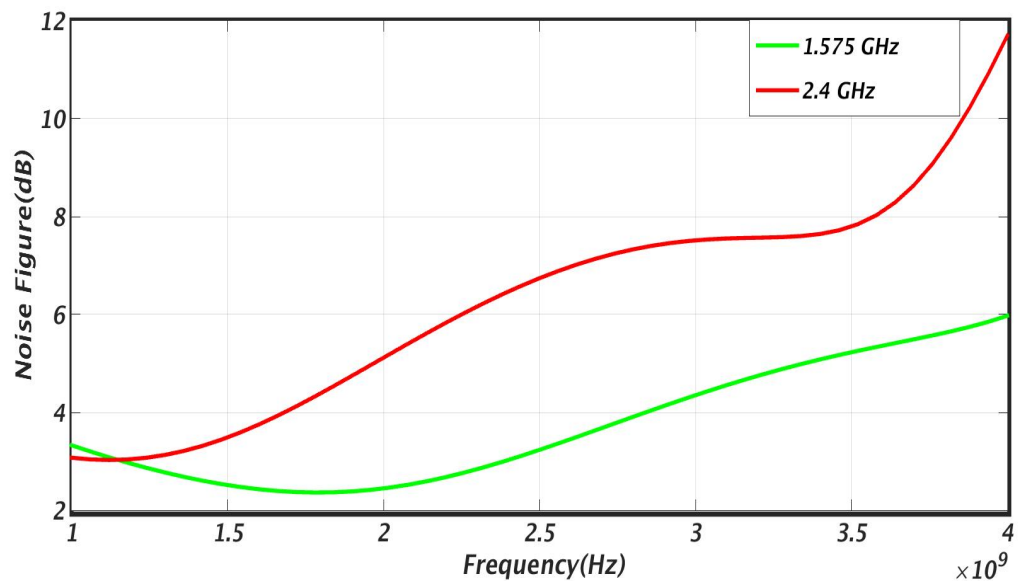


Figure 2.10: Simulated Noise Figure over two frequencies 1.575 GHz and 2.4 GHz

mW and 4.68 mW for a 1.2 V power supply for lower and higher frequency bands, respectively. Third-order input intercept points were obtained by considering 10 MHz signal as

Table 2.1: COMPARISON BETWEEN THE PROPOSED DESIGN AND OTHER RELATED DESIGNS

Ref	This work	Ref. [11]	Ref. [12]	Ref. [13]
Tech	90 nm	0.18 μm	90 nm	0.18 μm
FREQ(GHz)	1.575 2.4	1.575 2.4	2.04 2.44 2.44	0.9 2
Gain(dB)	11.2 12.4	10.47 11.17	>20.6* >16.2* >22.3*	12.9 12.4
S11(dB)	-25.26 -21.4	N/A N/A	<-7.9* <-10* <-12.4*	-14.5 -17.2
NF(dB)	3.4 2.9	3.21 3.21	1.73 1.77 1.64	2.55 2.3
IIP3(dBm)	-3.12 -2.137	1.62 1.16	-0.15 -0.6 -3.3	N/A N/A
Supply(V)	1.2	1.8	1	N/A
Pdc(mW)	8.9 4.68	33.3	28.5 25.3 30.5	26.5 18.8

* Measured at the operating bandwidth.

interferer for both bands. IIP3 of -3.12 dBm and -2.137 dBm was noted for lower and upper bands. The performance of the dual-band LNA is summarized and compared with other related works in Table 2.1. Which shows the proposed dual-band LNA is very competitive in all aspects, especially power consumption.

A Simple and Efficient SPICE Based Design Methodology for LNA Design

3.1 Introduction

A simple design methodology for designing a LNA is developed by which size of MOS transistors and passive components can be computed orderly. A conventional cascode LNA structure in Fig. 3.1 is used to demonstrate the idea. The proposed methodology also provides a systematic approach to contemplate the trade-offs involved in the design of the LNA block. The most principal recognizable trade-off exists between LNA power consumption and noise figure (NF). Although noise figure being the primary consideration in an LNA design, for some applications it is not recommended to have a very low noise figure at the cost of very high power dissipation. For such applications, an approach which aids in wisely choosing the component values is presented.

The primary advantage of the proposed methodology is simple and efficient to design compared to other existing design methods [27] [28]. But this design neglects the consideration of the gate induced noise based on the fact that it is very minimal at the operating

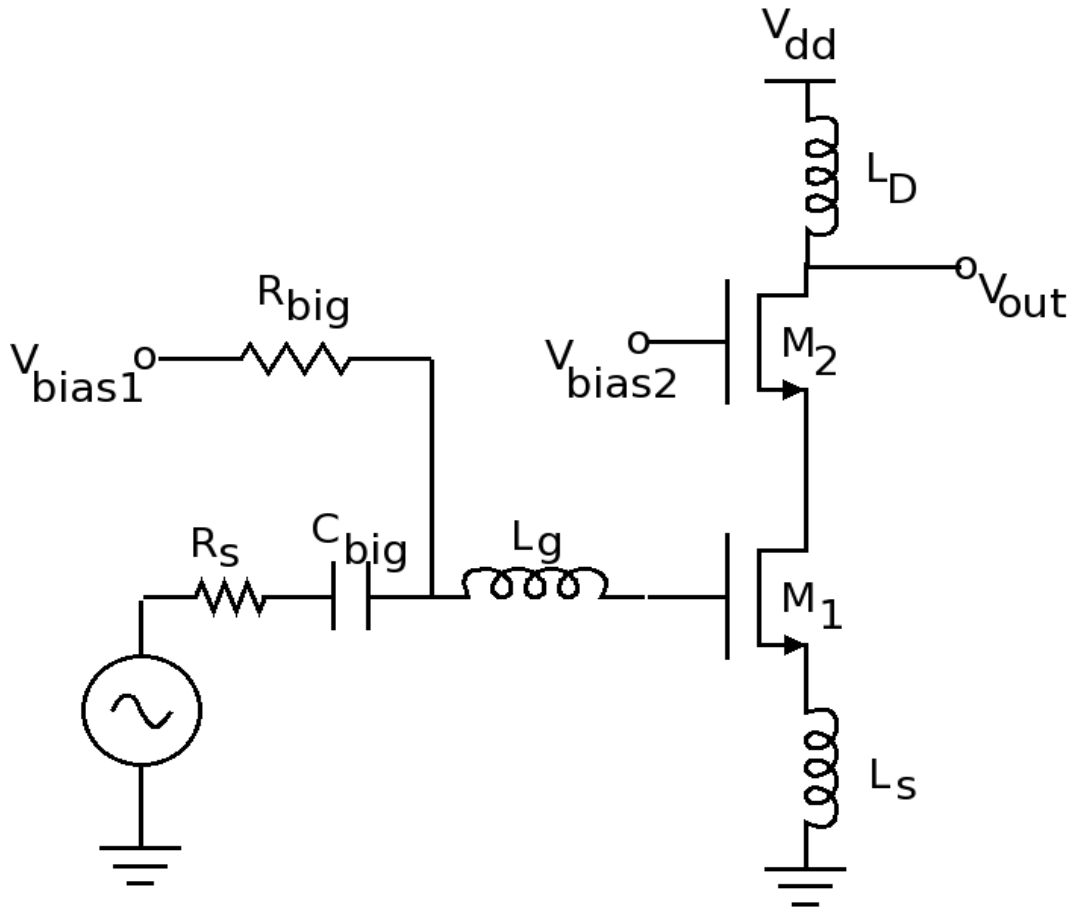


Figure 3.1: Simplified Schematic of the conventional LNA.

frequencies considered.

3.2 Proposed Design Methodology of LNA

3.2.1 Choice of operation region

CMOS devices in saturation can be utilized in weak, moderate, or strong inversion. Each region of operation exhibits different expressions for transconductance (g_m) and drain current (I_d) as a function of V_{gs} . Weak inversion offers large power efficiency (g_m/I_D) but slow

speed or low operating frequency, and strong inversion offers fast speed or high operating frequency but lower g_m/I_d , relatively. Moderate inversion offers the best compromise between achieving reasonable g_m/I_d and reasonable speed [29] [30] [31]. Which region of operation to choose is purely a designer's choice based on the application. Best suitable region of operation can be elegantly chosen if one can employ directly SPICE values to calculate the critical design parameters due to the complexity of the device model in encompassing these three operating regions. The proposed design strategy follows a methodology in which LNA oriented performance metrics are directly generated with the help of SPICE based plots using Cadence EAD tools.

3.2.2 Selection of design variable and design flow chart

For a LNA design, the key measured parameter is noise figure given by expression (3.1) for the chosen configuration [7].

$$F = 1 + \frac{R_{Lg}}{R_s} + \frac{R_g}{R_s} + \gamma g_{do} R_s \left(\frac{\omega_o}{\omega_T} \right)^2 \quad (3.1)$$

Where, gate resistance of the MOSFET (M1) from Fig. 3.1, is represented by R_g , the input source resistance is represented by R_s and R_{Lg} is the parasitic resistance of the inductor L_g . Where γ is around 2/3 for long channel. Note γ value is higher than that in sub-micron technology [11].

It is clearly shown in expression (3.1) that ω_T , angular transit frequency, is a critical design metric for noise figure. To obtain acceptable noise levels, choose a cut off frequency

which is 10 times that of the operating frequency ($f_t=10*f_o$) [29]. f_t is defined as (3.2) [9].

$$f_t = \frac{g_m}{2\pi(2 * C_{gd} + C_{gs})} \quad (3.2)$$

Here, C_{gd} is the gate to drain and C_{gs} is the gate to source input capacitance of M1 in Fig. 3.1. And $2*cgd$ is the Miller equivalent gate to drain capacitance for a cascode configuration common source amplifier with gain of -1 [8].

The flow chart shown in Fig. 3.2 depicts the overall design flow.

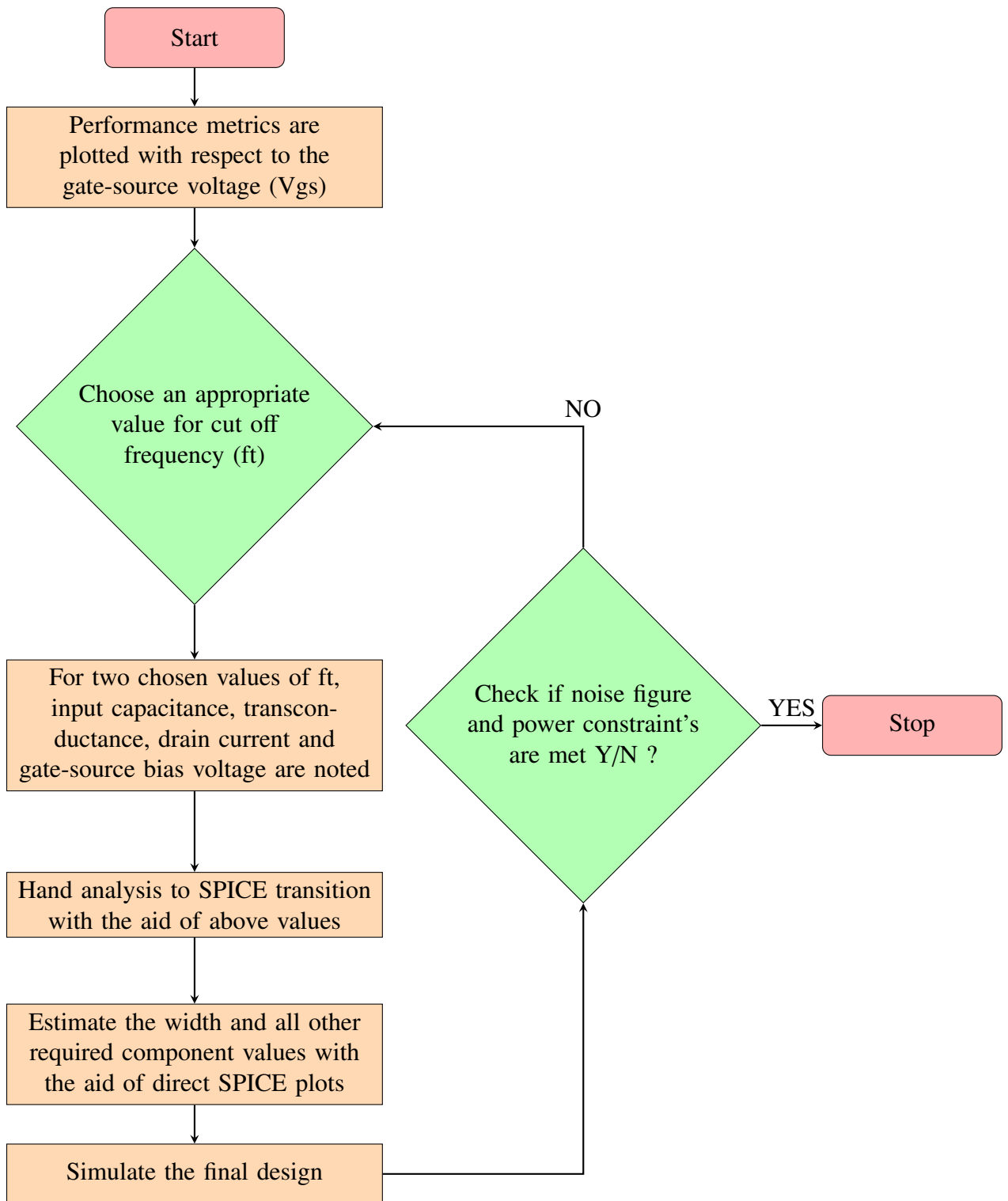


Figure 3.2: Flow chart of the overall design flow.

As shown in Fig. 3.3 the proposed strategy of designing the LNA follows a methodology in which LNA oriented performance metrics such as transit frequency (f_t), the total effective input capacitance ($c_{gs} + 2 * c_{gd}$) observed by the input signal, the transconductance (g_m) and the drain current (I_D) are plotted with respect to the gate-source voltage (V_{gs}) as in Fig. 3.3.

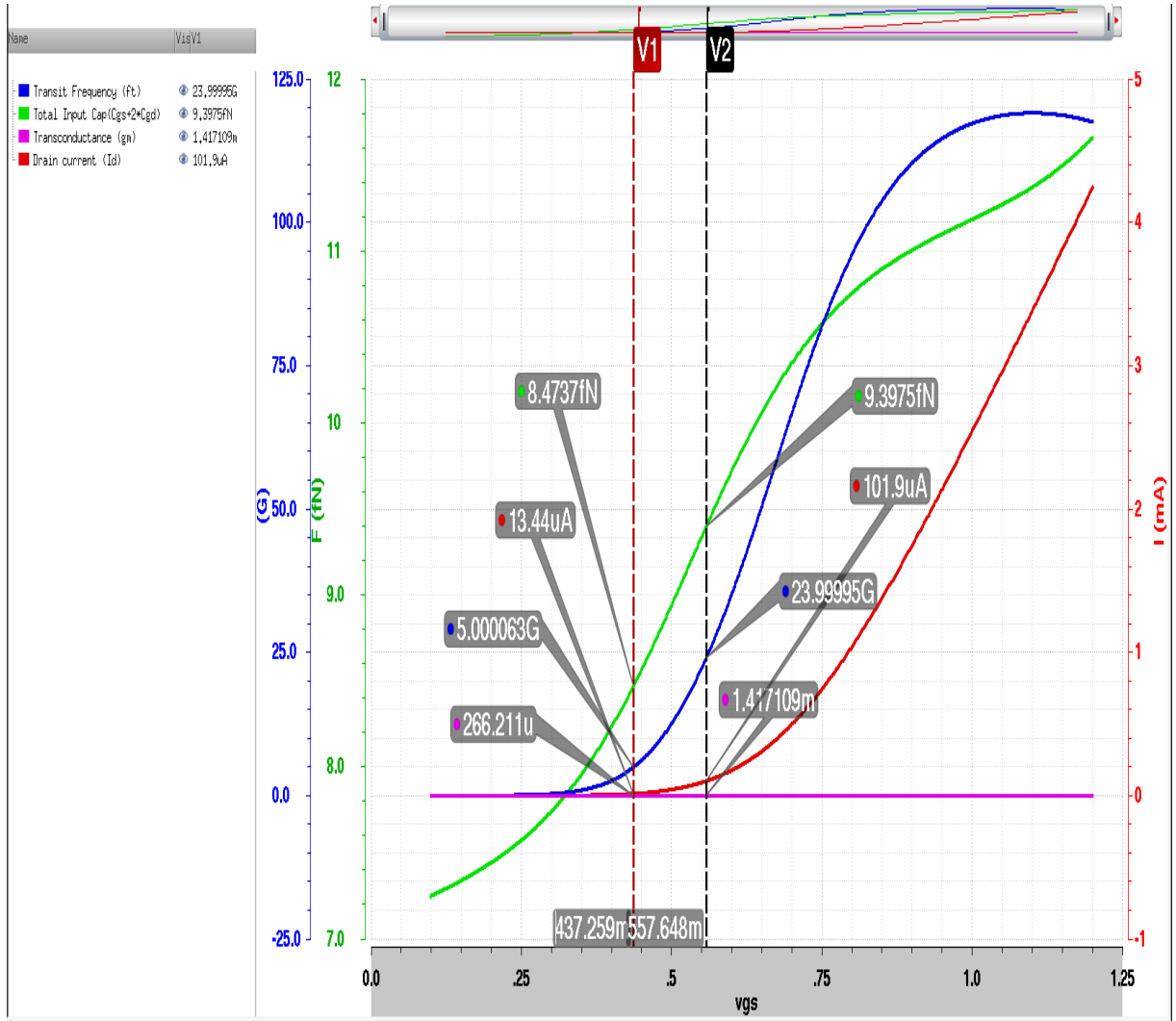


Figure 3.3: Design metrics plotted with respect to V_{gs}

These plots in Fig. 3.3 are generated once and then used throughout the design process. As these plots are technology specific and are direct result of the Spice model files

there should not exist any discrepancy between calculated and simulated values. The advantage of this design metrics plot based methodology is that it aids in transition from hand analysis to SPICE without incorporating uncertainties [29]. Primary reason being the incorporation of the direct relevant simulation data into the design process.

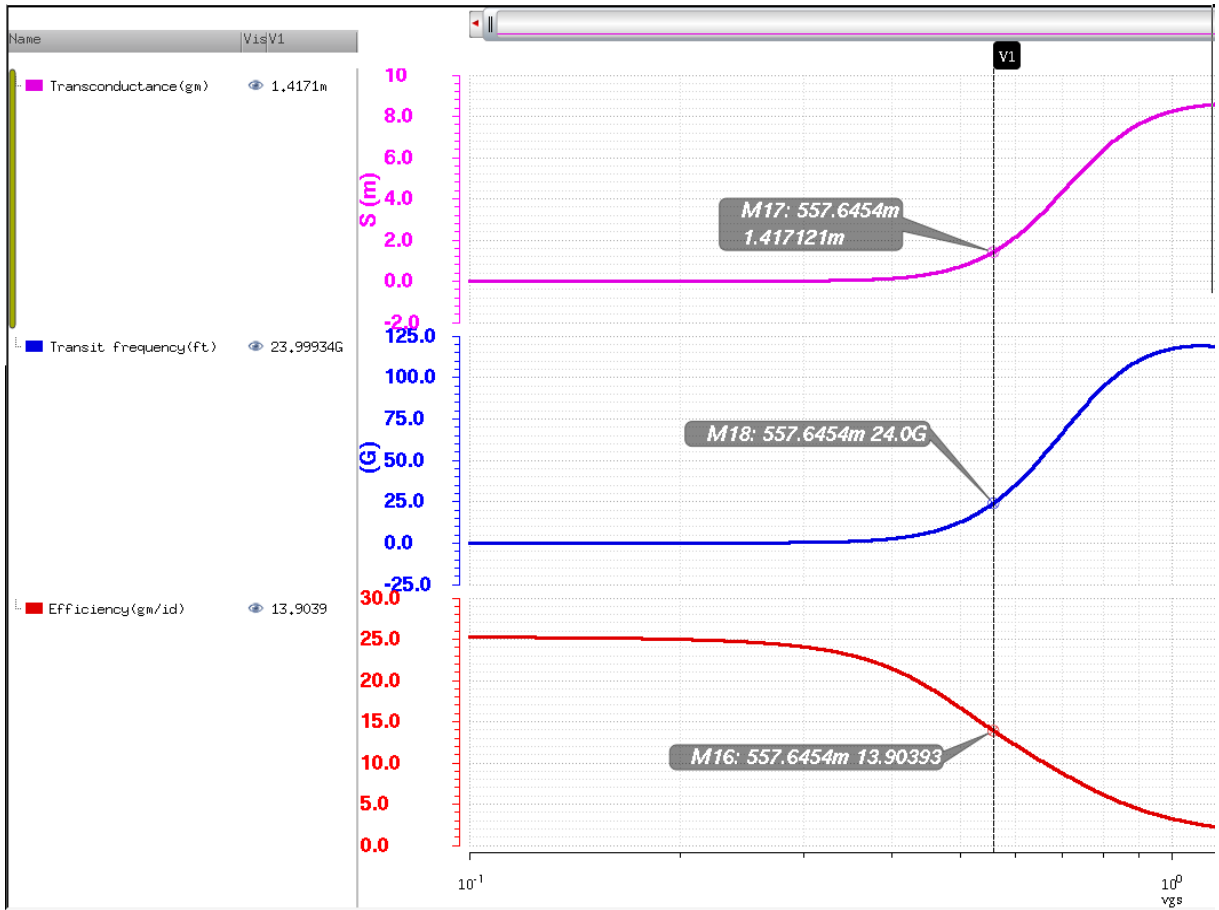


Figure 3.4: Power efficiency(g_m/I_D), g_m and f_t (speed) Profile with respect to V_{gs}

It is clear from the plots that f_t increases with the increase in gate to source voltage which can result in a minimal noise figure. But high f_t also demands more transconductance (g_m). Power Efficiency(g_m/I_D), g_m and f_t (speed) Profile can be observed in Fig. 3.4. It can be seen that high f_t values have low power efficiency g_m/I_D , i.e g_m resulting from a unit bias current invested is very poor. As the designer is aware of the operating frequency ω_o ,

its relatively easy to choose an appropriate ω_T which results in an acceptable noise figure basing on the design specifications.

The basic idea is to design the LNA which can exhibit good transconductance or power efficiency (g_m/ID) without consuming much bias current (ID) and without introducing large C_{gs} , so that it has sufficient transit frequency (f_t) as already discussed.

In the proposed design methodology ' f_t ' is the critical parameter used for choosing the width of the transistors. Recall the noise figure is directly related to f_t given by (3.1). f_t is the critical parameter that let's us trade power efficiency (g_m/ID) for noise performance. So the value for f_t is to be chosen with careful consideration.

3.2.3 Proposed design procedure exmple

SPECIFICATIONS

- Power= 6 mW
- VDD= 1.2 V
- Operating Frequency f_o = 2.4 GHz
- Noise Figure \leq 3 dB

Design step 1:

The input impedance can be readily analyzed from Fig. 3.5 as (3.3). The input circuit takes the form of series resonant circuit and the input impedance is purely real at the

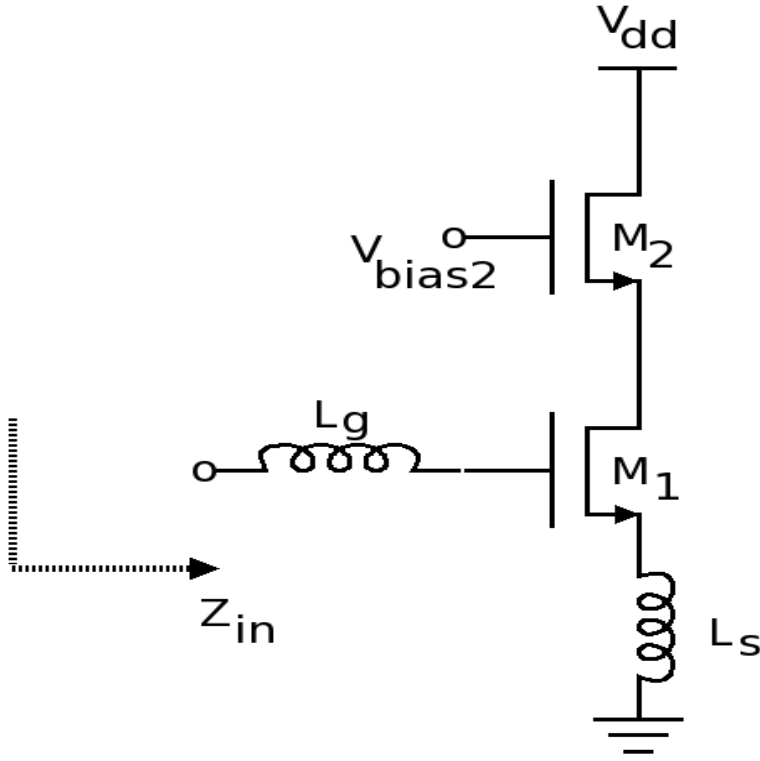


Figure 3.5: Schematic of the conventional LNA input stage.

resonant frequency.

$$Z_{in} = \frac{(g_m)L_s}{2 * C_{gd} + C_{gs}} + j \left[\omega_o(L_s + L_g) - \frac{1}{\omega_o(C_{gd} + C_{gs})} \right] \quad (3.3)$$

To provide a resistive or real input impedance of 50Ω , the imaginary part of the expression (3.3) must be set equal to zero as (3.4) at the operating angular frequency ω_o .

$$\omega_o(L_s + L_g) + \frac{1}{\omega_o(2 * C_{gd} + C_{gs})} = 0 \quad (3.4)$$

Design step 2:

The design starts following the provided specifications by constraining DC bias cur-

rent to 5 mA to limit the power dissipation to 6 mW. Initially the following design metrics are plotted with respect to gate-source voltage, V_{gs} as in Fig. 3.3:

- Transit or Cut off frequency ω_t ,

$$\omega_t = \frac{g_m}{(2 * C_{gd} + C_{gs})} \quad (3.5)$$

- Transconductance g_m ,
- Total effective input capacitance ($2 * C_{gd} + C_{gs}$)
- Drain current I_d .

width is chosen to be 10 μm and length is chosen to be the minimum (100nm) for all the parameters.

Note: Design assumes that following are the values for a single finger and the width of the single finger is 10 μm as mentioned above.

From Fig. 3.3. It can be noticed that we have the following values for the above considered design metrics.

The design methodology starts with setting the angular transit frequency ω_t ($\omega = 2\pi f$) equal to 10 times the ω_o as already discussed above, which will satisfy the noise requirements, optimally.

$$\omega_t = 10\omega_o$$

$$\omega_o = 2\pi 2.4 \text{ GHz}$$

Design Metrics	Transit Frequency(f_t)	
	$f_t=5$ GHz	$f_t=24$ GHz
Input capacitance ($C_{gs} + 2 * C_{gd}$) _f	8.47 fF	9.3975 fF
Transconductance (g_m) _f	266.21 uS	1.41 mS
Drain current (I_{d_f})	13.44 uA	101.9 uA
Gate-source bias voltage (V _{gs})	437.25 mV	557.64 mV
Source inductance (L_s)	331.57 pH	331.57 pH
gate inductance (L_g)	10.35 nH	9.2 nV
width of M1	435 um	490 um

Table 3.1: Design metrics at the lower (5 GHz) and higher (24 GHz) transit frequencies

$$\omega_t = 2\pi 24 \text{ GHz}$$

$$Z_{in} = \frac{(g_m)L_s}{(2 * C_{gd} + C_{gs})} = (\omega_t)L_s = 50\Omega \quad (3.6)$$

$$L_s = \frac{50\Omega}{(\omega_t)} = 331.57 \text{ pH} \quad (3.7)$$

This gives the value of L_s as the ω_t is fixed for 24 GHz

Design step 3:

As the power is a principal constraint the total width which allows the required amount of dc bias current can be calculated as follows. For instance here, the LNA is allowed to conduct only 5 mA of current then the scaling factor (n) for obtaining total width, which is referred as number of fingers from now on can be obtained as follows:

$$\text{number of fingers}(n) = \frac{5\text{mA}}{I_{D_f}} = \frac{5\text{mA}}{13.44\text{uA}} = 49 \quad (3.8)$$

The total width required by the device (M1) can be easily obtained now by the follow-

ing expression. As ID_f is the current conducted in 10 um width.

$$width = number \text{ of fingers}(n) * 10um = 490um \quad (3.9)$$

In this configuration the input resonance frequency is set by the gate inductance L_g , source inductance L_s and the total Input gate capacitance ($C_{gs} + 2 * C_{gd}$). The total Input gate capacitance ($C_{gs} + 2 * C_{gd}$) can be calculated as follows.

$$(cgs + 2 * cgd) = number \text{ of fingers}(n) * (cgs + 2 * cgd)_f = 461.2fF \quad (3.10)$$

Once the total equivalent input gate capacitance is calculated the total inductance L_t which gives the required tuning at resonance can be obtained as follows.

$$\omega_o = \frac{1}{\sqrt{(L_t)(2 * C_{gd} + C_{gs})}} = \frac{1}{\sqrt{(L_s + L_g)(2 * C_{gd} + C_{gs})}} = 2\pi 2.4GHz. \quad (3.11)$$

Here, $L_t = L_g + L_s$

$$L_t = \frac{1}{(2 * C_{gd} + C_{gs})(2\pi 2.4GHz)^2} = 9.53nH \quad (3.12)$$

$$L_g = L_t - L_s = 9.2nH \quad (3.13)$$

Design step 4:

The output inductance value for L_D can be chosen by calculating the total capacitance

value at the output node as in (3.15)

$$\omega_L = \frac{1}{\sqrt{(L_D)(C_{parasitics} + C_{LOAD})}} \quad (3.14)$$

$$L_D = \frac{1}{(C_{parasitics} + C_{LOAD})(2\pi 2.4GHz)^2} \quad (3.15)$$

Choosing an appropriate value for f_i is very critical in this methodology which will be clearly evident now. similar design approach is followed and f_i is chosen to be 5 GHz instead of 24 GHz. It is obvious from the TABLE. 3.1 that the drain current is scaled almost by a factor of ten resulting in a drastic decrease in the DC power dissipation . By allowing 1 dB increase in the noise figure power is decreased almost by a factor of 10. If the noise figure specification is clearly known prior to the designer then the f_i needed to maintain that noise figure can be easily obtained from the expression (3.15) and rest of the design follows similar approach detailed above. Choosing a large f_i than what is needed means simply to dissipate more power than what is needed. This design principle is aimed at optimally choosing the required f_i needed to meet the design specifications.

3.3 Simulation Results of LNA

The design simulations were carried out using Spectre RF from Cadence design suite. The design exhibits a power gain of 26 dB and 12.4 dB at lower and upper f_i , respectively. The -3 dB bandwidth spans to 500 MHz and 516 MHz for the lower (5 GHz) and higher (24 GHz) transit frequencies, respectively.

Plots of input return loss (S11) for both lower and upper f_t are shown in Fig. 3.6 and Fig. 3.7. The design exhibits input power loss of -26.63 dB and -32.57 dB at the lower (5 GHz) and higher (24 GHz) transit frequencies, respectively. S11 remained well below -26 dB for entire -3 dB bandwidth for both standards.

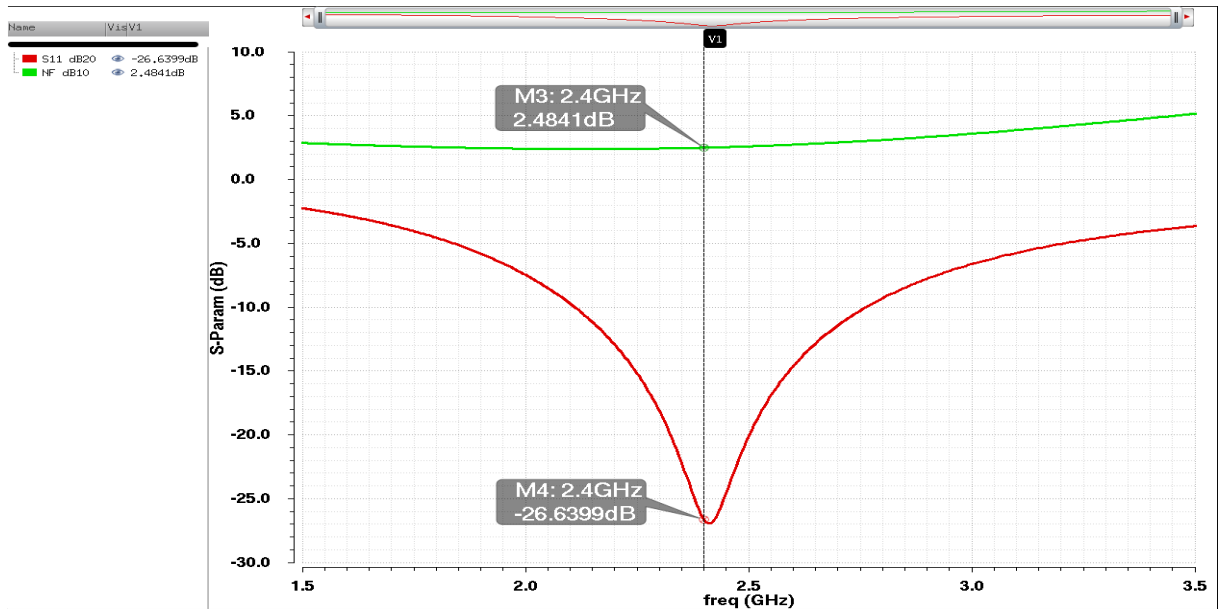


Figure 3.6: Noise Figure and s11 plot for lower ' f_t '.

The simulated plots in Fig. 3.6 and Fig. 3.7 show that the lower f_t design achieves 2.48 dB of noise figure and higher f_t of 1.56 dB noise figure.

The power consumption turned out to be 600 uW and 6 mW for a 1.2 V power supply for lower and higher f_t designs, respectively. The 1 dB compression point of -3.12 dBm and -2.137 dBm was noted for the lower (5 GHz) and higher (24 GHz) transit frequencies, respectively.

The performance of both the designs is summarized in TABLE 3.2. Which encompasses the trade off involved between power dissipation and noise figure. Approximately

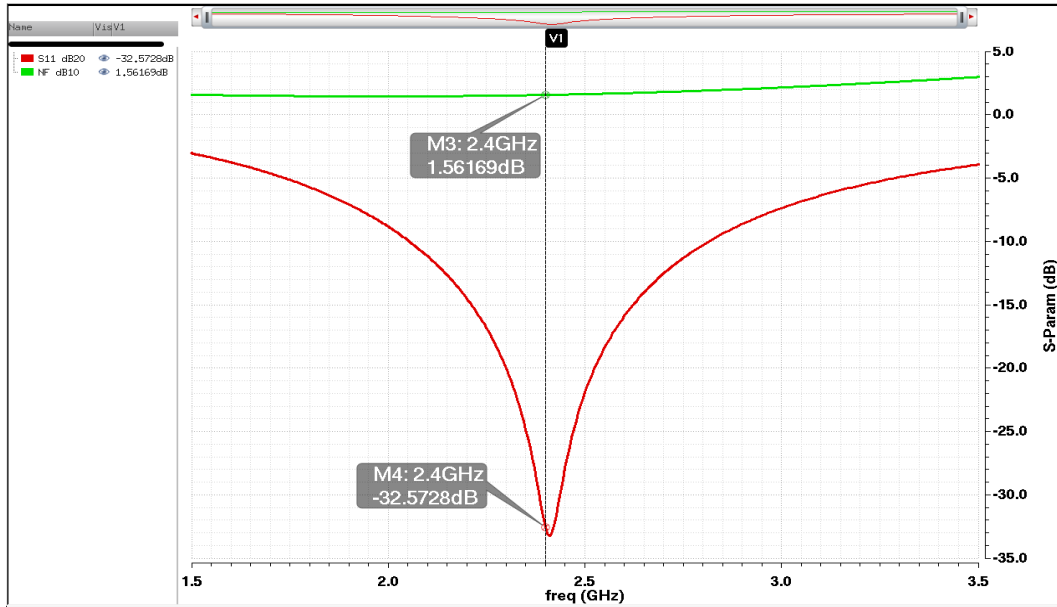


Figure 3.7: Noise Figure and s11 plot for higher ' f_i '.

Performance Characteristics	Transit Frequency(f_i)	
	$f_i=5$ GHz	$f_i=24$ GHz
Input frequency	2.4 GHz	2.4 GHz
Supply voltage	1.2 V	1.2 V
DC power dissipated	600 uW	6 mW
Noise Figure	2.48	1.56
S11	-26.63 dB	-32.57 dB
Gain	20.3 dB	26 dB
1 db compression point	-2.137 dBm	-3 dBm

Table 3.2: Performance Characteristics at the lower (5 GHz) and higher (24 GHz) transit frequencies

1 dB improvement in noise figure demands around 5 mW of power under the given bias conditions. So appropriate choice of the transit frequency basing on the given specification can lead the designer to obtain a optimum design in terms of power dissipation. The design strategy in itself is very simple and gives better insight into the design methodology.

Conclusions and future work

4.1 Conclusions

A reconfigurable dual band LNA was designed to operate in 1.575 GHz and 2.4 GHz frequency bands. This design methodology is straightforward and it can be extended to other standards of operation. Due to the fact that the inductors are reused, the total design area would be relatively minimized as inductors generally requires a large fraction of chip area compared to transistors and capacitors. The LNA presented has the ability to operate in 1.575 GHz and 2.4 GHz frequency bands by simply enabling or disabling the control voltage V_c while avoiding any tuning mechanism at the input stage. Interesting aspect of the design is, the bias voltage V_{Bias} is same for both the transistors. Therefore, it does not need additional bias circuitry except for V_{Bias} .

The reconfigurable dual-band LNA can be tuned to operating frequency of either 1.575 GHz for global positioning system (GPS) or 2.4GHz for WLAN 802.11b standards. The simulated results performed power gain of 11.2 dB and 12.4 dB, and noise figure of 3.4 dB and 2.9 dB, an input return loss(S11) of -25.26 dB and -21.4 dB and a third-order input intercept point of -3.12 dBm and -2.137 dBm and the design dissipates 8.9 mW and 4.68

mW of power at 1.2 V power supply at the two frequency bands 1.575 GHz and 2.4 GHz, respectively.

Also a new approach is proposed for designing the LNA, which can guide the designer in obtaining a low power design with acceptable noise figure along with a good input impedance matching by investing very little design time. This design methodology is straightforward and it can be extended for other designs also. Using the presented approach, the feasibility in designing LNAs has been proven by simulations. The simulated results for the two designs with operating frequency band of 2.4 GHz performed power gain of 26 dB and 20.3 dB, and noise figure of 1.5 dB dB and 2.48 dB, an input return loss (S11) of -32.57 dB and -26.63 dB and the 1 dB compression point of -3.12 dBm and -2.137 dBm and the design dissipates 6 mW and 600 uW of power at 1.2 V power supply at the lower (5 GHz) and higher (24 GHz) transit frequencies, respectively.

The SPICE based design methodology is more intuitively appealing and gives better insight into the design compared to the design technique used in reconfigurable LNA. It involves the designer to directly work with the design based parameters without involving any discrepancy between hand based analysis and simulation results.

4.2 Future work

- With respect to the reconfigurable LNA design, a variable capacitor at the input side can be potentially employed to extend the number of frequency standards.
- In the SPICE based LNA design methodology, a generalized expression could be

developed which gives a direct relationship between the noise figure and the cut-off frequency.

Bibliography

- [1] A 900MHz Low Noise Amplifier with Temperature Compensated Biasing. ProQuest. 2008-01-01. ISBN 9780549667391.
- [2] <http://mwrf.com/mixed-signal-semiconductors/low-cost-front-end-receives-9-ghz>
- [3] <https://en.wikipedia.org/wiki/Scattering-parameters>.
- [4] <http://www.wetterlin.org/sam/SA/Operation/SParameters.pdf>
- [5] <http://www.ee.iitm.ac.in/ani/2013/ee6240/pdf/ee6240-2013-lec15.pdf>
- [6] Razavi, B. (2001). Design of Analog CMOS Integrated Circuits, Mc- Graw Hill.
- [7] Schaeffer, D. K., and Lee, T. H., "A 1.5 V, 1.5 GHz CMOS Low Noise Amplifier," IEEE J. Solid-State Circuits, 32, 745, 1997.
- [8] B. Razavi, RF Microelectronics, Prentice-Hall, 1997.
- [9] T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge, U.K.: Cambridge Univ. Press, 1998, ch. 11.

- [10] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, A physics-based MOSFET noise model for circuit simulators, IEEE Trans. Electron Devices, vol. 37, pp. 1323-1333, May 1990.
- [11] A. A. Abidi, "High-Frequency Noise Measurements on FET's with Small Dimensions," IEEE Trans. on Electron Devices, VOI.ED-33,N0.11, pp.1801-1805, NOV.1986.
- [12] M. El-Nozahi, E. Sanchez-Sinencio, and K. Entesari," A CMOS Low- Noise Amplifier with Reconfigurable Input Matching Network ", IEEE Trans. Microw. Theory Techn., vol. 57, pp. 1054 - 1062, May 2009.
- [13] W.-S. Wuen and K.-A. Wen, "Dual-band switchable low noise amplifier for 5-GHz wireless LAN radio receivers," in Proc. IEEE Midwest Symp. Circuits Systems, vol. 2, 2002, pp. II-258-II-261.
- [14] V. Vidojkovic, J. van der Tang, E. Hanssen, A. Leeuwenburgh, and A. van Roermund, "Fully-integrated DECT/Bluetooth multiband LNA in 0.18 μ m CMOS," in Proc. IEEE Int. Symp. Circuits Systems, vol. 1, 2004, pp. I-565-I-568.
- [15] T. K. K. Tsang and M. N. El-Gamal, "Dual-band sub-1 V CMOS LNA for 802.11a/b WLAN applications," in Proc. IEEE Int. Symp. Circuits Systems, vol. 1, 2003, pp. 217-220.

- [16] Z. Li, R. Quintal, and K. K. O, "A dual-band CMOS front-end with two gain modes for wireless LAN applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 2069-2073, Nov. 2004.
- [17] Edwin C. Becerra-Alvarez, F. Sandoval-Ibarra and J.M. de la Rosa, "Continuously-Tuned 1-V 90-nm CMOS LNAs for Multi-Standard Wireless Applications", *Proc. of the 2011 Workshop on Analog and Digital Electronic Design (WADED)*, Oct. 5-7 2011, Mexico.
- [18] S. Mou, J. Ma, K. S. Yeo, and M. A. Do, "An integrated SiGe dual- band low noise amplifier for Bluetooth, HiperLAN and wireless LAN applications," in *Proc. Eur. Microwave Conf.*, vol. 1, Oct. 2003, pp. 5-8.
- [19] N. M. N. L. Li Lian and M. Mustafa, "A dual-band Ina with 0.18 μm cmos switches," in *Micro and Nanoelectronics (RSM), IEEE Regional Symposium* , pp. 172-176, 2011.
- [20] F. S.-I. E.C. Becerra-Alvarez and J. M. D. L. Rosa, "Design of a 1- V 90-nm CMOS adaptive LNA for multi-standard wireless receivers," *Revista Mexicana de Fisica*, vol. 54, pp. 322-328, 2008.
- [21] Abdelkader Taibi, Abdelhalim Slimane, Mohand Tahar Belaroussi, Sid Ahmed Tedjini, "Low power and High linear Reconfigurable CMOS LNA for Multi-Standard Wireless Applications," in *Microelectronics (ICM)*, pp. 1-4, 2013.

- [22] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 1998, ch. 11.
- [23] Peitro Andreani and Henrik Sjølland, "Noise optimization of an inductively degenerated CMOS low noise amplifier," *IEEE Trans. Circuits and Systems-IT. Analog and Digital Signal Processing*, vol.48, No.9. pp.835-841, September 2001.
- [24] T.-K. Nguyen, C.-H. Kim, G.-J. Ihm, M.-S. Yang, , and S.-G. Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 5, pp. 1433-1442, May 2004.
- [25] Schaeffer, D. K., and Lee, T. H., "A 1.5 V, 1.5 GHz CMOS Low Noise Amplifier," *IEEE J. Solid-State Circuits*, 32, 745, 1997.
- [26] <http://literature.agilent.com/litweb/pdf/5980-0490E.pdf>
- [27] H.W. Chiu, et al., "A 2.17-dB NF 5-GHz-band monolithic CMOS LNA with 10-mW DC power consumption," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 3, pp. 813-824, Mar. 2005.
- [28] B. Mohammadi, et al., "5.8 GHz CMOS LNA for WLAN applications," *IEEE RFIC Symp. Dig.*, pp. 113-116, 2004.
- [29] F. Silveira et. al. "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE Journal of Solid-State Circuits*, Sept. 1996, pp. 1314-1319.

- [30] D. Flandre, A. Viviani, J.-P. Eggermont, P. Jespers, "Improved synthesis of regulated-cascode gain-boosting CMOS stage using symbolic analysis and gm/ID methodology", IEEE Journal of Solid-State Circuits (Special Issue on 22nd ESSCIRC conference), 32 (1997) 1006-1012.
- [31] B. E. Boser, "Analog Circuit Design with Submicron Transistors," IEEE SSCS Meeting, Santa Clara Valley, May 19, 2005,