Fall 2005

CEG 260: Digital Computer Hardware Switching Circuits

Eric Matson
Wright State University - Main Campus

Computer Engineering (CEG) 260
Digital Computing Hardware/Switching Circuits

Fall Quarter 2005
Wright State University

Course Description
We will discuss and cover basic digital, combinational and sequential logic systems. Labs will be used to gain valuable practical experience in implementing elementary circuits and logic designs.

Goals
There are several goals to accomplish in CEG 260
1. Master numbering systems and basic circuit theory
2. Gain practical experience in designing logic systems
3. Develop a foundation for further study in this area
4. Enjoy the process!

Lecturer
Eric Matson
Office: 336 Russ Engineering Center
Phone: 937-775-5108
Office Hours: 10:00 – 12:00 am Tuesday/Thursday
Email: eric.matson@wright.edu
Web: www.cs.wright.edu/~matson

Class
- Tuesday/Thursday 12:20 – 1:35 153 Russ Engineering Center
- Lab each week, starting in the second week of class

Text
Required: *Logic and Computer Design Fundamentals, Mano and Kime, Prentice-Hall 2004.*

Required Work

Homework	20%	Lots of homework problems!
Lab	30%	8 Lab Assignments
Quizzes	10%	Quizzes to keep everyone up with the class readings!
Midterm Exam	20%	
Final Exam	20%	

Grading
The base scale is: A: 90-100, B: 80-89, C: 70-79, D: 60-69, F: 0-59. This is the highest requirement that will be used. The scales may be lowered or revised if necessary.

You must achieve a minimum of 60% in the lab section and all labs must be completed to pass the course. Lab is a crucial element for learning design fundamentals.

Policies and Notes

- Attendance: Attendance is not required, nor will it be taken after the first couple of lectures. If you are not a regular attendee, it will be your responsibility to seek out what material was covered in the lecture and learn it. Most of my exam questions will be taken directly from ideas covered during the lecture, so it greatly helps if you attend!

- I will utilize my CS web page (www.cs.wright.edu/~matson) to post updates to the course, solutions, assignments, announcements, schedule, etc. Get in the habit of checking it regularly.

- Always make back ups of all of you work. Never have just one copy of anything!

- If you are going to miss an exam, for any reason, discuss it with me in advance. If it is an emergency situation, please notify me as soon as possible

- You can reach me a number of ways. Email is normally the best as I check it about 18 hours a day normally. You can also reach me by phone during the day at 775-5108. If you need human contact either stop in during my office hours, make an appointment, or just come by my office. If I am in and not on a deadline to get something else completed, I will normally try to help as much as possible.

- There are technologies we will use in this class that you may not already know, such as working with tools in lab. We will cover some of these technologies or they will be discussed in lab. If you have trouble, please don't hesitate to come and talk with one of the teaching assistants or me.

- The key to learning in this class will be spending time working through the problems. Don't wait until 2 hours before something is due to try to learn the concept. This normally ends in a disaster! Stay up with the readings and try to work through some of the problems in the book. There will be lots of problems, so try and work through them when you get them and don't wait until the end. *This is not a class where 3 hours of "cramming" right before the midterm/final will translate into a good grade!*

Academic Misconduct

In this class, the only way to truly learn the concepts to is do the work yourself. I encourage working with other people on the course concepts. When you begin to write the assignment, complete and submit your own work.

Work that has obviously been copied or in the more extreme case, when the original author's name has not even been changed, both parties will receive a 0 grade for that assignment. Both parties will also be turned over to the Office of Judicial Affairs.

Schedule

#	Day	Date	Topic	Reading	Labs
1	T	Sept 6	Introduction	1.1 – 1.2	
2	U	Sept 8	Number Systems, Gates	1.3 – 1.7, 2.1	
3	T	Sept 13	Boolean Algebra/Circuit Design	2.2 – 2.3	1
4	U	Sept 15	Optimization/Maps	2.4	
5	T	Sept 20	Lab work/Quiz #1		
6	U	Sept 22	**No Class**		
7	T	Sept 27	Karnaugh Maps	2.5 - 2.6	2
8	U	Sept 29	Optimization/Gates	2.7 - 2.10	
9	T	Oct 4	Logic Design	3.1 – 3.3	3
10	U	Oct 6	Logic Design/Review	3.4 – 3.6	
11	T	Oct 11	**Midterm Examination**		4
12	U	Oct 13	Decoders/Encoders	4.1 – 4.3	
13	T	Oct 18	Multiplexers	4.4 – 4.6	5
14	U	Oct 20	Latches	6.1 – 6.2	
15	T	Oct 25	Flip flops	6.3 – 6.6	6
16	U	Oct 27	Registers	7.1	
17	T	Nov 1	Counters	7.6	7
18	U	Nov 3	Arithmetic Circuits	5.1 – 5.4	
19	T	Nov 8	Arithmetic Circuits		
20	U	Nov 10	Review		
21	T	Nov 15	**FINAL EXAM 1:00 – 3:00**		

Always have readings scheduled for that day complete prior to the class meeting

Note: T = Tuesday
W = Thursday