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Fall 2006

CEG 420/620: Computer Architecture

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CEG 420/620 Computer Architecture

Fall 2006, 2:15-3:30 PM, Tue., Thr., at 155 RC

Instructor: Jack Jean

Office Hours: 1:40-2:40 PM, M, W; 1:10-2:10 Tue., Thr.; 334 RC, 775-5106, jack.jean@wright.edu

Textbook: **Computer Organization and Design**, 3rd edition, David Patterson and John Hennessy, Morgan Kaufmann, 2005.

Reference: **Modern Processor Design**, 1st edition, John Paul Shen and Mikko H. Lipasti, McGraw Hill, 2005.

Weekly Schedule:

Week	Contents	Chapters to Read
1	Overview, Processor Instructions	1, 2
2	Computer Arithmetic	3
3	Computer Arithmetic; CPU Performance	3, 4
4	Datapath and Control	5
5	MIDTERM ; Datapath and Control	5
6	Pipelining	6
7	Pipelining	6
8	Pipelining; Memory Hierarchy	6,7
9	Memory Hierarchy	7
10	Computer Peripherals	8

Grading: Final letter grade: 90+ (A), 80+ (B), 70+ (C), 60+ (D), otherwise (F).

- Project - 20%.
- HW - 10%
- Midterm - 30%; Oct. 3, Tue.; open book and notes.
- Final - 40%; Nov. 16, Thur., 3:15-5:15PM; Not comprehensive, open book and notes.
- Students taking CEG620 will be assigned more analysis works for assignments/tests.