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Effect of multistep wafer-annealing on main traps in Czochochalski-grown semi-insulating GaAs

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Both multistep wafer-annealed (MWA) and ingot-annealed semi-insulating (SI) GaAs wafers, grown by the Czochochalski technique, are characterized by using normalized thermally stimulated current (NTSC) spectroscopy. Two main NTSC traps, T_3 at 200 K and T_5 at 140 K, which are thought to be related to arsenic vacancy defects, are found to be largely suppressed by MWA processes, especially by a new MWA process. Concomitant with a decrease of these traps, a significant increase of the threshold electrical field for both the thermal quenching of T_5 and the low-temperature photocurrent saturation has been observed. © 1996 American Institute of Physics. [S0003-6951(96)00946-1]

In order to obtain high quality semi-insulating (SI) GaAs substrates, suitable for GaAs device and integrated circuit fabrications, a new annealing process, multistep wafer annealing (MWA) has been developed.^{1,2} The microscopic defects (As precipitates), the uniformity, and the purity in the MWA substrates, have been studied by chemical etching, coulometric titration analysis,³ microscopic resistivity distribution,³ cathode luminescence,³ photoluminescence (PL) topography,⁴ and selective pair PL.⁵ The studies show an obvious reduction of As precipitates and a significant improvement of uniformity and purity in the MWA SI GaAs. In this letter we report the effects of MWA on the main traps in Czochochalski (CZ)-grown SI GaAs. Five wafers, described in Table I, were used in this study. The first three wafers listed were from different sections of the same boule. Wafers cut from a given section show similar electrical properties.

The conventional ingot annealings are usually carried out at 900–1000 °C, while the MWA includes, as a first step, annealing in an evacuated quartz ampoule with arsenic at 1100 °C for 5 h, and, as a second step, annealing in an open tube furnace at 950 °C for 3 h. The details of these annealing procedures are given in Ref. 1. The major difference between the old and new versions of the MWA is that the arsenic vapor pressure during the 1100 °C annealing was increased by approximately a factor three for the new process (wafer 13), as compared with the old one (wafer d2–186). The electrical properties (averaged over three samples cut from the center, the ring, and the edge of a particular wafer) and the average etch pit densities of the wafers are summarized in Table I. The main traps were measured by thermally stimulated current (TSC) spectroscopy. To compare trap densities, a normalization procedure based on temperature dependent photocurrent (TDPC) was employed; it can be shown that the normalized ratio I_{TSC}/I_{PC} (called NTSC) is independent of mobility μ , lifetime τ , and geometric factors.⁶ Thus, the NTSC spectrum gives a truer picture of the relative trap densities.

Figure 1(a) shows regular TSC spectra from the center areas of a new MWA wafer and an ingot-annealed wafer, respectively. The TDPC's, using a weak 1.13 eV light with an intensity of 3.3×10^{14} photon/cm² s, are also presented in the figure. From Fig. 1(a), six traps, i.e., T_2 at 220 K, T_3 at 200 K, T_4 at 155 K, T_5 at 140 K, T_5^* at 125 K, and T_6^* at 94 K, can be observed in the ingot-annealed sample, and some new features, i.e., T_a at 170 K and T_6 at 100 K, in the new MWA sample. The apparent trap parameters, i.e., activation energy E_T and capture cross section σ_T , for the traps T_2 , T_3 , T_5 , and T_6^* have been determined using Arrhenius plots of $\ln T_m^4/\beta$ vs $1/T_m$, where T_m is the peak temperature for a given trap and β the heating rate in the thermal scan. The parameters are 0.63 eV and 1.9×10^{-13} cm² for T_2 , 0.50 eV and 1.1×10^{-13} cm² for T_3 , 0.35 eV, and 1.9×10^{-14} cm² for T_5 , and 0.15 eV and 1.8×10^{-17} cm² for T_6^* , respectively.⁷ In the same way, the E_T and σ_T for T_6 were determined to be 0.16 eV and 3.6×10^{-17} cm², respectively. In order to study the effect of the new MWA process on the main traps in SI GaAs, the measured TSC spectra in Fig. 1(a) were normalized by the corresponding TDPC, and the normalized (NTSC) spectra are shown in Fig. 1(b). From Fig. 1(b), we see that: (1) the dominant traps in the two SI GaAs samples are T_2 and T_5 ; (2) T_6^* is not a dominant trap and, in fact, the high TSC of T_6^* seen in the regular spectrum is simply due to the high carrier mobility and apparent lifetime at the T_6^* peak temperature, which also results in a high PC; (3) there is almost no change in the density of T_2 after the new MWA process; and (4) the densities of T_3 and T_5 are clearly reduced by the wafer annealing.

In Fig. 2 are shown the NTSC spectra for center samples from old MWA, ingot-annealed+old MWA, and ingot-annealed wafers, respectively. From the figure, once again we see nearly no change in the density of T_2 but a reduction in the densities of T_3 and T_5 . The normalized TSC spectra for samples subjected to either the old MWA or the ingot-anneal+old MWA processes are very similar to each other, which implies that the traps in these SI GaAs samples are mainly controlled by the wafer (MWA) annealing. Similar to

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TABLE I. Average electrical properties and etch pit density (EPD) for studied wafers.

Wafer	Process	Resistivity $10^7 \Omega \text{ cm}$	Mobility $10^3 \text{ cm}^2/\text{V s}$	Electron concentration 10^7 cm^{-3}	EPD 10^4 cm^{-2}
d2-186, 3 in.	Old MWA	10.07	7.12	1.10	3.7
d4-86, 3 in.	Ingot-anneal + old MWA	6.28	7.69	1.45	4.9
d6-80, 3 in.	Ingot-anneal	4.62	7.61	1.79	4.4
13, 3 in.	New MWA	4.97	7.22	1.76	4.4
a-12, 4 in.	Ingot-anneal	3.79	7.37	2.24	7.1

the effect of the new MWA, the old MWA also causes a disappearance of T_6^* ; however, it does not create the new feature T_6 .

In the past, the nature of the main traps, T_2 , T_3 , and T_5 , has been carefully studied by TSC spectroscopy in conjunction with sample conditions, measurement conditions (such as illumination time and electrical field), and the infrared (IR) quenching of EL2 and its thermal recovery. In one of our earlier studies, As-rich and Ga-rich stoichiometries in CZ-grown wafers were observed to favor higher T_2 and T_3 , respectively, in the TSC spectra.⁸ The profile of T_2 across the diameters of wafers grown by the high-pressure (HP) and low-pressure (LP) liquid encapsulated Czochralski (LEC) and vertical gradient freeze (VGF) techniques, respectively, has the same shape as the profile of the respective dark current at 300 K, which is well-known to be controlled by both

EL2⁰ and EL2⁺; also the profiles of T_2 and T_3 across the diameter of a typical LP-LEC wafer show an anticorrelation, i.e., a W- vs M-shape.⁹ The T_2 and T_3 defects are quenchable under IR illumination at 90 K; i.e., the traps T_2 and T_3 both disappear, changing into a trap T_2^* (peaking at 210 K) after complete IR quenching of EL2, and recovering after annealing at 124 K.¹⁰ A good correlation between the T_2 trap density and the positron trapping rate at the metastable vacancy associated with EL2* in SI GaAs has been recently observed,⁷ which further supports the fact that As-rich conditions favor the formation of T_2 . Based on these results we infer that T_2 is related to As_{Ga} , but is not identical to EL2 because of its different activation energy (0.63 eV for T_2 vs 0.75 eV for EL2), and that T_3 might be associated with V_{As} , most likely a V_{As} -related defect complex. On the other hand, the As-rich stoichiometry melt in CZ growth also favors higher T_5 .⁸ Based mainly on its IR quenching behavior¹⁰ and its thermal recovery at a rate $r = 2.0 \times 10^8 \exp(-0.26 \text{ eV}/kT) \text{ s}^{-1}$,¹¹ which is very close to that of EL2, T_5 is probably also related to As_{Ga} . Furthermore, an electrical-field-enhanced thermal quenching of T_5 , i.e., the disappearance of T_5 during a TSC scan at high applied bias, can be more frequently observed in VGF samples than in HP-LEC samples.¹² Since HP-LEC samples generally have more EL2 than VGF samples, the smaller thermal quenching of T_5 in the former material implies that the As_{Ga} density is not the only relevant factor. The values of E_T and σ_T obtained for T_5 are very close to those of the EL6 level, which is often observed by DLTS in undoped semi-conducting VGF and LEC GaAs samples, but more abun-

FIG. 1. (a) Regular TSC spectra and TDPCs (using 1.13 eV) for two center samples cut from ingot-annealed and MWA wafers, respectively. (b) NTSC spectra (i.e., $I_{\text{TSC}}/I_{\text{PC}}$) for the same samples.

FIG. 2. NTSC spectra for three center samples cut from old MWA, ingot-annealed+old MWA, and ingot-annealed wafers, respectively.

dantly in VGF samples.¹³ Recently, a good correlation between the T_5 trap density and the positron trapping rate for V_{As} at 80 K has been found,⁷ which indicates the involvement of V_{As} in T_5 . Therefore, we infer that T_5 might be a complex involving both As_{Ga} and V_{As} . Actually, EL6 has also been identified with a defect complex involving As_{Ga} (or $V_{Ga}-As_i$) and V_{As} .¹⁴⁻¹⁶

From a stoichiometry point of view and based on the Ga-As phase diagram, the mechanism of arsenic precipitation in LEC-grown SI GaAs and the dissolution of arsenic precipitates by MWA have been discussed in Refs. 1-3. However, from the defect point of view, in addition to large defects, such as the As precipitates, there exist various point defects, such as As_{Ga} , Ga_{As} , V_{Ga} , V_{As} , and As_i , and their complexes in either as-grown or ingot-annealed LEC SI GaAs.^{17,18} The abundance of the point defects depends not only on the crystal stoichiometry, but also on the crystal growth conditions and the postgrowth annealing parameters, including the cooling rate after the annealing. High-temperature wafer annealing at 1000-1200 °C, either under an arsenic vapor pressure³ or in vacuum,¹⁹ causes an n - to p -type conversion. According to Oda *et al.*³ and Mori *et al.*,¹ the reason for the n to p -type conversion is because of the decrease of EL2 due to its dissolution into the crystal matrix, or because of As outdiffusion to the wafer surface; both can be controlled by the arsenic overpressure. According to Ohkubo *et al.*,¹⁹ the defect reaction $As_{Ga} \rightarrow V_{Ga} + As_i$ is possibly responsible for the reduction of EL2, since V_{Ga} generated by this process acts as an acceptor and a measured hole trap at $E_v + 0.52$ eV might originate from this V_{Ga} . In addition to these mechanisms, there possibly exists a localized movement of As_i defects from the cell walls to nearby V_{As} defects, giving the reaction $V_{As} + As_i \rightarrow As_{As}$, which results in a more uniform crystal due to the annihilation of arsenic vacancies. The reduction of the V_{As} -related traps, T_3 and T_5 , by MWA procedures, especially by the new MWA, supports the third mechanism. Medium-temperature wafer annealing at 950 °C can regenerate EL2 by the reactions $As_{As} + V_{Ga} \rightarrow As_{Ga} + V_{As}$ or $As_i + V_{Ga} \rightarrow As_{Ga}$.²⁰ In a selective pair PL study, two residual acceptor impurities, Zn_{Ga} and Si_{As} , were found to be noticeably reduced by MWA,⁵ which may be another indication of reduction of V_{Ga} and V_{As} in the MWA crystal. From the above discussion, we surmise that the arsenic vapor pressure during high-temperature annealing is a key factor in controlling the abundance of V_{As} - and As_{Ga} -related point defects.

Interestingly, as a consequence of the further decrease in V_{As} defect-related traps, T_5 in the new MWA samples shows a much less electrical-field-enhanced thermal quenching as compared to that of the old MWA samples. We find that a threshold electrical field, $\mathcal{E}_{th}$, for the thermal quenching of T_5 in the new MWA sample, is close to 42 V/cm, while in the old MWA sample between 11 and 21 V/cm. As we indicated in Ref. 12, the PC using 1.45 eV photons at 83 K saturates at electrical fields that are high enough to cause TSC quenching of T_5 . In Fig. 3, we present the PC's as a

FIG. 3. Photocurrents (using 1.45 eV) at 83 K. Note that they saturate at different biases for the ingot-annealed and MWA samples.

function of bias for four samples (two of them are ingot annealed and the other two have experienced MWA). From the figure, we find that: (1) the PC's all show an Ohmic behavior at lower biases and then saturate at higher biases; and (2) the biases for PC saturation in the MWA samples (using either the old or new versions) are much higher than those in ingot-annealed samples. These results could mean that the V_{As} -related defects in SI GaAs play an important role in the thermal quenching of T_5 and the 83 K PC saturation behavior.

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