

Fall 2006

# CEG 720: Computer Architecture I

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# CEG 720 Computer Architecture I

Fall Quarter, 2006

*Catalog Data : Review of sequential computer architecture and study of parallel computers. Topics include memory hierarchy, reduced instruction set computer, pipeline processing, multiprocessing, various parallel computers, interconnection networks, and fault-tolerant computing. 3 hours lecture and 2 hours lab.*

**Prerequisite** : CEG633, or CEG520 and CEG611

**Prerequisite Topics**: Process management, CPU scheduling, Memory management, Cache management, Disk management. If not familiar with these topics, take CEG433/633 (Operating Systems) first.

**Instructor** : Dr. Soon M. Chung

403 Russ Engineering Center (775-5119)

soon.chung@wright.edu, <http://www.cs.wright.edu/~schung>

**Class** : Section 01: Tu. Th. 2:15-3:30 pm at 248 Oelman

Section 02: Tu. Th. 6:05-7:20 pm at 154 Russ

**Office hour** : Tu, Th. 3:45-4:45 pm at 403 Russ, or by appointment.

\*use e-mail for short questions.

**Text Book** : K. Hwang, Advanced Computer Architecture: Parallelism, Scalability, and Programmability, McGraw-Hill, 1993.

## References :

J. L. Hennessy and D. A. Patterson, Computer Architecture, Morgan Kaufmann.

A. Silberschatz, P. Galvin, and G. Gagne, Operating System Concepts.

D. Sima, T. Fountain and P. Kacsuk, Advanced Computer Architectures, Addison-Wesley.

## Topics : Parallel Computer Models (Chapter 1)

Processors and Memory Hierarchy (Chapter 4)

Bus, Cache, and Shared Memory (Chapter 5, Section 8.1.2)

Interconnection Networks (Section 2.4)

Pipeline and Superscalar Techniques (Chapter 6)

Multivector and SIMD Computers (Sections 8.1 and 8.4)

Multiprocessors and Multicomputers (Section 7.1)

**Grading** : A:[85,100], B:[75,85), C:[65,75), D:[55,65), F:[0,55)

Midterm 30% (10/12, Tu.)

Final 40% (Section 01: 11/16, Th. 3:15-5:15 pm)

(Section 02: 11/16, Th. 8:00-10:00 pm)

Paper-review project 30% {papers referenced 7%, organization 6%,  
written presentation 8%, discussion 9%}

## CEG 720 Project

1. Choose a topic and select at least 5 relevant technical papers. High-quality journal papers are preferred.
2. Summarize and compare the papers, and then add your own discussion.
3. Submit the working title and the list of candidate papers. (due 10/17)
4. Present in the class (?), and submit the report and the papers you studied. (due 11/16)
5. Size of the report is between 25 and 35 double-spaced pages.
6. This project can be done as an individual project or a team (of two) project.

### Possible Topics

- Multiprocessor cache management
- SIMD, MIMD machines
- Fault tolerant computing
- Parallel algorithms
- Performance evaluation of parallel computers
- Interconnection networks
- Cluster and GRID computing
- RISC/CISC processors
- Reconfigurable array of processors
- Optical computing
- Application specific architectures
- Realtime computer systems
- Artificial neural network
- Other relevant topics

### Reference Sources

- IEEE Transactions on Computer
- Computer (IEEE Computer Magazine)
- Communications of ACM
- IEEE Tutorials, such as Tutorial on computer architecture, on supercomputing, etc.
- Proceedings of Int'l Conf. on Parallel Processing
- Proceedings of Int'l Symposium on Computer Architecture: available in the volumes of Computer Architecture News
- Journal of Parallel and Distributed Computing
- ACM Transactions on Computer Systems
- IEEE Transactions on Parallel and Distributed Systems
- ACM Computing Surveys
- ACM/Springer Multimedia Systems
- IEEE Multimedia
- ACM Transactions on Modeling and Simulation
- IEEE Transactions on Knowledge and Data Engineering
- IEEE Transactions on VLSI
- IEEE Transactions on Neural Networks
- IEEE Micro
- Journal of Supercomputing
- and others

## CEG 720 Computer Architecture I

### Prerequisite Test

Briefly answer the following questions.

1. What is the definition of a process?
2. List a couple of CPU scheduling algorithms and explain how they work.
3. Explain the *paging* memory management scheme and the role of a page table.
4. Explain a couple of cache block replacement algorithms.