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Very high channel conductivity in low-defect AlN/GaN high electron mobility transistor structures

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Low defect AlIn/GaN high electron mobility transistor (HEMT) structures, with very high values of electron mobility (>1800 cm²/V s) and sheet charge density (>3×10¹³ cm⁻²), were grown by rf plasma-assisted molecular beam epitaxy (MBE) on sapphire and SiC, resulting in sheet resistivity values down to ~100 Ω/□ at room temperature. Fabricated 1.2 μm gate devices showed excellent current-voltage characteristics, including a zero gate saturation current density of ~1.3 A/mm and a peak transconductance of ~260 mS/mm. Here, an all MBE growth of optimized AlN/GaN HEMT structures plus the results of thin-film characterizations and device measurements are presented. © 2008 American Institute of Physics. [DOI: 10.1063/1.2970991]

High electron mobility transistors (HEMTs) based on AlGaN/GaN heterostructures have been extensively studied for their potential application in high power, high frequency, and high temperature amplifiers. However, as the device dimensions are being reduced, a number of issues including rf current collapse, leakage currents, and short channel effects have severely hindered the progress. Variations in the basic structure, including indium-containing HEMTs such as AlGaN/InGaN/GaN, have also been investigated in response to theoretical predictions of higher performance devices. Recently, the insertion of a thin (~1 ML) film of AlN in the HEMT structure has been shown to improve the device performance by increasing the two dimensional electron gas (2DEG) confinement and reducing alloy scattering. However, much less work has been done on AlN/GaN heterostructure for HEMT devices mainly due to the difficulty in growing high-quality AlN barrier layers on GaN by either metal organic chemical vapor deposition (MOVCD) or molecular beam epitaxy (MBE). Nonetheless, the expected reduction in short channel effects and lower threshold voltages, using ultrathin AlN barrier layers, makes these structures of great interest for very high frequency and high power applications.

Previous attempts to grow AlN/GaN HEMTs directly on sapphire substrates have produced structures with limited room-temperature (RT) 2DEG mobility (μRT<500 cm²/V s), which resulted in high values of sheet resistance, ρs, in spite of very large 2DEG densities (n₂>2×10¹³ cm⁻²). To date, the best ρs values for AlN/GaN HEMTs have been demonstrated by rf plasma-assisted MBE on thick MOCVD grown templates that contain a low density of threading dislocations (TDs). Based on these results, it may be concluded that the quality of the 2DEG, generated by strong polarization fields at the AlN/GaN interface, can be severely degraded by a number of factors including a high density of TDs, interface roughness, and/or cracking of the highly strained AlN layer. On one hand, for high-quality AlN/GaN HEMTs the AlN barrier should be thick enough to provide both a high density of carriers and good confinement of 2DEG. On the other hand, the critical thickness for dislocation formation in the AlN barrier layer, with about 2.4% lattice mismatch on GaN, can be as small as 3 nm depending on growth conditions and interface quality. In this work we demonstrate that AlN/GaN HEMT structures, directly grown on sapphire and SiC under optimized conditions, can show both very high values of μRT and n₂, resulting in record low values of ρs in III-nitride HEMTs. We will also present the results of dc and pulsed device characterization on these structures.

AlN/GaN HEMT structures were grown on c-plane sapphire and semi-insulating 6H-SiC in a MBE system equipped with a rf nitrogen plasma source from SVT Associates (SVTA-RF45). During growth, reflection high-energy electron diffraction was used to monitor surface morphology. Other in situ measurements, including emissivity-corrected surface temperature, thin film growth rate, and III/V flux ratio were performed by a combination of pyrometry and two-color reflectometry (SVTA-IS4000). The growth process started with surface preparation at high temperatures by either removing the surface oxides, in the case of SiC, or nitridation using rf plasma source, in the case of sapphire, followed by the growth of a thin AlN nucelation layer. Next, a 2–3 μm low-defect GaN buffer was grown. A relatively low TD density (<1×10⁶ cm⁻²) in these films was confirmed by both etch pit density measurements, using atomic force microscopy (AFM), and by transmission electron microscopy (TEM). Finally, the AlN/GaN active layer was formed by growing a thin (<5 nm) AlN layer at about 700 °C. To protect the AlN layer, ~1 nm of undoped GaN cap layer was grown on some samples. For comparison, a number of conventional AlGaN/GaN HEMT structures were also grown on sapphire and SiC. The optical and electrical properties of the samples were characterized by cathodoluminescence, Hall, and capacitance-voltage measurements. The thin film quality and surface roughness were studied by x-ray diffraction, TEM, and AFM.

Some of the AlN/GaN structures were processed using standard photolithography to fabricate metal oxide semiconductor (MOS) HEMTs for device measurements. The device
Table I. Results of RT Hall measurements for several AlIN/GaN and AlGaIN/GaN HEMTs grown on sapphire and SiC.

<table>
<thead>
<tr>
<th>Sample</th>
<th>$n_s$ (cm$^{-2}$)</th>
<th>$\mu_{RT}$ (cm$^2$/V s)</th>
<th>$\rho_s$ (Ω/$\square$)</th>
<th>HEMT structure</th>
<th>Substrate</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$5.47 \times 10^{12}$</td>
<td>1220</td>
<td>937</td>
<td>1 nm GaN / 2.0 nm AlN / 3.0 nm GaN</td>
<td>Al$_2$O$_3$</td>
</tr>
<tr>
<td>2</td>
<td>$1.83 \times 10^{15}$</td>
<td>1610</td>
<td>213</td>
<td>1 nm GaN / 3.0 nm AlN / 3.0 nm GaN</td>
<td>Al$_2$O$_3$</td>
</tr>
<tr>
<td>3</td>
<td>$2.50 \times 10^{15}$</td>
<td>1780</td>
<td>140</td>
<td>1 nm GaN / 3.5 nm AlN / 3.0 nm GaN</td>
<td>Al$_2$O$_3$</td>
</tr>
<tr>
<td>4</td>
<td>$3.27 \times 10^{15}$</td>
<td>1130</td>
<td>170</td>
<td>1 nm GaN / 4.0 nm AlN / 3.0 nm GaN</td>
<td>Al$_2$O$_3$</td>
</tr>
<tr>
<td>5</td>
<td>$4.10 \times 10^{15}$</td>
<td>110</td>
<td>1390</td>
<td>1 nm GaN / 5.0 nm AlN / 3.0 nm GaN</td>
<td>Al$_2$O$_3$</td>
</tr>
<tr>
<td>6</td>
<td>$1.68 \times 10^{15}$</td>
<td>1630</td>
<td>228</td>
<td>2 nm GaN / 3 nm AlN / 3.0 μm GaN</td>
<td>Al$_2$O$_3$</td>
</tr>
<tr>
<td>7</td>
<td>$2.30 \times 10^{15}$</td>
<td>1460</td>
<td>185</td>
<td>1 nm GaN / 3.5 nm AlN / 2.0 μm GaN</td>
<td>6H-SiC</td>
</tr>
<tr>
<td>8</td>
<td>$1.05 \times 10^{15}$</td>
<td>1830</td>
<td>325</td>
<td>2 nm GaN / 20 nm Al$_{1-x}$Ga$_x$N / 3.0 μm GaN (reference)</td>
<td>Al$_2$O$_3$</td>
</tr>
<tr>
<td>9</td>
<td>$9.60 \times 10^{12}$</td>
<td>1990</td>
<td>327</td>
<td>2 nm GaN / 20 nm Al$_{1-x}$Ga$_x$N / 2.0 μm GaN (reference)</td>
<td>6H-SiC</td>
</tr>
</tbody>
</table>

Table I shows the Hall measurements, averaged over the 2 in. wafer, for a number of AlIN/GaN HEMT structures grown on sapphire and SiC. Samples 1–5 in this table show that both $\mu_{RT}$ and $n_s$ values are strongly affected by small changes in the thickness of the AlN layer. On the low-defect GaN buffers grown by MBE in this work, the optimum AlIN thickness of 3.5 nm produced the lowest as-grown RT $\rho_s$ of ~140 Ω/$\square$ (sample 3). This is about twice the channel conductivity of typical high-quality AlGaIN/GaN HEMTs grown on sapphire or SiC (reference samples 8 and 9). To date, the highest RT and 77 K electron mobility values that we have measured on AlIN/GaN HEMT wafers are 1850 and 6530 cm$^2$/V s, respectively, at a relatively constant $n_s$ value of ~1.6 $\times$ 10$^{13}$ cm$^{-2}$. Temperature-dependent Hall measurements, performed on samples with $n_s$ as high as 3 $\times$ 10$^{13}$ cm$^{-2}$, also showed a constant $n_s$ from RT down to ~10 K (as shown in Fig. 1). Kuzmik et al. recently reported a $\rho_s$ of 237 Ω/$\square$ for an as-grown InAIN/AlAIN/GaN structure by MOCVD, which could be reduced to as low as 110 Ω/$\square$ by depositing a thin ZrO$_2$ layer. We have observed similar improvements in channel conductivity using a thin Al$_2$O$_3$ layers formed by ALD on the AlIN/GaN HEMTs. In one example, the as-grown average $\rho_s$ of ~259 Ω/$\square$ on a 2 in. AlIN/GaN HEMT dropped to an average of 156 Ω/$\square$ after depositing 15 nm of Al$_2$O$_3$, as measured by TLM. On the same wafers, we measured local $\rho_s$ values down to ~100 Ω/$\square$. This is the lowest RT sheet resistivity reported for any III-N based HEMT structure to date. Although the mechanism for such enhancement is not very well understood, these results point to the possibility of even higher channel mobility in HEMTs with lower as-grown $\rho_s$ values (e.g., sample 3), which is currently being investigated.

Samples with thicker AlIN barrier layers (e.g., 4 nm in sample 4) showed a large drop in $\mu_{RT}$, which resulted in a lower channel conductivity in spite of a substantially higher $n_s$. This might correspond to the onset of dislocation formation in the highly strained AlN layer, which has been reported to depend strongly on a number of extrinsic factors including starting density of TDs, growth conditions, and interface roughness. As the AlIN layer thickness was further increased to 5 nm or more (sample 5), much higher $n_s$ values ($>4 \times 10^{13}$ cm$^{-2}$) with lower values of $\mu_{RT}$ (<500 cm$^2$/V s) were obtained. We note that $n_s$ values ~6 $\times$ 10$^{13}$ cm$^{-2}$ have been theoretically predicted for these structures. The lower values of $\mu_{RT}$ coincide with the formation of a network of microcracks in the highly strained AlIN layer, as shown in the AFM images of Figs. 2(a) and 2(b). In addition to a crack-free surface morphology, high mobility samples were found to have atomically abrupt AlIN/GaN interface, as imaged by high resolution cross-sectional TEM, shown in Fig. 2(c). Figure 2(c) also shows the importance of growing these structures on low-defect GaN buffer.

![FIG. 1. Temperature dependent Hall measurements on two AlIN/GaN HEMT samples (circle and triangle symbols) showing higher 2DEG mobility (closed symbols) with a fixed sheet carrier density (open symbols) at lower temperatures.](attachment:image1.png)

![FIG. 2. (Color online) AFM images of (a) 4 nm and (b) 7 nm AlIN layer grown on GaN and (c) TEM image of an AlN/GaN HEMT structure.](attachment:image2.png)
layers in order to obtain smooth AlN/GaN interface for high \( \mu_{RT} \) values. Though the Coulomb scattering of 2DEG from the charged dislocation lines is expected to be well screened for \( n_g > 10^{12} \) cm\(^{-2} \), a large density of TDs can still reduce the mobility by scattering due to both strain variations across the interface, which results in a nonuniform polarization field, and increased surface roughness (e.g., by hillock formation).\(^{17} \) This is also indicated in recent calculations of Bulashevich et al.\(^{18} \) showing the effect of the interface rms roughness, \( \Delta \) resulting from TDs at a density of \( N_{TD} \), on the low-temperature mobility as \( \mu \propto \Delta_{rms} \). Finally, a comparison of samples 2 and 6 in Table I shows that to a lesser extent the thickness of the GaN cap layer can also affect \( n_g \), which could be caused by modifying the strain and/or the density of surface states.

Lastly, we examined the device performance of the AlN/GaN structures by measuring the dc and pulsed I-V characteristics of AlN/GaN HEMTs fabricated in this work. Figure 3 shows the dc (solid line) and pulsed (dotted line) I-V characteristics of a device grown on sapphire. The source-drain separation of the device was 4.5 \( \mu \)m. The gate length and width sizes were \( \sim 1.2 \) and 200 \( \mu \)m, respectively. The gate bias \( V_G \) was changed from 0 to \(-7 \) V in 1 V steps. The pulse length used was 1 \( \mu \)s. The pulse separation was 2 ms. The initial bias point for each pulse was zero gate and drain voltages. This bias point was chosen to highlight the effect of self-heating, which is seen as a drop in dc source-drain current \( I_{DS} \) at higher source-drain voltages \( V_{DS} \). As expected from very low \( \rho_s \) values, and considering the device dimensions used here, we obtained very high values of zero gate bias \( I_{DS} \sim 1.3 \) A/mm (Fig. 3) and peak transconductance \( g_{ms} \sim 260 \) ms/mm at a gate bias voltage of \(-3 \) V. However, these low \( \rho_s \) values also point to the need for further reduction in contact resistance in order to obtain higher currents. These results are consistent with recent measurements on AlN/GaN HEMTs grown on MOCVD GaN templates, showing very high current densities as the device dimensions are reduced,\(^{19} \) and point to the great potential of these HEMTs for very high-frequency and high-power applications.

In summary, we have demonstrated high-quality AlN/GaN HEMT structures directly grown on sapphire and SiC by rf plasma-assisted MBE. The strong confinement of the 2DEG and the reduction in roughness and alloy scattering in these structures resulted in both very high \( \mu_{RT} \) and \( n_g \) values. The observed RT sheet resistivity of 100 \( \Omega/\square \), on an AlN/GaN structure covered by a thin protective Al\(_2\)O\(_3\) layer, is the best reported value for a III-nitride HEMT to date. Based on the I-V characteristics of the MOS-HEMTs, with device dimensions used in this work, we expect record high dc and rf device performance for the short channel (<0.25 \( \mu \)m gate length) AlN/GaN HEMTs on SiC, which are currently being studied.

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