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# Deviations from bulk transport measurements in semi-insulating GaAs

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Because of the high bulk resistivity of semi-insulating GaAs, surface or near-surface effects can change the apparent magnitudes of resistivity, mobility, and carrier concentration. We consider the following causes: (1) above-surface conduction, such as that due to impurities in a porous oxide; (2) subsurface conduction, due to sawing and polishing damage; (3) tunneling conduction in surface states; and (4) changes in near-surface conduction due to the modification of surface potential by surface states or absorbates. The most important of these effects appear to be subsurface damage and surface potential changes.

## I. INTRODUCTION

Semi-insulating (SI) GaAs is an integral component of various GaAs and other III-V homostructure and heterostructure devices. Thus, it is important to be able to characterize SI GaAs accurately, especially its electrical properties, since the high resistivity of this material forms the basis of its usefulness. Unfortunately, the high resistivity makes accurate and reproducible electrical measurements difficult, mainly because surface or near-surface conductivity can shunt the current flowing in the bulk region, and thus obscure the bulk properties. Recent round-robin Hall-effect studies have shown that different laboratories can get widely differing results on the same SI GaAs samples, primarily because of variations in initial sample preparation. This problem has serious technological implications, since resistivity, mobility, and carrier-concentration values are used as acceptance standards by the GaAs device industry. In this study, we will consider the relative contributions of four possible components of "parasitic" conductance: (1) conduction in a porous oxide on the surface; (2) conduction in subsurface damage, often arising from the wafer-sawing and polishing processes; (3) conduction in surface states, which are known to be fairly dense ( $10^{12}$ – $10^{13}$  cm $^{-2}$ ) in GaAs; and (4) conduction in a near-surface region which is modified by the presence of the surface states or an absorbate. Also, procedures for minimizing the effects of these parasitic conductances will be offered.

## II. CONDUCTION PROCESSES

### A. Bulk conduction

Before discussing surface and near-surface conduction it is necessary to understand the bulk-conduction process, which arises from free electrons and holes:

$$\sigma_{\text{bulk}} = e(n\mu_n + p\mu_p), \quad (1)$$

where  $n$  and  $p$  are the concentrations of free electrons and holes in the conduction and valence bands, respectively, and  $\mu_n$  and  $\mu_p$  are their mobilities. For undoped liquid-encapsulated Czochralski (LEC) GaAs, the most widely used form of SI GaAs at present, the hole concentration is negligible,

and can be ignored. The electron concentration can be determined from the charge balance equation<sup>1</sup>:

$$n + N_A^{\text{net}} = \frac{N_D}{1 + (g_1/g_0)(n/N_C)e^{E_D/kT}}, \quad (2)$$

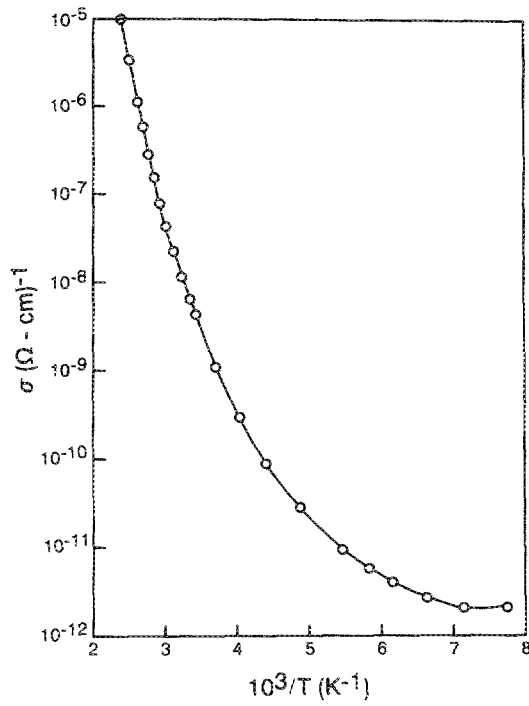
where  $N_D$  is the deep donor concentration (EL2 in this case),  $N_A^{\text{net}}$  is the net shallow acceptor concentration,  $g_1$  and  $g_0$  are the occupied- and unoccupied-state degeneracies, respectively,  $N_C$  is the effective conduction-band density of states, and  $E_D$  is the donor (EL2) activation energy. For temperatures below about 600 K,  $n$  for SI GaAs obeys

$$n = \left( \frac{N_D}{N_C} - 1 \right) \left( \frac{g_0}{g_1} N_C' e^{\alpha_D/k} \right) T^{3/2} e^{-E_{D0}/kT}, \quad (3)$$

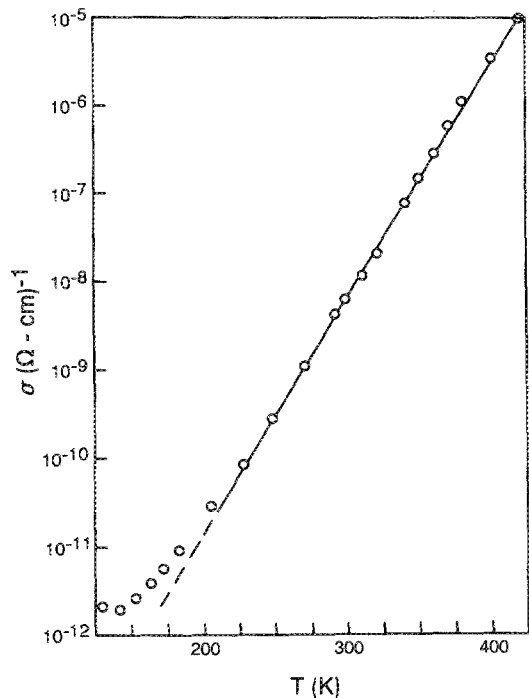
where  $N_C' = N_C/T^{3/2}$ , and  $\alpha_D$  is a temperature coefficient defined by  $E_D = E_{D0} - \alpha_D T$ . Thus, a plot of  $\ln(n/T^{3/2})$  vs  $T^{-1}$  should give a straight line with a slope of  $E_{D0}/k$ , where  $E_{D0} \approx 0.75$  eV for EL2-dominated GaAs. In fact, nearly all SI GaAs obeys Eq. (3) over the range 300–600 K, as shown in Fig. 1(a). However, at some lower temperature, the conductivity will begin to bend over, due to one or more of the parasitic components being discussed here. Although the sample shown in Fig. 1 is an extreme example (e.g., it was not cleaned or etched prior to measurement), nevertheless nearly all SI GaAs samples will show some effects of surface or subsurface conduction, even at room temperature.

### B. Above-surface conduction

All GaAs which has been exposed to air will have an oxide on the surface, probably composed mainly of Ga<sub>2</sub>O<sub>3</sub> and As<sub>2</sub>O<sub>3</sub>, with the former being more stable.<sup>2,3</sup> There is evidence that this oxide grows initially in a very compact form, but then converts to a colloidal porous layer, typically reaching 30–50 Å in thickness.<sup>4</sup> The porous material can trap impurities, which can directly lead to increased conduction, or can modify the surface states, which can change the surface potential and lead to an accumulation layer (with respect to the bulk potential) below the surface. Kuhnel *et al.*<sup>4</sup> have studied this problem by varying the purity of the final rinse water, used in the cleaning process. They hypoth-



(a)



(b)

FIG. 1. (a)  $\ln \sigma$  vs  $T^{-1}$  data for a Cr-doped, semi-insulating GaAs sample, which had not been cleaned or etched prior to measurement; (b)  $\ln \sigma$  vs  $T$  data for the same sample.

esize that very pure rinse water may wash out the impurities in the porous layer, while impure water may actually add further impurities. In any case, for water of resistivity  $\rho_{H_2O} < 10^4 \Omega \text{ cm}$ , they begin to see increased total sample conductance.

Besides impurities in the oxide, one must also be concerned about other conductive foreign matter, such as grease, on the surface. The sample shown in Fig. 1 was not cleaned at all before the data were taken, and it is clear that band conduction [Eq. (3)] does not dominate at room temperature and below. At low enough temperatures, because of the steep temperature dependence of the band conduction, surface conduction will nearly always be observed. However, routine measurements are typically made at room temperature, and we have found that most reasonable cleaning procedures will eliminate significant above-surface conduction; an indication is the applicability of Eq. (3) to the data.

### C. Subsurface conduction

It is known that sawing and polishing damage can extend several micrometers, even several tens of microns, into the GaAs bulk. It might be expected, and indeed it has been found, that various metal precipitates and other impurities can congregate preferentially in this damaged region. (In fact, sometimes surface damage is purposely used to getter impurities.) In Table I we present data which are not untypical of present-day SI GaAs. In this particular case it was necessary to remove about  $5 \mu\text{m}$  of material before bulk properties could be accurately measured. The data in Table I can be analyzed to yield the electrical properties of the  $5\text{-}\mu\text{m}$  layer itself<sup>5</sup>:

$$\rho_{\text{layer}} = \frac{\Delta d}{d} \frac{1}{\Delta(1/\rho)} = 2.5 \times 10^6 \Omega \text{ cm}, \quad (4)$$

$$\mu_{\text{layer}} = \frac{\Delta(\mu/\rho)}{\Delta(1/\rho)} = 5.4 \times 10^3 \text{ cm}^2/\text{V s} \quad (5)$$

$$n_{\text{layer}} = \frac{d}{e \Delta d} \frac{[\Delta(1/\rho)]^2}{\Delta(\mu/\rho)} = 4.6 \times 10^8 \text{ cm}^{-3}. \quad (6)$$

Although these numbers are somewhat inaccurate, still it appears that  $n$  is definitely higher in the damaged layer than in the bulk. As can be seen from Eq. (3), this situation could be caused by a much higher  $N_D$  ( $\equiv N_{\text{EL}2}$ ), or a much lower  $N_A^{\text{net}} \equiv N_{\text{AS}} - N_{\text{DS}}$ , where the subscript  $S$  refers to shallow (or, more precisely, shallower than EL2). The latter possibility is the most likely, with  $N_{\text{DS}}$  increasing to become on the order of  $N_{\text{AS}}$  in the damaged region. If  $N_{\text{DS}} > N_{\text{AS}}$ , however, then the deep EL2 level ( $N_D$ ) will no longer dominate

TABLE I. Measured electrical properties of undoped, semi-insulating, LEC GaAs, before and after a  $5 \mu\text{m}$  etch.

	$d$ (thickness, $\mu\text{m}$ )	$\rho$ ( $10^7 \Omega \text{ cm}$ )	$\mu$ ( $10^3 \text{ cm}^2/\text{V s}$ )	$n$ ( $10^7 \text{ cm}^{-3}$ )
Before etch	640	7.62	3.60	2.28
After etch	635	10.0	6.42	0.974

the electrical properties, and Eq. (3) will not apply at all [although Eq. (32) will still hold].

Thus, subsurface damage can certainly affect the measured electrical properties. However, an etch of several  $\mu\text{m}$  is usually sufficient to overcome this problem.

#### D. Tunneling in surface states

The surface of air-exposed GaAs is known to usually contain a high density of surface states,<sup>3,6</sup> about  $10^{13} \text{ cm}^{-2}$ . One scenario for the production of these states is that  $\text{As}_2\text{O}_3$ , formed from the oxidation process, is unstable, and that nearby Ga atoms extract the O, forming  $\text{Ga}_2\text{O}_3$ , and thus leaving unbonded As behind.<sup>2</sup> It is also known that the surface states must be able to bind electrons, since they remove free carriers from the near-surface region of *n*-type GaAs. Conceivably, these electrons could hop or tunnel from site to site, thus conducting current. The tunneling process leads to an interesting temperature dependence:

$$\sigma = \sigma_0 \exp(2\alpha^2 kT/M\omega^2), \quad (7)$$

where  $M$  is an atomic mass,  $\omega$  a characteristic vibrational frequency, and  $\alpha^{-1}$  a decay length for the atomic state. Equation (7), sometimes said to be of the Berthelot form, often fits semiconductor data quite well over a fairly extended temperature range, and has been invoked to possibly explain surface conduction in SI GaAs.<sup>7,8</sup> In Fig. 1(b) we plot in  $\sigma$  vs  $T$  for the same sample as that depicted in Fig. 1(a). Indeed, Eq. (7) fits the data reasonably well over five orders of magnitude. Similar examples of good fits can be found in the literature.<sup>7,8</sup> However, a problem arises when the magnitudes of the various parameters are considered. From the slope of the curve in Fig. 1(b), it is found that  $2\alpha^2 k/M\omega^2 \approx 6.2 \times 10^{-2}$ . The average atomic mass in GaAs is  $1.2 \times 10^{-22} \text{ g}$ , and a typical vibrational frequency would be  $\omega \approx 10^{12} \text{ s}^{-1}$ . Thus,  $\alpha^{-1} \approx 0.6 \text{ \AA}$ , which is much smaller than expected. (One would expect  $\alpha^{-1} \approx 2-3 \text{ \AA}$ , the interatomic distance in GaAs.<sup>9</sup>) Of more serious concern, however, is the calculated value of  $\delta \approx \Gamma(2kT/M\omega^2) \approx 2.6 \text{ \AA}$  at 300 K, where  $\delta^2$  should be mean-square atomic displacement of the vibrating atoms. Obviously,  $\delta$  cannot be nearly this large or the crystalline structure would not survive. A reasonable value of  $\alpha^2 \delta^2$ , the value of the argument in Eq. (7), would be

$[2(0.2)]^2 \approx 0.2$ , whereas the data yield  $\alpha^2 \delta^2 = 20$ , at 300 K.

A further problem is that the model leading to conduction according to Eq. (7) implicitly assumes that the surface states are as dense as the atomic states, i.e., about  $10^{15} \text{ cm}^{-2}$ ; this value is much too high for typical surface-state densities in GaAs. Emin<sup>9</sup> has suggested that the temperature dependence for transfer between two harmonic oscillator wells separated by  $R_0$  should be given in the term  $\exp(-\alpha^4 R_0^2 \delta^2)$ . Again, if  $\alpha^{-1}$  is taken to be about  $2.5 \text{ \AA}$ , then  $R_0^{-2} \approx 10^{14} \text{ cm}^{-2}$ , which seems at least one order of magnitude too large for the surface-state density of GaAs.

To summarize our views on this mechanism, although the temperature dependence of Eq. (7) seems to satisfactorily fit our data (and those of others) over a large temperature range, still we feel that the required magnitudes of the various parameters cannot be explained. It may be that a combination of band conduction, which seems to always dominate at the higher temperatures, and surface conduction, which may dominate at the lower temperatures, can give a temperature dependence like that seen in Eq. (7), over a rather large temperature range. Conversely, there may be an entirely different mechanism responsible for the low-temperature conduction.

#### E. Surface charge-transfer effects

Even though the surface states may not carry current, still they can indirectly modify the sample conductance by depleting or enhancing the free-carrier concentration in a region of depth  $w$  below the surface. A solution to Poisson's equation can be written as follows<sup>1</sup>:

$$-w \frac{d\mathcal{E}(w)}{dz} + \mathcal{E}(w) - \mathcal{E}(0) = \frac{e^2}{\epsilon} \int_0^w z(N_{\text{EL2}}^+ - N_{\text{AS}}^- + p - n) dz, \quad (8)$$

where the depth  $w$  at this point is arbitrary, and it is assumed that EL2 is the dominant deep donor and that the shallow donor concentration  $N_{\text{DS}}$  obeys  $N_{\text{DS}} \ll N_{\text{AS}}$ , which is usually the case. Also,  $\mathcal{E}$  here denotes electron energy, not potential. In the depletion approximation we assume that  $w$  represents a sharp boundary between the space-charge and neutral regions, so that just beyond  $w$ ,  $d\mathcal{E}(w)/dz = 0$  and  $N_{\text{EL2}}^+$

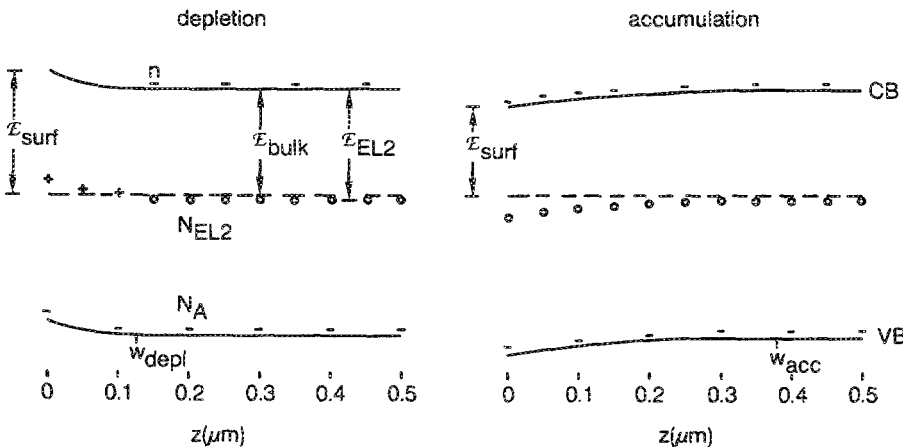


FIG. 2. A schematic representation of the valence band, conduction band, EL2, and acceptor energies as a function of depth for two different conditions: depletion and accumulation. The surface is at  $z = 0$ . The minus signs, plus signs, and circles stand for negative, positive, and neutral charges, respectively.

$-N_A^- + p - n = 0$ ; also  $p - n \ll N_{EL2}^+ - N_A^-$ , and  $N_A^- \approx N_A$ , everywhere, for SI GaAs. In Fig. 2 we depict two possible situations: surface "depletion," for which  $\mathcal{E}_{surf} > \mathcal{E}_{bulk}$ ; and surface "accumulation," for which  $\mathcal{E}_{surf} < \mathcal{E}_{bulk}$ . For the depletion case,  $N_{EL2}^+ \approx N_{EL2}$  for  $0 \leq z < w_d$ , and  $N_{EL2}^+ = 0$  for  $z > w_d$ . Then a simple integration of Eq. (8) gives

$$w_{depl} = \left( \frac{2\epsilon(\mathcal{E}_{surf} - \mathcal{E}_{bulk})}{e^2(N_{EL2}^+ - N_A)} \right)^{1/2}. \quad (9)$$

For the accumulation case,  $\mathcal{E}_{bulk} > \mathcal{E}_{surf}$ , and

$$w_{acc} = \left( \frac{2\epsilon(\mathcal{E}_{bulk} - \mathcal{E}_{surf})}{e^2 N_A} \right)^{1/2}. \quad (10)$$

Typical values of  $N_{EL2}^+$  and  $N_A$  (often carbon) are  $1 \times 10^{16}$  and  $1 \times 10^{15} \text{ cm}^{-3}$ , respectively. Then,  $\mathcal{E}_{bulk} \approx 0.61 \text{ eV}$ , just above  $E_{EL2}$ , which is estimated at  $0.65 \text{ eV}$  (296 K). Suppose  $\mathcal{E}_{surf} \approx 0.71 \text{ eV}$ ; then  $w_{depl} \approx 0.12 \mu\text{m}$ . On the other hand, suppose  $\mathcal{E}_{surf} \approx 0.51 \text{ eV}$ ; then,  $w_{acc} \approx 0.38 \mu\text{m}$ . Each of these hypothetical cases involves a surface band bending of  $|\mathcal{E}_{surf} - \mathcal{E}_{bulk}| \approx 0.1 \text{ eV}$ , and this leads to a free-carrier concentration difference, at room temperature, of

$$\frac{n_{surf}}{n_{bulk}} \approx e^{\pm 0.1/0.0225} \approx (50.5) \pm 1. \quad (11)$$

This carrier concentration difference is appreciable, and would usually be measurable in the accumulation case, even though the accumulation layer is only a few tenths of a micrometer thick.

One possible way to modify surface potential is to change the ambient. Lester, Kim, and Streetman<sup>10</sup> have measured resistance changes in *n*-type GaAs successively exposed to  $N_2$  and  $O_2$ . Their conclusion was that  $O_2$  tended to *flatten* the bands at the surface, thus leading to a decrease of the depletion depth and an increase of sheet carrier concentration. To study these effects, we exposed an undoped, SI GaAs to four different ambients, vacuum, air, helium, and nitrogen, without mounting or demounting the sample in between ambient changes. The results are shown in Fig. 3. Note that the percentage changes in the electrical properties as a function of ambient are very small, and not outside of measurement uncertainty. In this sample, therefore, we see no obvious changes in  $p$ ,  $\mu$ , or  $n$  due to changes in ambient, although other SI GaAs samples may well behave differently.

However,  $n$  here appears to be decreasing slowly as a function of *time*, regardless of ambient. This effect has also been observed in other samples, and could be due to slow removal of an adsorbate, or to slow equilibration of electron and hole traps. However, if an adsorbate is involved, the increased conduction must be due to its effects on surface potential, and not on direct conduction in the adsorbate; for, if the latter were true, the mobility would be expected to also change with time, which is not observed in Fig. 3.

### III. SUMMARY

We have considered several possible reasons for deviations in measurements of the bulk electrical properties of SI GaAs. Other than the necessity of removing obvious surface

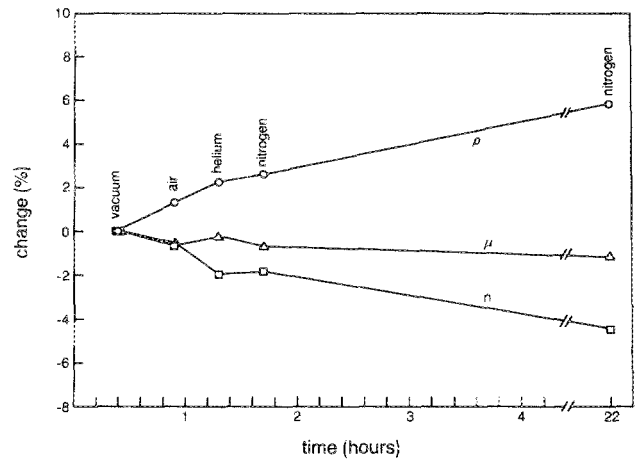


FIG. 3. Changes in  $\rho$ ,  $\mu$ , and  $n$ , as a function of time after being placed in vacuum, for an undoped, semi-insulating GaAs sample.

contaminants, normally accomplished by using degreasing solvents, the one firm conclusion of this study is that a few micrometers of surface material should also be removed, since this material often is more conductive than that of the bulk material, due to sawing and polishing damage. Finally, surface states can affect conduction in two ways: (1) through tunneling conduction in the states themselves, and (2) through the effects of the states on surface potential. It was concluded that the tunneling conduction, if it is at all significant, cannot be explained on the basis of present theory. Also, the surface potential does not seem to be affected by ambient, in the samples we have studied, but it is likely that factors other than ambient may well affect it. It was concluded that only a small change in surface potential is necessary to produce a significant change in the measured electrical properties, as long as  $\mathcal{E}_{surf} < \mathcal{E}_{bulk}$ .

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