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Fuzzy Logic Control of a Switched-Inductor PWM DC-DC Buck Converter in CCM

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Fuzzy Logic Control of a Switched-Inductor DC-DC Buck Converter in CCM

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I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Terry Kolakowski ENTITLED Fuzzy Logic Control of a Switched-Inductor PWM DC-DC Buck Converter in CCM BE ACCEPTED IN PARTIALFULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Engineering

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Abstract

Kolakowski, Terry. M.S.Egr., Department of Electrical Engineering, Wright State University, 2009. *Fuzzy Logic Control of Switched-Inductor DC-DC Buck Converter in CCM*

Modern electronics are operating at lower voltages with higher currents, requiring power converters to deliver these requirements efficiently. In this thesis, a switch-inductor buck converter is designed for the required specifications; and for the selected design, component losses and efficiency are calculated. A MATLAB/Simulink model is constructed, and tested in the presence of load and source disturbances to show the converter cannot maintain the desired output voltage when the disturbances are applied.

A fuzzy logic PID controller is designed to regulate the duty cycle of the converter to control the output voltage. Control surfaces are designed for proportional, integral, and derivative gains of the fuzzy PID controller. The compensated power converter is tested using the Simulink model in the presence of the disturbances, and it is shown that the fuzzy controller is capable of keeping the power converter output voltage within the operating requirements, while improving system speed and stability.

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1 Introduction

Power converters provide a highly efficient means to deliver a regulated voltage from a standard power source [1]. However, circuit trends are requiring voltage/current requirements outside the efficient range of most classical conveters; the duty cycle is below 0.1 or above 0.9, and therefore new conveter topologies must be developed [2]. In addition, these conveters/regulators are susceptable to various disturtances from the attached load or the power source. These disturbances, if not controlled may damage or shutdown devices attached to the converter [1],[3].

In recent years, the use of digital control schemes has become increasingly popular to control these converters [4]-[7]. These digital control schemes incorperate microcontrollers to analyze the input signal and produce the appropriate output signal. The popularity of using microcontrollers arises from their immunity to component variations, compatiblity with other digital systems, and their ability to incorperate advanced control schemes.

Fuzzy logic control provides a method of nonlinear control using piece-wise linear functions to apply varying gains depending on the error signal between the desired output and the actual output. The fuzzy logic controller is advantageous over classical controls where the gains are fixed. A fuzzy logic controller allows the proportional, integral, and derivative gains to be adjusted to work optimally to control the system and therefore make it a suitable for control of buck converter [8]-[11].

1.1 Background

1.1.1 Classical Buck

The classical buck converter is a basic step down DC-DC converter circuit which is used to provide a constant voltage from a standard source (12V, 24V, etc). The circuit contains two switches, either one transistor and one diode or a pair of transistors, to reduce the standard voltage to the desired value. When using a second transistor in place of a diode, the circuit is using synchronous rectification. In addition to the switches, an inductor is used to maintain the desired current and a capacitor is used to maintain the required output voltage. This buck converter uses pulse width modulation (PWM), a method whereby a duty cycle pulse is used to activate the switches to pass power from the source to load. Only one of the switches is active at a time. When the duty cycle pulse from the primary switch (transistor) is high, the source charges the inductor and capacitor, and when the duty cycle pulse of the primary switch is low, the diode/transistor (secondary switch) continues the flow of electrons through the circuit and discharges the the reactive components. Overall, the average power transferred within the circuit is related the duty cycle. The classical buck circuit has the following gain

$$\frac{V_O}{V_I} = D \tag{1.1}$$

where V_I is the input voltage, V_O is the output voltage, and D is duty cycle. The classical buck converter is capable of reliable operation between a duty cycle of 0.1

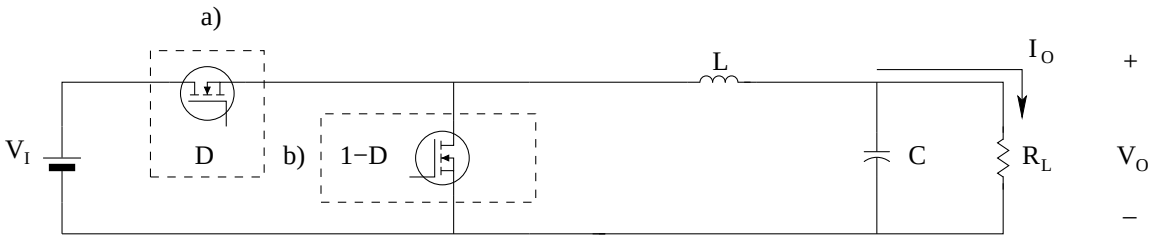

Figure 1: Synchronous buck converter with a) primary switch and b) secondary switch.

and 0.9. Outside these extremes, the operation is unreliable since heavy losses due to swtiching decreae the efficiency of the converter.

1.1.2 Switched-Inductor Buck

In order to combat the need for the extreme duty cycles, higher order topologies have been utilized. Multistage buck converter circuits are capable of having more median duty cycles. The quadratic buck circuit, for example, has the transfer function

$$\frac{V_O}{V_I} = D^2 \ . \tag{1.2}$$

However, the losses caused by the increase in parasitic resistances due to the increase in components, counteracts the increase in efficiency gained by having a more median duty cycle. In order to compensate for the need of a more meadian duty cycle and the parasitics losses,the switched inductor topology in figure 2 is examined. The switched inductor topology has the transfer function

$$\frac{V_O}{V_I} = \frac{D}{2-D} \ . \tag{1.3}$$

The switched-inductor topology utilizes the same number of components as the traditional quadratic circuit but has less current flow through the inductor inductors and switches within the circuit. The decrease in the current flow through these components leads to less losses due to parasitic resistances. In addition,the size of the inductor is reduced because less energy storage is required. To confirm these char-

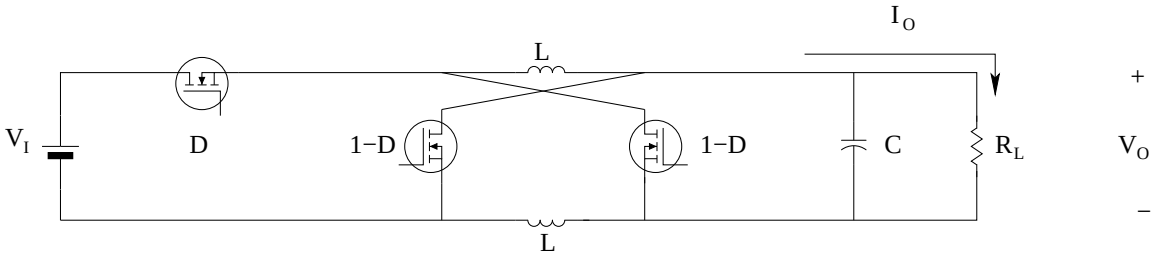

Figure 2: Switched-inductor buck.

acteristics DC analysis of the system is performed. Similar to the operation of all PWM circuits in continuous conduction mode (CCM), whereby the energy transfer from the inductor never goes to zero during switching cycles, the operation of the switched-inductor buck can be divided into two stages; the first stage when the primary switch is active and the second stage when the secondary switches are active. The first stage occurs when the duty cycle pulse from the pulse width modulator is high on the primary switch, $0 \leq t \leq DT$ where t is time, T is the period, and D is the duty cycle.The second stage occurs when the duty cycle pulse is low and occurs when $DT \leq t \leq T$.

During the first time interval, $0 \leq t \leq DT$, the inductors are in series. Therefore, when steady-state is reached, the current through the load is equal to the current flowing through the inductors.

$$I_{O1} = I_L = I_{L1} = I_{L2} = V_I/R_L \tag{1.4}$$

where I_{O1} is the output current from $0 \leq t \leq DT$, I_{L1} and I_{L2} are the currents through the inductors, V_I is the DC input voltage, and R_L is the load resistance.

During the second time interval, $DT \leq t \leq T$, the inductors are in parallel. Therefore, when steady-state is reached,the current through the load is sum of the currents in the inductors.

$$I_{O2} = I_{L1} + I_{L2} = 2I_L = -V_O/R_L \tag{1.5}$$

The total current through the load is the summation of the current through the two stages. Therefore, the relationship between the inductor current and the load current is

$$\begin{aligned} I_O &= I_{O1}D + I_{O2}(1-D) \\ &= I_L D + 2I_L(1-D) \end{aligned}$$

$$I_O = (2 - D)I_L \tag{1.6}$$

Substituting the values of I_{O1} and I_{O2} from equations (1.4) and (1.5) respectfully, we solve from for the output current in terms of the duty cycle, input and output voltages, and load resistance is given by

$$I_O = \frac{V_I D}{R_L} - \frac{(1 - D)V_O}{R_L} \tag{1.7}$$

Now, using Ohm's law and value of I_o from (1.7), the output voltage can be written as

$$V_O \;\; = \;\; \frac{V_I D}{2 - D} \tag{1.8}$$

Therefore the DC voltage gain of the system, M_v, in terms of the duty cycle is given by

$$M_v = \frac{V_O}{V_I} = \frac{D}{2 - D} \; . \tag{1.9}$$

Within this thesis, the ratio $\frac{D}{2-D}$ is refered to as the duty cycle control ratio, A.

DC analysis has provided the gain of the converter with respect to the duty cycle, (1.9) as well as the relationship between the inductor current and output current, (1.6). These characteristics differentiate the switched-inductor buck converter from the classical buck conveter. Taking into account these differences, the converter can be modeled and designed to meet perfromance criteria.

1.2 Thesis Objective

This thesis presents the design, modeling, and fuzzy logic control of a switched-inductor buck converter. The switched-inductor buck is designed from a set of required specifications, and then modeled to construct a block diagram within simulink. The overall performance is evaulated by implementing disturbances in the form of a connection to a 12 V DC standard source, a 1 A step change in the load current,

and 1 V step change in the source using MATLAB/simulink. A fuzzy logic controller then is designed to reject the disturbances from the change in the source and load as well as optimize the response from the connection to the source while maintain the operating parameters designated by the design requirements.

2 Design of Switched Inductor Buck

2.1 Design Parameters

The converter, in this thesis, is designed for CCM operation, and needs to operate from a 12 ± 3 V DC source. The output voltage, V_o, from the converter must be 2 ± 0.1 V with a steady-state ripple of less than 2.5 percent or 0.05 V. The converter is required to maintain output voltage while the output current, I_o, varies between 1 A and 10 A.

2.2 Component and Device Modeling for Design

The design of the swtiched-inductor buck converter requires the selection of two inductors, a capacitor, and two MOSFETS. Before designing for the requirements in section 2.1, the components and devices are modeled according to their impedence characteristics. These impedence charactertisics effect the overall performance of the converter as well as the steady-state ripple voltage.

2.2.1 Inductor Modeling

The inductors provide the magnetic storage element in the buck circuit. However, the inductor contain a parasitic equivalent series resistance (ESR), due to nature of the material from which the inductor is constructed and any connection leads from the inductor to other parts of the circuit. Therefore, a real inductor is modeled as a ideal inductor with a parasitic resistance, r_l, in series as shown in figure 3. The value of r_l affects the charging/discharging rate of the inductor by

$$\tau_L = \frac{L}{r_l} \tag{2.1}$$

where τ_L is the time constant of the inductor in seconds.the charging curve of the inductor current in amps with respect to time. A inductor with a high inductance

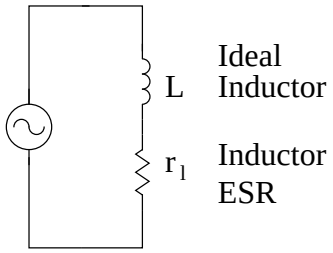

Figure 3: Inductor modeled as an ideal inductor with equivalent series resistance r_l.

value is capable of maintaining the current but has heavy losses due to the ESR and is slow to charge due to changes in the current. A small inductor, however, is able to charge and discharge quickly and has a lower ESR. However, it causes a high ripple in the output voltage. Therefore, a trade-off must occurs between efficiency and output ripple. The inductor chosen satisfies both conditions.

2.2.2 Capacitor Modeling

The capacitor provides the electrical energy storage element of the circuit. However, losses occur within the capacitor due to leakages across the dielectric boundary caused by imperfections in the material. The leakage equates to an ESR. Therefore, a real capacitor is modeled as an ideal capacitor with a parasitic resistance, r_c, in series as shown in figure 4. The ESR effects the time constant of the charging/discharging of

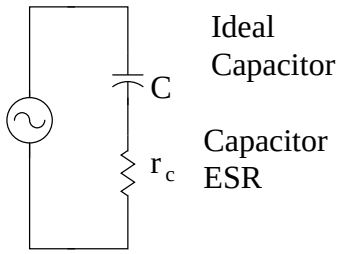

Figure 4: Capacitor modeled as ideal capacitor with equivalent series resistance r_c.

the capacitor by

$$\tau_C = Cr_C \tag{2.2}$$

where t is time in seconds and τ_C is the time constant of the capacitor. In addition, the ESR causes a ripple in the output voltage. The capacitor chosen meets both capacitance and ESR requirements.

2.2.3 MOSFET Modeling

The N-channel MOSFETs are used to provide the switching network for the switched-inductor buck circuit. While the MOSFETs are active, they contain an on-resistance, r_{DS}, which inhibits current flow and produces losses within the system. Therefore, the model for the MOSFET contains a perfect switch with resistance of r_{DS} in series as seen in figure 5.

2.3 Design

The power output of the system is based upon the the required output voltage of the system and the output current requirements. In addition, the maximum and minimum load are calculated using the required voltage and current.

$$P_{Omax} = V_O I_{Omax} = 20W \tag{2.3}$$

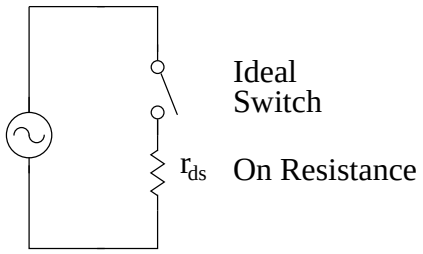

Figure 5: MOSFET modeled as a switch with on-resistance r_{DS}

$$P_{Omin} = V_O I_{Omin} = 2W \tag{2.4}$$

$$R_{Lmin} = \frac{V_O}{I_{Omax}} = 0.2\Omega \tag{2.5}$$

$$R_{Lmax} = \frac{V_O}{I_{Omin}} = 2\Omega \tag{2.6}$$

The minimum, nominal, and maximum values of the DC voltage gain are determined using the range of input voltages and the required output votlage.

$$M_{V\ DCmin} = \frac{V_O}{V_{Imax}} = 0.1333 \tag{2.7}$$

$$M_{VDCnom} = \frac{V_O}{V_{Inom}} = 0.1667 \tag{2.8}$$

$$M_{VDCmax} = \frac{V_O}{V_{Imin}} = 0.2222 \tag{2.9}$$

The duty cycle requirements are calucated from the DC voltage gain. However, since all of the components contain parasitic losses, the duty cycle is adjusted by an assumed efficiency which is later verified. Assume the effiecncy η is 0.95.

$$D_{min} = \frac{2M_{VDCmin}}{\eta(M_{VDCmin} + 1)} = 0.2476 \tag{2.10}$$

$$D_{nom} = \frac{2M_{VDCnom}}{\eta(M_{VDCnom} + 1)} = 0.3008 \tag{2.11}$$

$$D_{max} = \frac{2M_{VDCmax}}{\eta(M_{VDCmax} + 1)} = 0.3825 \tag{2.12}$$

Selecting the switching frequency, f_s, of the PWM to be 100 kHz, the minimum total inductance value required is

$$L_{Tmin} = \frac{R_{Lmax}(1 - D_{min})}{f_s} = 15.048\mu H \frac{2(1 - 0.2476)}{100 * 10^3} = 15.048\mu H \ . \tag{2.13}$$

Therefore the minimum inductance required for each inductor is

$$L_{min} = \frac{L_{Tmin}}{2 - D_{max}} = 9.303\mu H \ . \tag{2.14}$$

Cooper Electronic Technologies provides the CTX20-7-52M-R header mounted toroidal inductor which has an inductance, L, of 20 μH, an ESR, r_l, of 0.0110 Ω, and is capaple of delivering 11.4 A @ 75°C ambient without core losses.

The maximum inductor ripple current is

$$\Delta i_{Lmax} = \frac{V_O(1 - D_{min})}{f_s L} = 0.7524A \ . \tag{2.15}$$

In order to achieve the minimum ripple requirement, V_r of 0.05 V, the ESR of the output capacitor should be

$$r_{cmax} = \frac{V_r}{\Delta i_{Lmax}} = 0.0665\Omega \ . \tag{2.16}$$

Substituting (4.14) into (4.15), the minimum required capacitance is

$$C_{min} = \frac{1 - D_{min}}{2 f_s r_{cmax}} = 56.571\mu F \ . \tag{2.17}$$

NIC Components Corp. provides a surface mount ploymer-tantalum capacitor which can be used to meet both the capcitance and ESR requirements. The NTP227M4TRV(12)F has capacitance value, C of 200 μF and ESR, r_c of 12 $m\Omega$.

2.4 Device Stresses and Losses

The MOSFETs chosen for the swithching network must maintain operating condition under the voltage and current stresses from the power source, inductors, capactior, and load. The MOSFET chosen is the IRF3711z, provided by International Rectifier. The ifr3711z has a maximum drain-to-source voltage, V_{DS}, of 20 V, maximum

gate-to-sourve votlage, V_{GS}, of $\pm$ 20 V, maximum drain current, I_D, of 92 A @ 25°C, output capacitance, C_o, of 680 pF, and an on-resitance, r_{DS}, of 6.0 mΩ.

The voltage and current stresses on the MOSFETs can be defined as

$$V_{SMmax} = V_{DMmax} = V_{Imax} \ = 15V \tag{2.18}$$

and

$$I_{SMmax} = I_{DMmax} = \frac{1}{2}(\frac{I_{Omax}}{2 - D_{max}} + \frac{\Delta i_{Lmax}}{2}) = 3.279A \ . \tag{2.19}$$

The power loss in the primary MOSFET due to the on-resistance and switching is

$$P_{r_{DS1}} = D_{min} r_{ds1} (\frac{I_{Omax}}{2 - D_{max}})^2 \ = 0.0568W \tag{2.20}$$

and

$$P_{sw1} = f_s C_o V_{Imax}^2 \ = 0.0153W \ . \tag{2.21}$$

The power loss in the secondary MOSFETs due to the on-resistance and switching is

$$P_{r_{DS2}} = (1 - D_{min}) r_{ds2} (\frac{I_{Omax}}{2 - D_{max}})^2 \ = 0.1725W \tag{2.22}$$

and

$$P_{sw2} = f_s C_o V_{Imax}^2 \ = 0.0153W \ . \tag{2.23}$$

The power loss attributed to the ESR of the inductor is

$$P_{rLmax} = r_L (\frac{I_{Omax}}{2 - D_{max}})^2 \ = 0.4204W \ . \tag{2.24}$$

The power loss attributed to the ESR of the capacitor is

$$P_{rC} = \frac{r_C V_O^2 (1 - D_{min})^2}{12 f_s^2 L^2} \ = 0.05661W \ . \tag{2.25}$$

Therefore, the total power loss through the entire circuit is

$$P_T = P_{rDS1} + P_{sw1} + 2P_{rDS2} + 2P_{sw2} + 2P_{rL} + P_{rC} \ = 1.345W \ . \tag{2.26}$$

Subsituting (2.3) and (2.26), the total efficiency of the ciruit is given by

$$\eta = \frac{P_{Omax}}{P_{Omax} + P_T} = 0.94 \ . \tag{2.27}$$

Using the components selected from the modeling and design procedure, the complete converter circuit can be constructed. After construction, the complete circuit needs to be modeled and tested to determine if the output requirement can be maintained due to variances in the source and load.

3 Modeling and Analysis of Switched-Inductor Buck Converter

3.1 Modeling of Switched-Inductor Buck Converter

The switched-inductor buck converter has three variable parameters: the change in source voltage, v_i, the change in the load current, i_o, and the change in the duty cycle control raito, a. Each of these parameters can be defined as an input to converter while the output voltage, V_o, can be defined as the output of the converter. The result, as shown in figure 6, is a block diagram divided into three separate transfer functions.

The load current and source voltage, while bounded, are free to change and are treated as disturbances. The duty cycle control ratio can be adjusted to compensate for changes in the load and source, and thus it is a controllable parameter. The output voltage-to-input voltage transfer function is defined as M_v; the output voltage-to-duty cycle ratio transfer function is defined as T_{pa}; and the output voltage-to-load current transfer function is defined as Z_o.

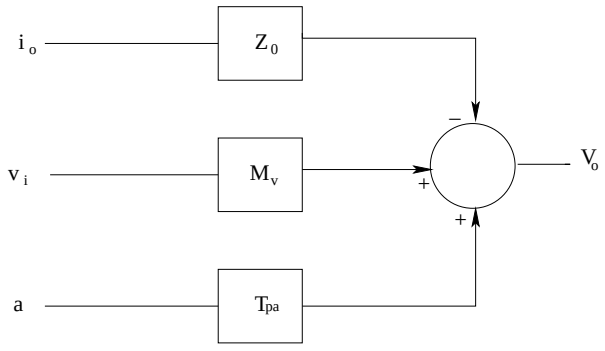

Figure 6: Open-Loop block diagram of swtiched-inductor buck

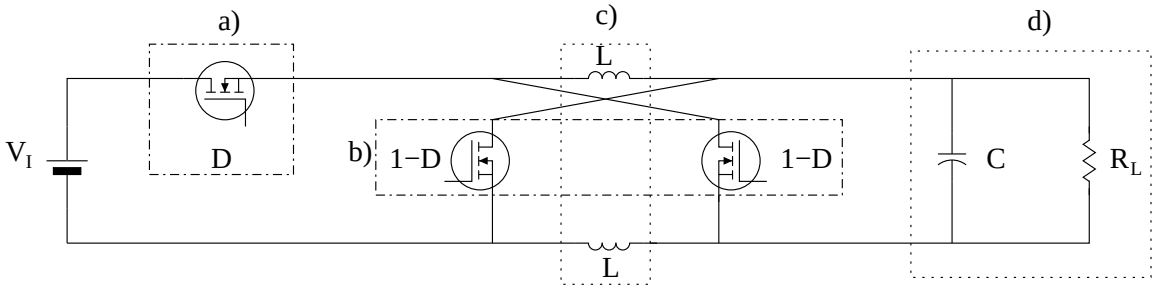

Figure 7: Switched-Inductor Buck with a) primary switch branch, b) secondary switch branches, c) inductor branches, and d) output branch.

3.1.1 Model Reduction

The circuit model in figure 7 contains four types of branches; a primary switch branch, secondary switch branches, inductor branches, and the output branch. The average current through these branches is not equal. However, all the currents can be related to the inductor current. The relationship between the output current and inductor current is stated in (1.6). The primary switch branch current, I_{S1}, corresponds to the inductor current I_L by

$$I_{S1} = \frac{I_L}{D} \tag{3.1}$$

The secondary switch branch current, I_{S2}, corresponds to the inductor current by

$$I_{S2} = \frac{I_L}{1-D} \tag{3.2}$$

Using the relationships between the currents in (3.1) and (3.2), the parasitic resitances from the primary switch branch, secondary switch branches, and inductor branches are combined into one total resistance r_T by

$$r_T = r_{ds1}D + 2r_L + (1-D)2r_{ds2} \ = 0.0322\Omega \tag{3.3}$$

However, since there are two inductors, the total parasitic resitance of these components is divided evenly between the inductors. The resulting circuit model with the combined parasitics from the switches and inductors is in figure 8.

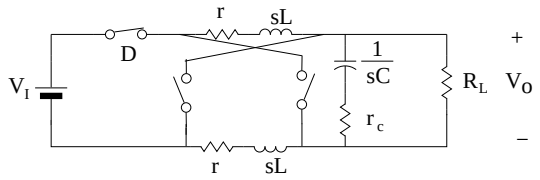

Figure 8: Reduced circuit model with combined parasitic resitances, r.

3.1.2 Output Voltage-to-Input Voltage Transfer Function

The output voltage-to-input voltage transfer function can be measured by reducing the change in duty cycle and load change to zero. Once this is accomplished, the system is reduced to a single-input single-output (SISO) system which can seen in figure 9. The system can be split into two parts: the two inductor branches and the output branch. Recall, the relationship between the inductor current and output current is described in (1.6). The impedance of the to be inductor branch is defined to be

$$Z_1(s) = \frac{sL + r}{2 - D} \tag{3.4}$$

and the impedance of the output branch is defined as

$$\begin{aligned} Z_0(s) &= (\frac{1}{sC} + r_c)||R_L & (3.5)\\ &= \frac{R_L(sCr_c + 1)}{C(r_c + R_L)s + 1} & (3.6) \end{aligned}$$

Therefore, the small signal transfer function $\frac{v_o(s)}{v_i(s)}$ is

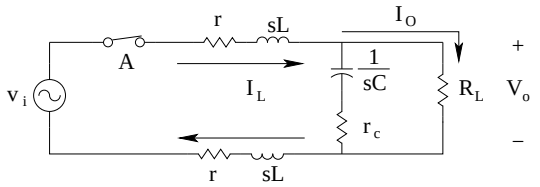

Figure 9: Circuit model to determine V_o-to-v_i transfer function.

$$\frac{v_o(s)}{v_i(s)} = \frac{Z_0(s)}{2Z_1(s)+Z_0(s)} \tag{3.7}$$

$$= \frac{\frac{(2-D)R_L(Cr_cs+1)}{2CL(r_c+R_L)}}{s^2+\frac{2C(r_c+R_Lr+C(2-D)r_cR_L+2L}{2CL(r_c+R_L)}s+\frac{2r+(2-D)R_L}{2CL(r_c+R_L)}} \tag{3.8}$$

The transfer function including the nominal DC transfer function, M_{vDCnom} is

$$\frac{V_o(s)}{v_i(s)} = \frac{v_o(s)}{v_i(s)}M_{vDCnom} \tag{3.9}$$

$$= \frac{v_o(s)}{v_i(s)}\frac{D}{2-D} \tag{3.10}$$

3.1.3 Ouput Voltage-to-Duty Cycle Control Ratio Transfer Function

The output voltage-to-duty cycle control ratio transfer function can be measured by reducing the change in the input voltage and change in the load current to zero. This produces another SISO system. Recall from chapter 1, the duty cycle control ratio is defined as

$$A = M_v = \frac{D}{2-D} \tag{3.11}$$

Since the duty cycle control ratio is a non-linear quantity, the change in ratio is defined as

$$a = \frac{D+d}{2-D-d} - \frac{D}{2-D} \tag{3.12}$$

where d is the change in the duty cycle. As stated in section 3.1.2, the system can be broken down into an inductor branch with impedence, Z_1, and an output branch with the impedence, Z_0. Therefore, the small signal output voltage-to-duty cycle control ratio transfer function can be

$$\frac{v_o(s)}{a(s)} = \frac{Z_0(s)}{2Z_1(s)+Z_0(s)} = \frac{v_o(s)}{v_i(s)} \tag{3.13}$$

The transfer function, T_{pa}, which includes the nominal input voltage, V_{Inom}, is

$$\frac{V_o(s)}{a(s)} = \frac{v_o(s)}{a(s)} V_{Inom} \tag{3.14}$$

3.1.4 Output Voltage-to-Ouput Current Transfer Function

The output voltage-to-output current transfer function can be measured by reducing the change in the input voltage and change in the duty cycle control ratio to zero. As stated in the section 3.1.2, the system can be broken down into an inductor branch with impedence, Z_1, and an output branch with the impedence, Z_0. The transfer function of the output voltage-to-output current, Z_O, is defined as

$$\frac{V_o(s)}{i_o(s)} = 2Z_1(s)||Z_0(s) \tag{3.15}$$

$$= \frac{\frac{2CLr_cR_Ls^2+(2Cr_cR_Lr+2LR_L)s+2R_Lr}{2CL(r_c+R_L)}}{s^2 + \frac{2Cr_Cr+2CR_Lr-CDr_cR_L+2Cr_cR_L+2L}{2CL(r_c+R_L)}s + \frac{(2-D)R_L+2r}{2CL(r_c+R_L)}} \tag{3.16}$$

3.1.5 Simulink Model of Open-Loop Switched Inductor Buck

The three transfer functions: V_o-to-v_i; V_o-to-a; and V_o-to-i_o, can be combined as in the block diagram in figure 6 and results in the simulink model seen in figure 10. This model has three inputs to the system: the power source, V_i; the change in control ratio, a, and the change in the load current i_o; and one output, V_o. The nomimal values of the source voltage, duty cycle control ratio, and load current are designated as initial conditions within the model.

3.2 Time-Domain Analysis of Open-Loop Switched-Inductor Buck

The time-domain response of the switched-inductor buck converter needs to maintain within operating parameters stated within section 2.1. As the input source varies ± 3 V and loads varies between 1 A and 10 A, the output voltage is required to be 2 ± 0.1 V. Three separate responses are analyzed to see if the switched-inductor buck

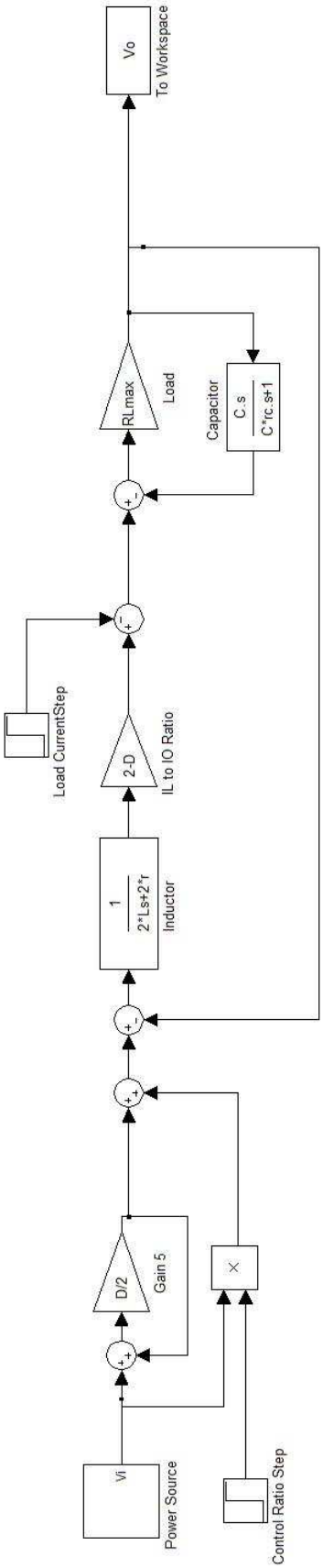

Figure 10: Simulink model of open-loop switched-inductor buck converter.

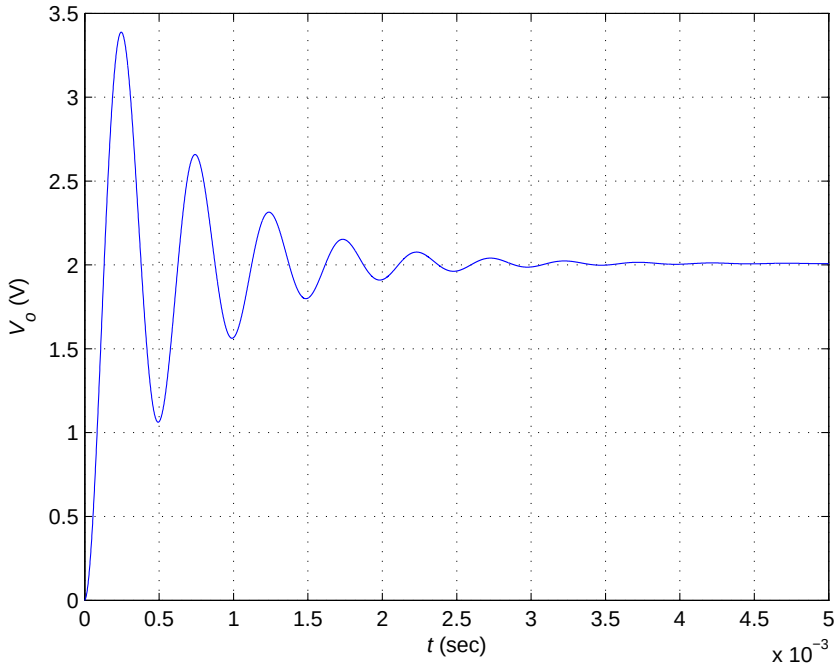

Figure 11: Uncompensated open-loop time-response of buck converter to a 12 V power source with a duty cycle of 0.2891.

remains within the required operating parameters: connection to the 12 V DC power source, 1 A step change in the load, and 1 V step change in the power source.

3.2.1 Response to 12 V DC Power Source

The buck circuit is required to reach a steady-state voltage of 2 V when connected to a 12 V power source. The converter is connected to the source operating under minimum loading conditions: 1 A. The duty cycle is set to 0.2891. From the response shown in figure 11, it can be seen that the output voltage meets the steady-state operating conditions; the steady-state error is 0.4 percent. The transient characteristics are a maximum overshoot of 69.4 percent, a rise time of 88 μsec, and a settling time of 2.75 msec.

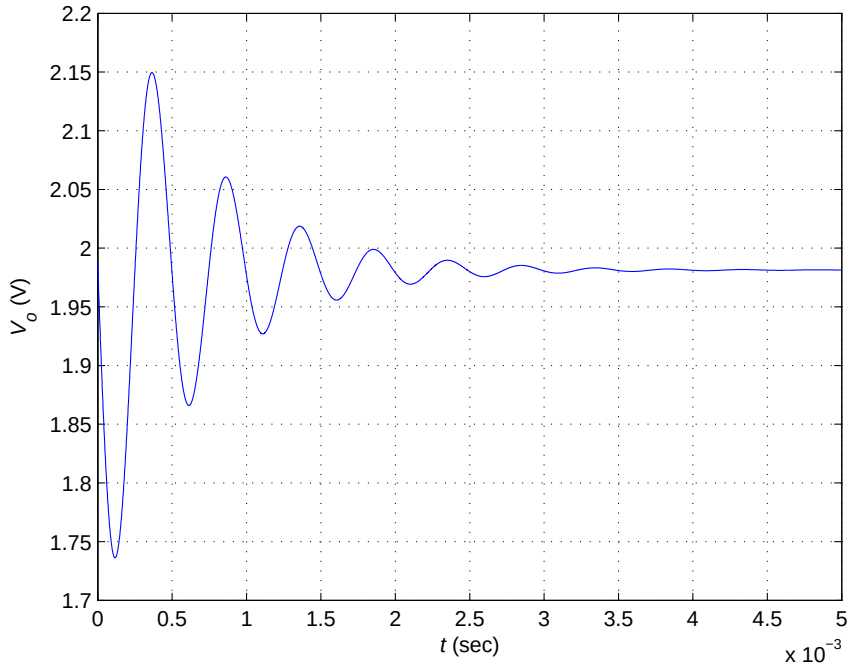

Figure 12: Uncompensated open-loop time-response to a 1 A step change in the load current with a duty cycle of 0.2891.

3.2.2 Response to 1 A Step Change in Load Current

The load is capable of varying between 1 A and 10 A after the system has reached steady-state. The changes in the load alter the operating condition of the system and therefore changes in the load are analyzed to see if the system still remains within operating parameters after a change in the load has occurred. To test the system, a 1 A step change in the load is applied. The response can be seen in figure 12. The output voltage response still meets steady-state operating conditions but the transient operating parameters are not satisfied. The steady-state error is 1 percent. The maximum overshoot is 7.5 percent, and the maximum undershoot is 13.5 percent, which exceed outside the 5 percent requirement.

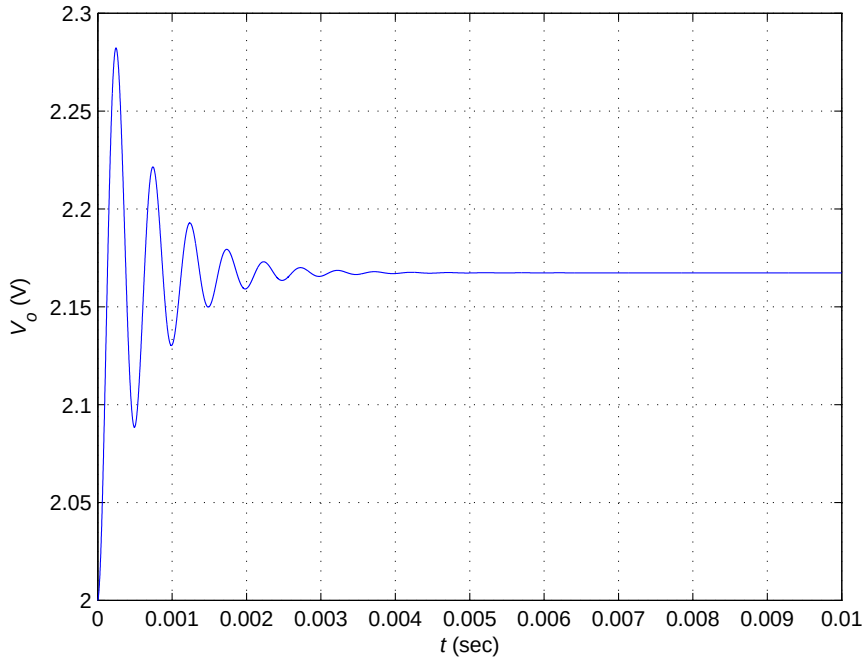

Figure 13: Uncompensated open-loop time-reponse to a 1 V step change in source voltage with a duty cycle of 0.2891

3.2.3 Response to 1 V Step Change in Power Source

The source is capable of varying ± 3 V, and changes in the source voltage affect the operating condition of the system, and therefore can impact the output voltage. To test if the system remains within operating parameters, a 1 V step change is applied to the converter after response from the power source has reached steady-state. The response of the output voltage can be seen in figure 13. The output voltage no longer meets the steady-state operating requirements. The steady-state error is 8.4 percent. In addition, the peak response of the is 2.282 V, which exceeds the 5 percent requirement.

3.3 Closed-Loop Switched-Inductor Buck

The open-loop buck converter is not capable of maintaining the steady-state and the transient operating requirements once disturbances are introduced. Therefore,

closed loop operation of the system is tested to see if operatung requirements can be maintained. Figure 14 shows the closed-loop block diagram for the switched-inductor buck. As shown, two addition devices need to be modeled in simulink to complete the model: an analog-to-digital conveter (ADC) and a digital pulse-width conveter (DPWM).

3.3.1 Analog-to-Digital Converter

The output voltage signal from the coverter is continuous while the DPWM is discrete-time device, therefore the signal must transformed into a discrete signal. A discrete signal is obtained using an ADC. In order to generate the discrete signal, the input signal is connected to one side ,V_{in}, of an analog comparator within the ADC while a time-dependent reference voltage, V_R, is connected to the second input of the ADC. The comparator can be seen in figure 15.

If the input voltage, V_{in}, is is greater than the reference voltage, V_R, the output produces a positive level, logical 1, while if the input voltage is less than the reference voltage, it will produce a low level, logical 0. In order to accurately perform the conversion from an analog to digital signal, the reference voltage is varied to determine which 2^n binary number is closest to the input signal. The reference voltage assumes 2^n values in the form

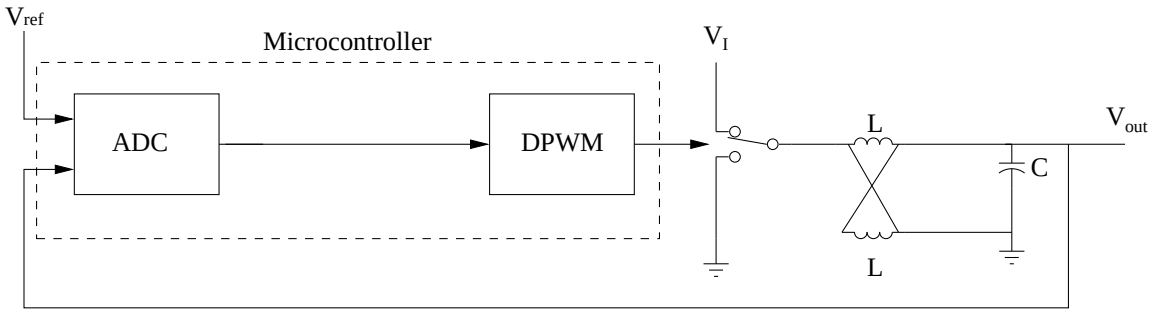

Figure 14: Block diagram of closed-loop switched-inductor buck converter.

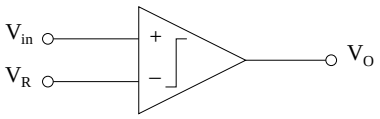

Figure 15: Comparator for analog-to-digital conversion.

$$V_R = V_r \sum_{i=1}^{n} A_i 2^{-i} \tag{3.17}$$

where V_r is the reference voltage, and A_i is the binary coefficients. The value of A_i is chosen so that the difference between the input and output signals is minimum.

$$e = |V_{in} - V_R| = |V_{in} - V_r \sum_{i=1}^{n} A_i 2^{-i}| \tag{3.18}$$

The resolution of the ADC is important since it controls the overall accuracy of the system. The resolution in bits, N_{ADC}, corresponds to the quantization level of

$$\Delta V_{ADC} = V_{in}/2^{N_{ADC}} \tag{3.19}$$

A tweleve bit ADC is chosen to analyze the output voltage and error signal. The range of the ADC is ± 10 V. V_R is chosen to be 10 V, therefore gain of 5 is applied to the output voltage so the error signal is zero when V_o reaches the required 2 V. The ADC converter is also chosen to have a gain of 0.1. Under these conditions, the

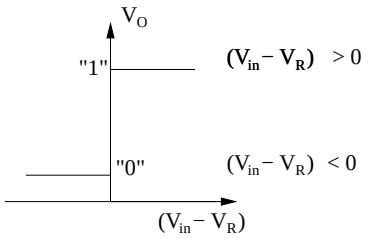

Figure 16: Logic for A/D conversion.

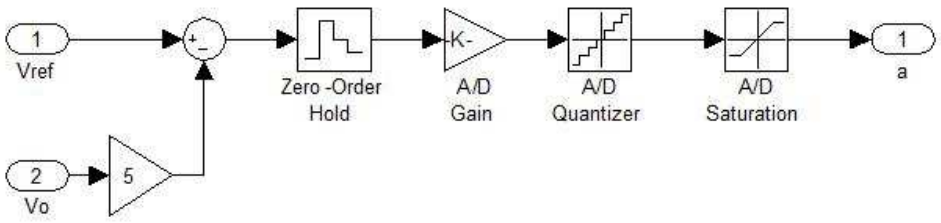

Figure 17: Simulink model of analog-to-digital converter.

overall accuracy is

$$\Delta V_{ADC} = 2 * 10 * 0.1/2^{12} = 4.8828 * 10^{-4} V$$

The ADC is modeled in simulink, shown in figure 17, using a quantizer to set the resolution, ΔV_{ADC}, a zero-order hold to represent the hold betweeen sample times, a saturation to set the upper and lower bounds of [-10, 10], a gain to represent the attenuation of 0.1 of the input signal, and a transport delay to represent any delay caused by the circuit used for actual implementation.

3.3.2 Digtal Pulse Width Modulator

The digital pulse width modulator (DPWM) is the driving circuit which applies the duty cycle to the switching components. The circuit is capaple of produing a duty cycle between 0 ans 1 but duty cycles less the 0.1 and greater than 0.9 are avoidable due to circuit switching losses. The operating frequency of the modulator ranges from the kHz to MHz range. The operating frequency selected for operation of PWM circuits is normally 100 kHz, therfore 100k Hz is chosen for the switching frequency as in section 2.1. In addition, the duty cycle resolution of the converter is based on the of the number of bits in the DPWM.

$$\Delta_{DPWM} = \frac{1}{2^{N_{DPWM}}} \tag{3.20}$$

where N_{DPWM} is number of bits in the DPWM and Δ_{DPWM} is resolution of the DPWM. In addition, the resolution of the DPWM is required to be higher than the

resolution of the ADC in case an integral controller is needed.

$$\Delta_{DPWM} < \Delta_{ADC} \tag{3.21}$$

In order to acheive the required resolution, the DPWM must have at least 12 bits. Therefore a 12 bit DPWM is used. The resolution of the DPWM is

$$\Delta V_{DPWM} = 1/2^{12} = 2.4414 * 10^{-4} V. \tag{3.22}$$

The DPWM needs higher resolution than the ADC so the integral may converge. A quantization level must exist in the DPWM which cooresponds to zero error range from the ADC. If the resolution is less than or equal to resolution of the ADC, such a level does not exist. The result would be steady-state oscillations around the desired value, seen in figure 18.

The DPWM is modeled in simulink, figure 19, using a saturation to set the limits of the DPWM and a quantizer to set the resolution.

3.3.3 Sampling Rate

The next parameter of the digital control system which is chosen is the sampling frequency. The sampling rate of controller the is determined by finding the highest frequency of the system and applying the nyquist criterion. The nyquist criterion allows for accurate respentation and reconstruction of a sampled signal; it states

$$f_{sa} > 2B \tag{3.23}$$

where f_{sa} is sampling frequency and B is highest frequency of the system. The highest frequency in a PWM circuit is the swtiching frequecy of the DPWM, which is f_s of 100 kHz . Therefore, the minimum sampling frequency is

$$f_{sa} = 2f_s = 200kHz. \tag{3.24}$$

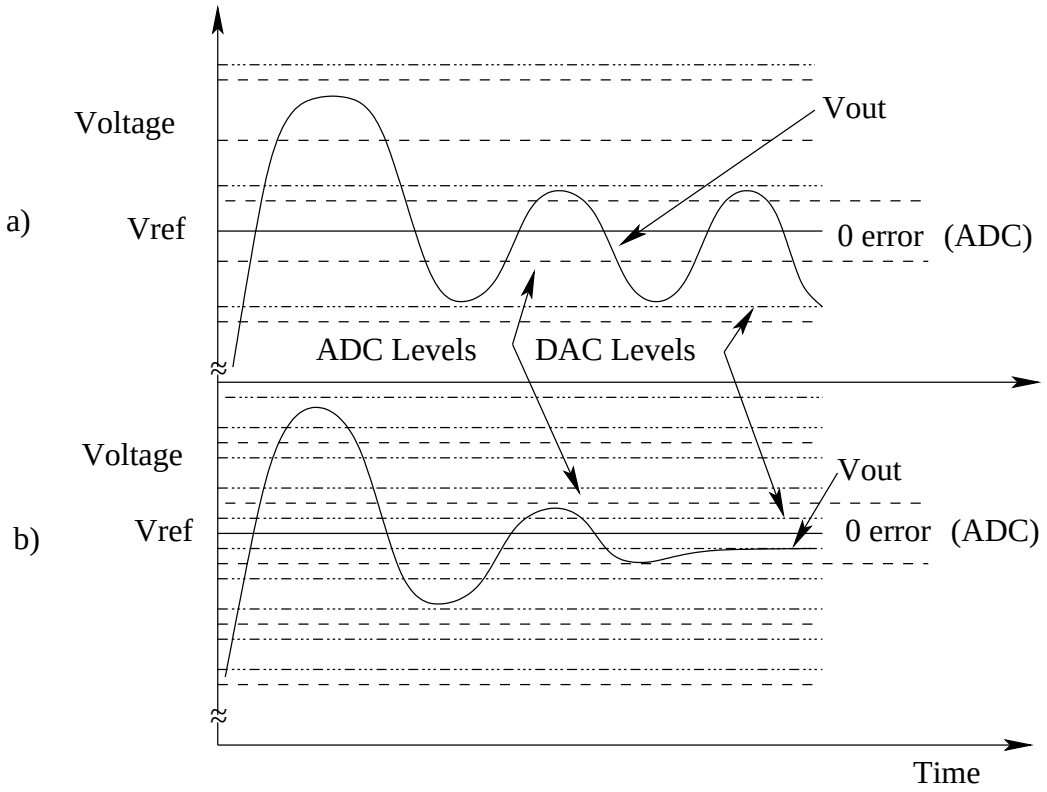

Figure 18: Output of DPWM if a) resolution of DPWM is less than ADC and b) relsolution is greater than ADC

However, to ensure accuracy, a sampling frequecy of 1 MHz is chosen, which is 5 times the nyquist frequency

3.3.4 Closed-Loop Simulink Model

The simulink model of the closed-loop system is seen in figure 20. The model still contains three inputs: the power source, V_i; the change in control ratio, a, and the change in the load current i_o; and one output, V_o. However, the change in the

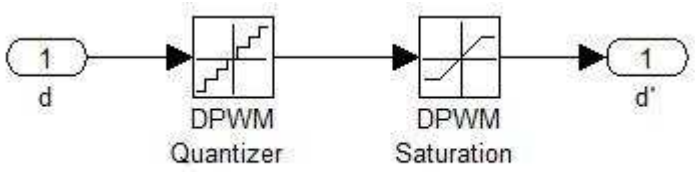

Figure 19: Simulink model of DPWM

change in the control ratio, a, is now being regulated by the error signal between the output voltage and the reference voltage. The resulting system, however, is unstable when tested with the disturbances. Since neither the open-loop or closed-loop system are capable of maintaining the operating requirements designated in section 2.1, a controller must be designed which is capaple of meeting the requirements.

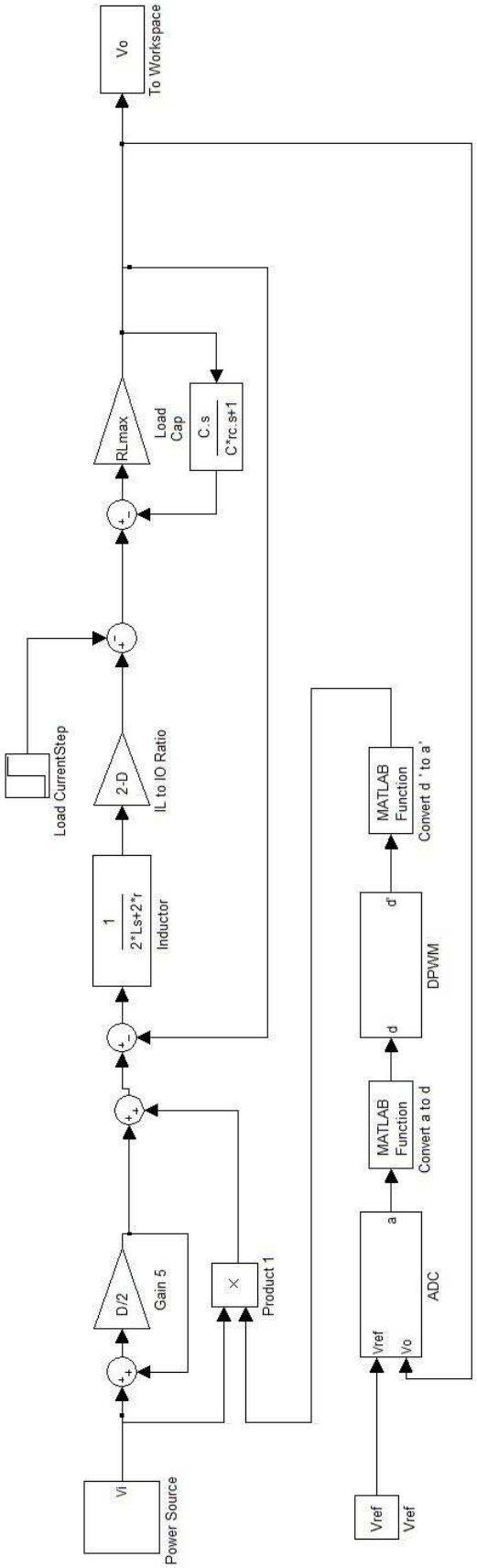

Figure 20: Simulink model of closed-loop switched-inductor buck converter

4 Control Selection

In chapter 3, it is shown that the outout of voltage of the converter cannot be maintain without a controller. Therefore a controller to be selected which is capable of meeting the operating requirements outlined in section 2.1. This can be accomplished by adjusting the duty cycle to not only the appropriate value to meet the steady-state requirements and by adjusting the rate of change of the duty cycle so the transient requirements are met.

Before selecting the controller type, the control configuration is chosen. The control configuration selected is a simple feedback system. The reference signal is the desired output voltage of the converter. The compartor compares the reference signal to the actual output of the converter to create an error signal to work on by the controller. The controller chosen to control the buck converter and keep it within operating conditions is a fuzzy logic PID controller. The fuzzy logic controller uses piecewise linear functions to adjust the proportional, integral, and derivative gains according to the error signal. The adjustment of these gains through a rule base and/or control surface allows the gains only to be applied where they have optimial effect. For example, the derivative is only required when the signal is approaching steady-state to reduce the overshoot, and the integral gain is only needed close to steady state to reduce the error signal to zero. Classical controllers such as the gain conpensator, PI, and PID controllers have constant gains, shown insufficent to control the buck converter.

4.1 Gain Controller

A gain controller cannot control both steady-state error and overshoot, since it only has one controllable parameter. As the gain is increased to meet steady-state error

requirements, the overshoot increases. Both conditions are required and thus this controller is not acceptable

4.2 PI Controller

An analog PI controller is capable of reducing the steady-state error to zero, but stability is sacrificed in order to achieve the steady-state requirement. The loss in stability will increase the overshoot and undershoot, therefore the transient requirement cannot be achieved. Even if the gain is reduced to improve stability, the system slows, which is an undesirable effect.

4.3 PID Controller

An analog PID controller is capable of reducing the steady-state error to zero and maintaining the stability requirements, however, the implementation of the of a analog PID controller is non-desirable. The derivative portion of the controller is required to provide the necessary damping to eliminate the overshoot, however it is highly susceptible to noise and is not reliable to use. Even if implementable, the linear gains force trade-offs between the integral and derivative since both are active in the same proportion independent of the output voltage and error signal.

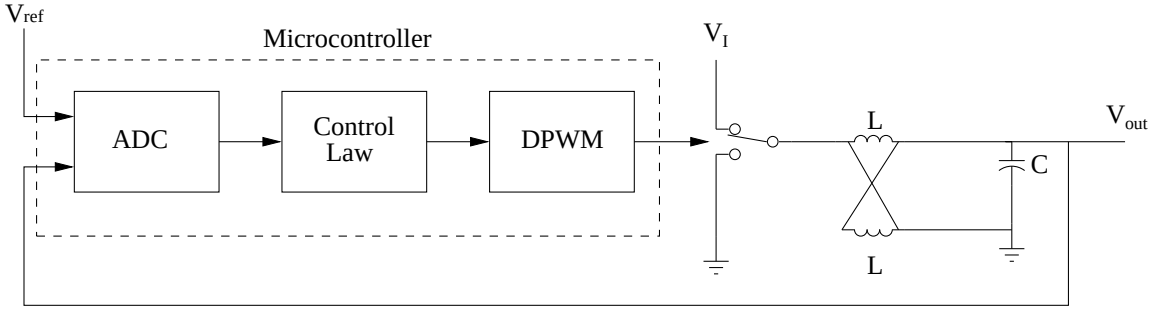

Figure 21: Block diagram of control system for switched-inductor buck converter

4.4 Fuzzy Logic PID Controller

A fuzzy logic PID controller is capable of reducing the steady-state error zero as well as maintaining the transient and stability requirements. The fuzzy controller is capable of producing nonlinear gains, therefore the undesirable effects of the integral and derivative being in constant proportion can be removed, since their effect changes with the output voltage and error signal. In addition, the fuzzy controller can be implemented on a microcontroller, which can isolate the noise from the error signal. In order to implement the fuzzy logic PID control on a microcontroller, the fuzzy logic control law has the follwing form

$$D_{ca}(k+1) = -K_p D_e(k) - K_d[D_e(k) - D_e(k-1)] - K_i D_i(k) + D_{ref}(k) \qquad (4.1)$$

where k is discrete time, $D_{ca}(k)$ is duty cycle control ratio command, $D_e(k)$ is error signal, $D_{ref}(k)$ is reference signal, $D_i(k)$ is state of the integrator given by

$$D_i(k+1) = D_i(k) + D_e(k). \qquad (4.2)$$

In addition, K_p is the gain based on the proportional gain control surface, K_d is the gain based on derivative gain control surface, and K_i is the gain based on the integral gain control surface. The design of these fuzzy logic control surfaces are discussed in Chapter 6. The control ratio command also needs to converted to so the duty cycle is changed to the correct value. In order to change the duty cycle appropritately, the duty cycle command is computed from the control ratio command by

$$D_c(k+1) = \frac{2D_{ca}(k+1)}{D_{ca}(k+1)+1}. \qquad (4.3)$$

where D_c is the duty cycle command and D_{ca} is the duty cycle control ratio command. Now that the fuzzy logic PID controller has been selected to control the converter, it must be designed to meet the operating specifications.

5 Fuzzy Logic

5.1 Overview

Fuzzy Logic is a piecewise linear method of data analysis based on using non-precise values over a range to determine the correct coorespondence to a particular group. Since fuzzy logic is used within the control scheme, explaination of the methodology and terminology is provided.

The fuzzy logic procedure consists of three parts: input fuzzification, input-to-output mapping, and output defuzzification as seen in figure 22. A precise input, such as voltage, current, etc is measured. The input is the fuzzified by mapping it to a set of input membership functions, through a set of inference procedures. Once the membership to the input functions is determined, the input is mapped to the output membership functions according to a rule base. The rule base is unique to the system and based on expert knowledge. The degree of belonging to the output membership functions is determined and is used to produce a precise output through defuzzification or another inference procedure.

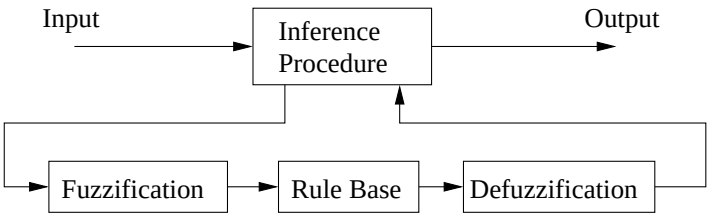

Figure 22: Overview of fuzzy logic procedure.

5.2 Fuzzy Logic Naming Conventions

Fuzzy logic makes use of liguistic variables to determine relationships instead of numerical variable. For example, the variables used within this thesis to express the error voltage are given the names “Negative Big (NB)”, “Negative Medium (NM)”, “Negative Small (NS)”, “Zero (ZO)”, “Postive Small (PS)”, “Positive Medium (PM)”, and “Positive Big (PB)“. In order to determine the which catagory the input belongs, membership functions are defined in order to show the degree of belonging to each particular variable.

5.3 Membership Functions

Membership functions are graphical mappings to determine how close or how much something belongs to a particular group. Membership functions can be almost any arbitrary shape though some common ones are triangular, trapezoidal, or bell-shaped, as in figure 23. The membership functions are combined over the total domain to produce fuzzy sets. The degree which an input belongs to each membership function in the fuzzy sets is determined through the inference procedure.

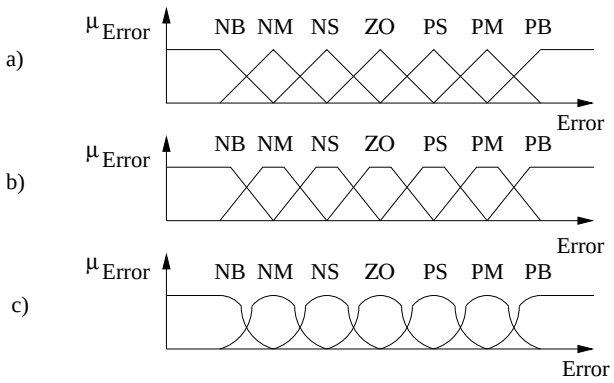

Figure 23: Membership function shapes: a) triangular, b) trapazoidal, and c) bell-shaped.

5.4 Fuzzy Operations

In order to understand the inference procedure, the basic fuzzy operation and the rule base are explained. A set of rules for the interaction of the membership functions within the fuzzy sets is defined since membership function overlap. The basic set rules/operations are union, intersection, and complement. Let A and B be the fuzzy sets in U with membership functions μ_A and μ_B where U is universe of discourse over the range of all possible input values x.

1. Union

   The membership function $\mu_{(A \cup B)}$ of the union $A \cup B$ is defined for all $x \in U$ by

   $$\mu_{(A \cup B)(x)} = max\ (\mu_A(x), \mu_B(x))$$

2. Intersection

   The membership function $\mu_{(A \cap B)}$ of the intersection of $A \cap B$ is defined for all $x \in U$ by

   $$\mu_{(A \cap B)}(x) = min\ (\mu_A(x), \mu_B(x))$$

3. Complement

   The membership of the function $\mu_{\overline{A}}$ of the complement of fuzzy set A is defined for all $x \in U$

   $$\mu_{\overline{A}} = 1 - \mu_A(x)$$

Each of the operations: union, intersection, and complement is graphically displayed in figure 24.

5.5 Fuzzy Rule/Fuzzy Rule Bases

A fuzzy rule is mapping from the input domain to the output domain. The fuzzy rule is typically based on expert knowledge of the system. Usually fuzzy rules follow an

if.. then.. structure, where

If x is A, and y is B, then z is C

where x and y are the input fuzzy variables; z is the output fuzzy variable; A, B, and C are the fuzzy subsets corresponding to the universe of discourse of X, Y, and Z respectfully. Therefore, if there are n fuzzy rules defined as

R1: If x is A1, and y is B1, then z is C1

R2: If x is A2, and y is B2, then z is C2

R3: If x is A3, and y is B3, then z is C3

.....

.....

Rn: If x is An, and y is Bn, then z is Cn

the rule base, R, is defined as the union of the individual rules. An example rule base is shown in figure 25. The rule base may also by presented graphically as a surface similar to figure 26

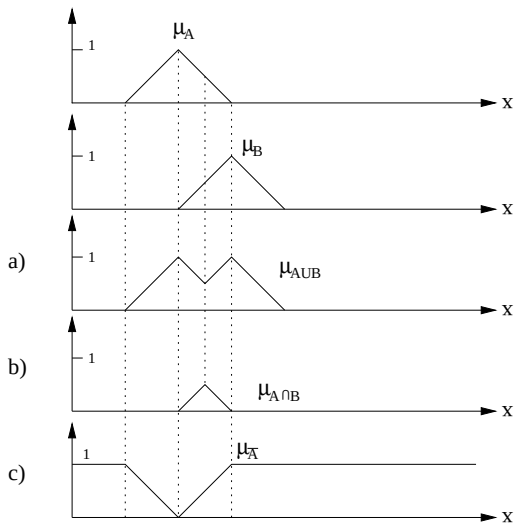

Figure 24: Fuzzy Operations a) union, b) intersection, and c) complement.

	error						
Δerror	NB	NM	NS	ZO	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZO
NM	NB	NB	NB	NM	NS	ZO	PS
NS	NB	NB	NM	NS	ZO	PS	PM
ZO	NB	NM	NS	ZO	PS	PM	PB
PS	NM	NS	ZO	PS	PM	PB	PB
PM	NS	ZO	PS	PM	PB	PB	PB
PB	ZO	PS	PM	PB	PB	PB	PB

Figure 25: Fuzzy model rule base with two input and single output.

$$R = R1 \cup R2 \cup R3 \cup \ldots\ldots \cup Rn$$

5.6 Inference Procedure

The inference procedure determines the degree of correlation between the rules and the input. Since the input is typically involves more than one membership function, the

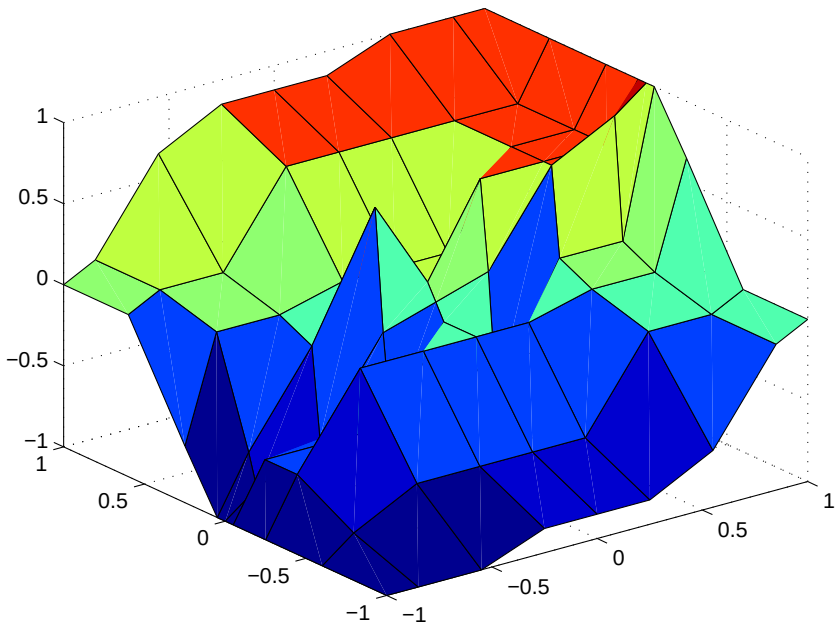

Figure 26: Fuzzy model rule base with two input and single output shown as a surface.

inference is used to decide how much of each rule to utilize. Two methods are typically used, inference with min as conjunction or inference with product as conjunction. Assuming the following rule,

R: if x is A then z is C

where x as the input fuzzy variable; z the output fuzzy variable; and A and C are the fuzzy subsets corresponding of the universe of discourse of X and Z respectfully. The degree of correlation would correspond to the membership of x to A

$$r = \mu_A(x)$$

$$c' = min(c, r)$$

or

$$\mu'_c(r) = min(\mu_c(r), r)$$

for all z $\in$ Z.

Similary, the degree of correlation for the production of conjunction

$$r = \mu_A(u)$$

$$c' = c * r$$

or

$$\mu'_c(z) = \mu_c(z) * r$$

for all z $\in$ Z.

5.7 Weighted Average Method

If the inference procedure does not produce a crisp output, a weighted average is taken to produce the best possible outcome based on the rules and membership functions. For the input $u \in [A_i, A_{i+1}]$, assume the following rules:

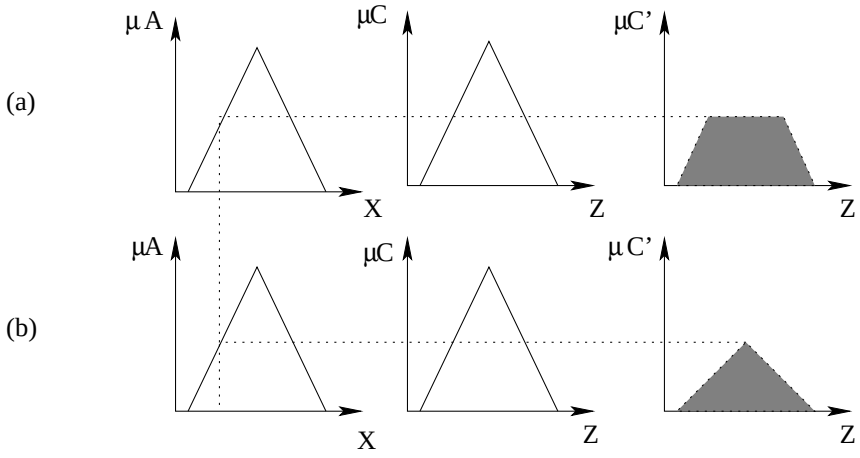

Figure 27: Inference procedure with a) minimum as conjunction and b) product as conjunction.

R1:If x is A_i, then z is C1

R2:If x is A_{i+1}, then z is C2

The weighted average is

$$\frac{\sum_{j=1}^{n} \mu_{A_j}(u) C_{j_i}}{\sum_{j=1}^{n} \mu_{A_j}(u)}$$

where μ_{A_i} is the weight of the membership in the in set A_i and Cj_i is the consequent of the rule if x is Ai then z is Cj_i. Therefore, the output is

$$\mu_{Ai}(u)C1 + \mu_{Ai+1}(u)C2$$

This chapter shows an overview of fuzzy logic including the fuzzification procedure, rule base, and defuzzification procedure. The methods outlined are used within the fuzzy logic controller to interpret the input and construct an output control signal.

The design of the fuzzy logic controller using these procedures is covered in the next chapter.

6 Control Design: Fuzzy Logic Control

6.1 Overview of Fuzzy Logic Control

The controller chosen to control the switched inductor buck will be of the form of fuzzy logic PID controller, as shown in the block diagram in figure 28.The strucure of a fuzzy logic portion of the controller consists of 5 parts:

- input scaling
- fuzzification
- rule base
- defuzzification
- output scaling

6.2 Input Scaling

Input scaling provides a means to bound the input of the fuzzy controller within a certain range. Since the inference procedure is designed to only operate within the bounds [-1,1] ihe input into the fuzzy logic controller is bounded within the universe of discourse between [-1,1]. The input to the fuzzy sets is directly connected to the output of the ADC. Therefore the input gain, g_i, should be selected such that $V_{o_{ADC}} g_i \ \in [-1, 1]$.

$$g_i = \frac{1}{max\ |(V_{o_{ADC}})|} = 1$$

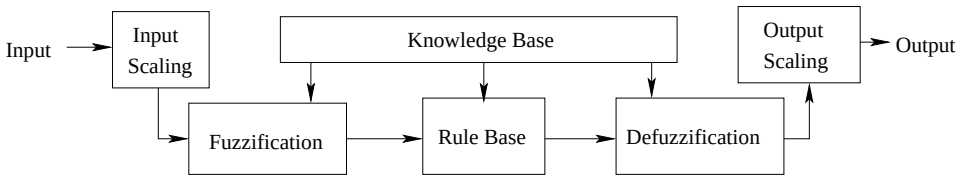

Figure 28: Fuzzy logic control block diagram.

However, to produce adequate output from the fuzzy logic controller, the scale of the integral and derivative must be altered. The sampling frequency of the integral and the derivative causes the output of the integral to be three orders of magnitude smaller than the error signal. Likewise, the output of the derivative is three orders of magnitude larger than the error signal. Such inputs would cause the derivative to dominate the output of the fuzzy logic controller and integral to have little to no effect. In order to produce an output where each operation: proportional, integral, and derivative, has qualatatively equal effect, the inputs are adjusted by the $g_{ip} = 1$, $g_{ii} = 1000$, and $g_{id} = 0.001$ where g_{ip} is the scaling gain of the proportional input, g_{ii} is the scaling gain of the integral input, and g_{id} is the scaling gain of the derivative input.

6.3 Fuzzication

The fuzzification procedure uses triangular membership functions whose spacing is described by the ruler base/control surface in section 6.4. Triangular membership function are chosen due to their simplicity and ease of calculation.

6.4 Rule Base

The rule base provides a method to map the input signal to the corresponding output signal. The rule base, represented as a control surface, where the input is the error voltage and the output is the control action. Three distinct rule bases are utilized to contruct the output signal. One rule base is used to control the propotional gain, one the integral gain, and the last the derivative gain. Each rule base is used to control a differenct aspect of the response.

	NB2	NB2	NB	NM	NS	ZO	PS	PM	PB	PB2	PB3
Input	-1	-0.9	-0.8	-0.12	-0.01	0	0.01	0.12	0.8	0.9	1
Output	1	-0.6	-0.42	-0.3	-0.1	0	0.1	0.3	0.42	0.6	1

Figure 29: Centers for input/output fuzzy set for proportional gain.

6.4.1 Proportional Control Surface

The proportional gain control surface needs to minimize the rise time, the overshoot and steady-state error. In order to improve the rise time, overshoot, and steady-state error, the centers for the input and output fuzzy sets are choosen, shown in figure 29. The control surface corresponding to these centers can be seen in figure 30.

6.4.2 Integral Control Surface

The integral control surface needs reduce the steady-state error to zero while still maintaining the overall stability of the system. In order to decease the steady-state

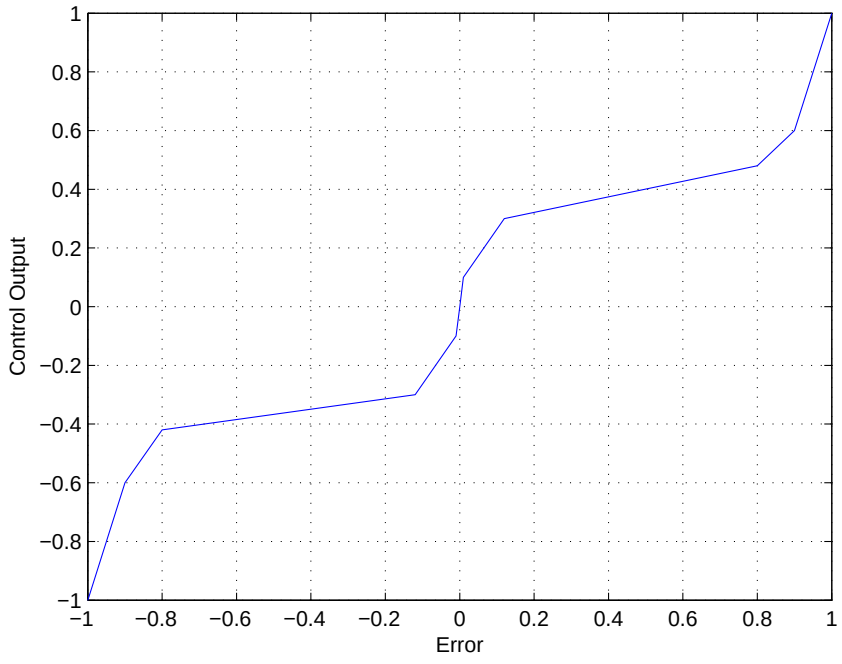

Figure 30: Proportional Gain Control Surface

	NB2	NB2	NB	NM	NS	ZO	PS	PM	PB	PB2	PB3
Input	-1	-0.35	-0.1	-0.01	-0.005	0	0.005	0.01	0.1	0.35	1
Output	1	-1	-0.4	-0.2	-0.01	0	0.01	0.2	0.4	1	1

Figure 31: Centers for input/output fuzzy set for proportional gain.

error while still maintaining stability, the centers for the input and output fuzzy sets are choosen, shown in figure 31. The control surface corresponding to these centers can be seen in figure 32.

6.4.3 Derivative Control Surface

The derivative control surface needs to increase the stability and decrease the overshoot of system, while having little impact on the speed of the system. In order to decrease the overshoot and increase the stability of the system, the centers for the input and output fuzzy sets are choosen, shown in figure 33. The control surface

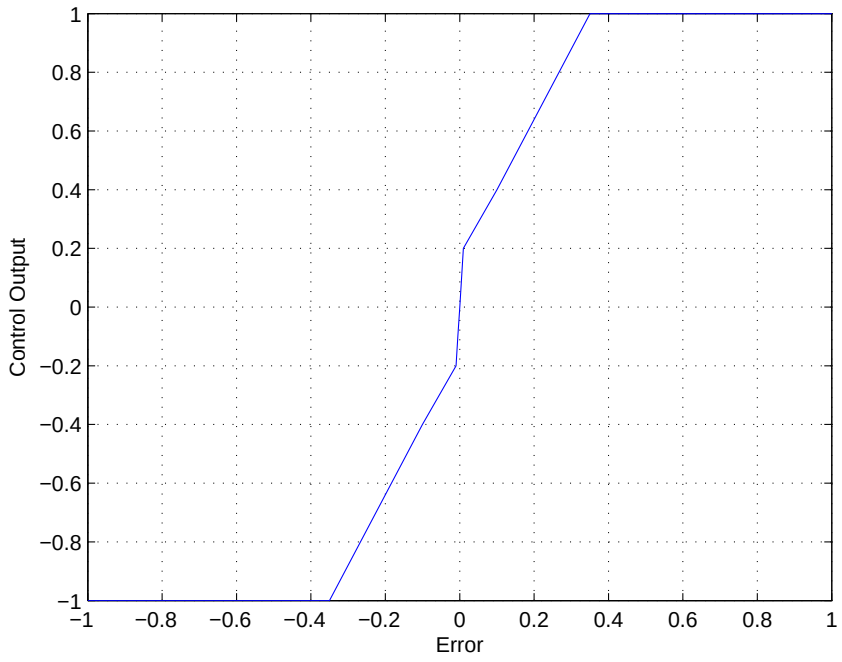

Figure 32: Integral Gain Control Surface

	NB	NM	NS	ZO	PS	PM	PB
Input	-1	-0.2	-0.02	0	0.02	0.2	1
Output	-1	-0.8	-0.2	0	0.2	0.8	1

Figure 33: Centers for input/output fuzzy set for proportional gain.

corresponding to these centers can be seen in figure 34.

6.5 Defuzzification

The defuzzification procedure uses a weighted average method to recieve a crisp output from the membership of the output fuzzy sets.

6.6 Output Scaling

Output scaling allows the output of the fuzzy logic controller to be adjusted so it is the appropriate amplitude when applied to the DPWM of the buck converter. The fuzzy

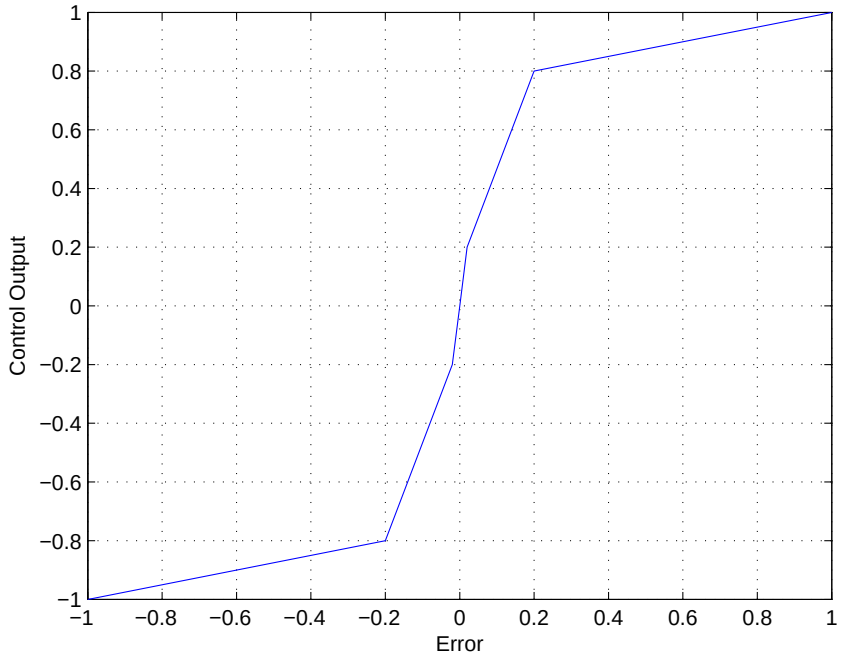

Figure 34: Derivative Gain Control Surface

controller output is bounded in the universe of discourse between [-1,1]. The change in duty cycle control ratio of the DPWM is bounded between $[-\frac{D}{(2-D)}, 1-\frac{D}{(2-D)}]$, therefore the output gain must be selected such that $g_o V_{ofuzzy} \in [-\frac{D}{(2-D)}, 1-\frac{D}{(2-D)}]$. Since V_{ofuzzy} = a, it is already bounded between $[-\frac{D}{(2-D)}, 1-\frac{D}{(2-D)}]$ and $g_o = 1$. The overall gain of the fuzzy controller needs to be decreased in order properly regulate the duty cycle. The outputs the of the the proportional, intergal, and derivative fuzzy sets are decreased by $g_{op} = 0.2$, g_{oi} 0.15, and $g_{od} = 0.15$ respectfully.

6.7 Simulink Model of Fuzzy Logic PID Control

A simulik model, figure 35, is contructed from the parameters obtained in sections 10.2 -10.6. The model has a the error voltage, V_e as the input, and the change in the duty cycle control ratio, a, as the output. The model of the fuzzy logic PID controller is added to the simulink model of the system in figure 20. The resulting is the model is shown in figure 36, and is tested in the next section against the disturbances in the load and source to show improvement has been acheived compared to the open-loop response.

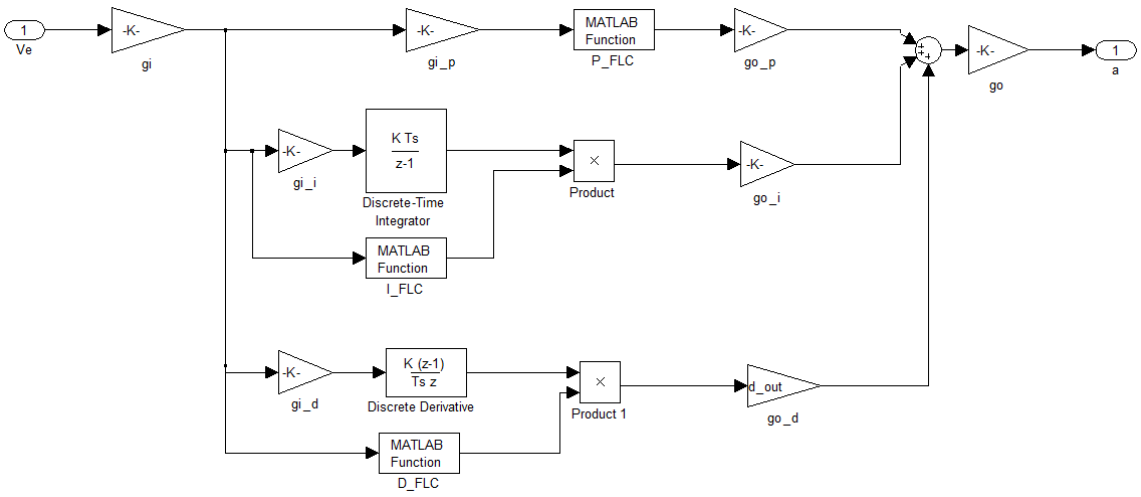

Figure 35: Simulink Model of PID Fuzzy Logic Controller

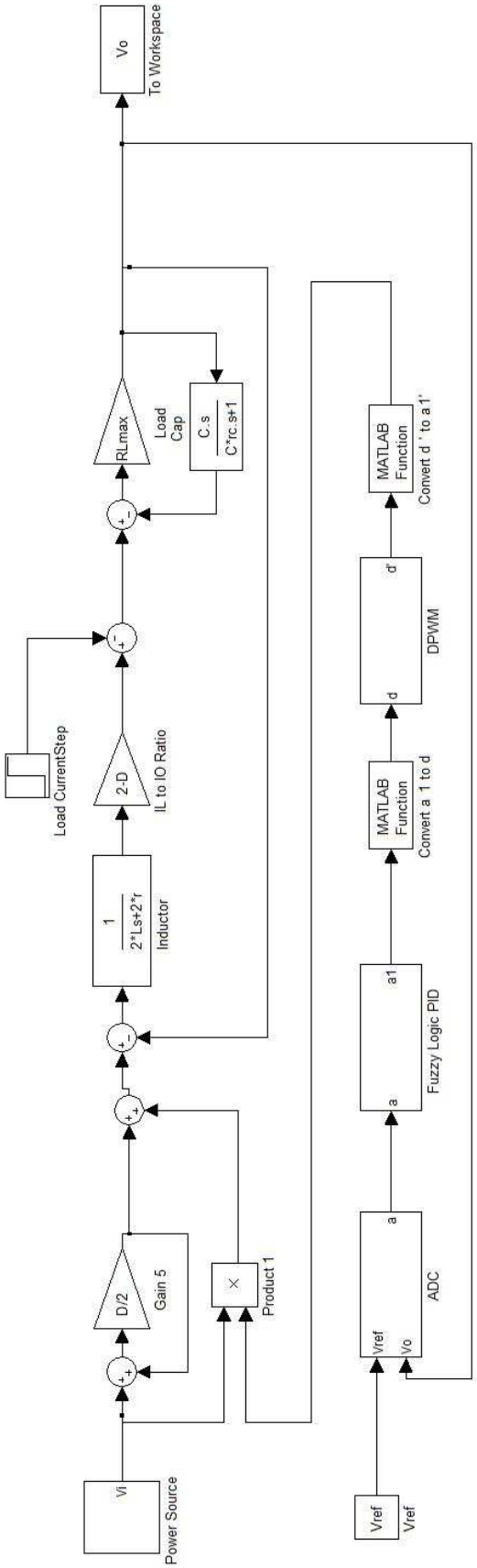

Figure 36: Simulink model of closed-loop compensated switched-inductor buck converter

7 Simulation

7.1 Simulation Parameters

The MATLAB/simulink simulation tests the transient and state-state response of the system to various disturbances from the source and load with using the model in figure 36, with the controller regulating the change in the duty cycle. The simulation is designed to compare the open-loop response of the system with the compensated closed-loop response of the system. The conditions simulated are the same as in section 4 and consist of the following:

1. Connection to the 12 V DC power source
2. 1 Amp step change in the load
3. 1 volt step change in the power source

The switched-inductor buck designed in Section 2 has the following component values:

- L = 20 μH
- C = 220 μF
- R_L = 2.00 Ω
- D_{nom} = 0.2891
- r = 0.0161 Ω @ D_{nom}

The controller is a fuzzy logic PID with the control surfaces outline in section 6.4. The controller contains the required input and output gains mentioned in sectons 6.2 and 6.6. The ADC of the controler has a resolution of $4.8828 * 10^{-4}$ V and a gain of 0.1, while the DPWM has a resolution of $2.4414 * 10^{-4}$ V. Other assumptions made are

- The output ripple due to switching is ignored.
- All other disturbances from the power source, including noise, are ignored.

7.2 Simulation Results

7.2.1 Response to 12 V DC Power Source

The response to the connection to 12 V DC power source of the open-loopv system and the system compensated by a fuzzy logic PID controller can be seen in figure 37. Both responses have zero steady-state error since the initial condition of the duty-cycle, D is 0.2891, is chosen so that is met. The open-loop response has a maximum overshoot of 70 percent while the closed-loop response has a maximum overshoot of 6.5 percent. In addition, the settling rise has been reduced from 2.75 msec to 1.10 msec. However, the rise time has been increased from 0.2 msec to 0.6 msec.

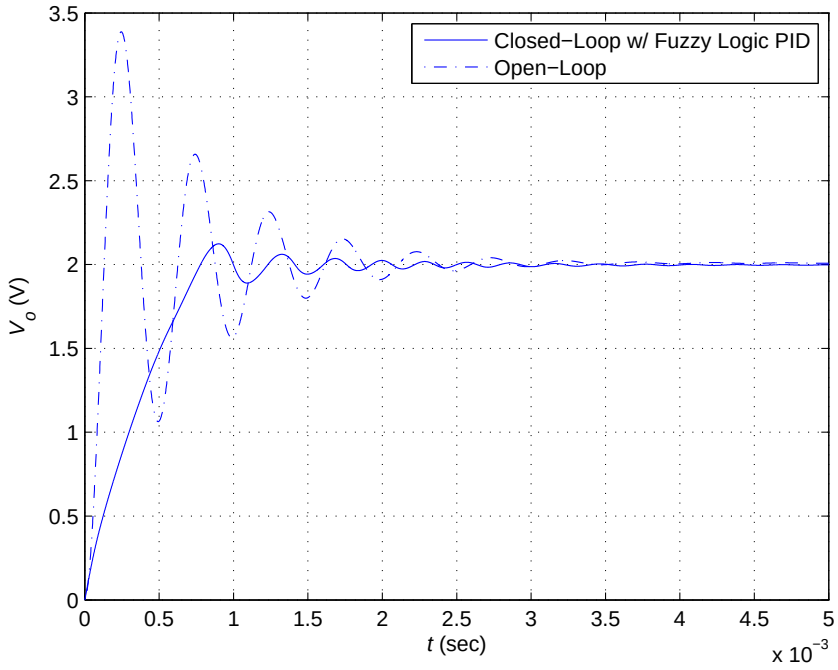

Figure 37: Time response of the open-loop system and closed-loop system compensated by a fuzzy logic PID controller to 12 V DC power source.

7.2.2 Response to 1 A Step Change in Load Current

The time resposne of the open-loop and closed-loop sytem compensated by a fuzzy logic PID controller to a 1 A step change in the load can be seen in figure 38. It can be seen from this figure that the steady-state error decreases from 1 percent to zero. In addition, the maximum undershoot improves from 12 percent to 3 percent and the maximum overshoot improves from 7 percent to 2 percent.

7.2.3 Response to 1 V Step Change in Power Source

The time response of the open-loop and closed-loop system compensated by a fuzzy logic PID controller for a 1 V step change in the source can be seen in figure 39. The figure shows that the steady-state error improves from 8 percent to less than 1 percent for the simulation. The steady-state error of the compensated system eventually decrease to zero because of the integral action. In addition, the maximum

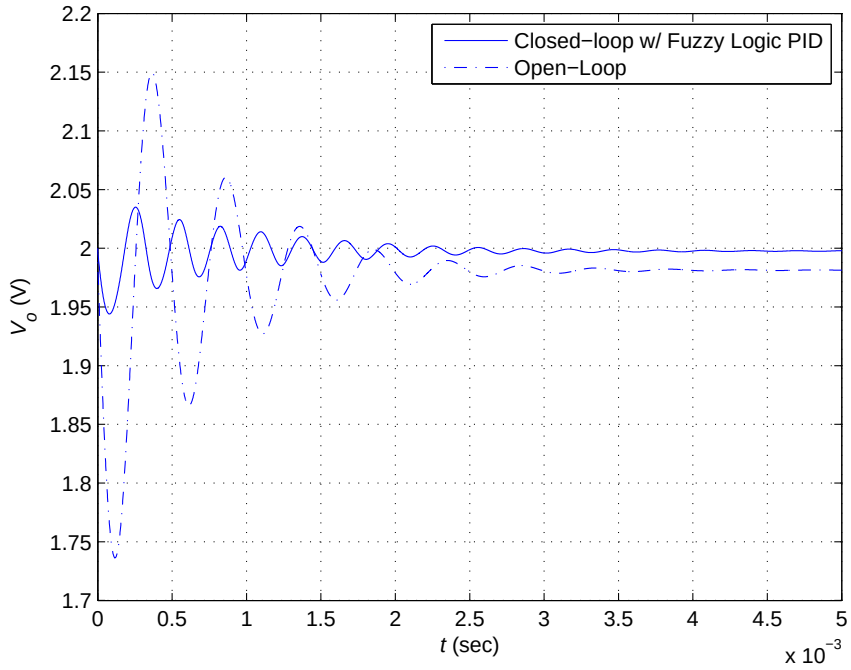

Figure 38: Time response of the open-loop system and closed-loop system compensated by a fuzzy logic PID controller to a 1 A load step change.

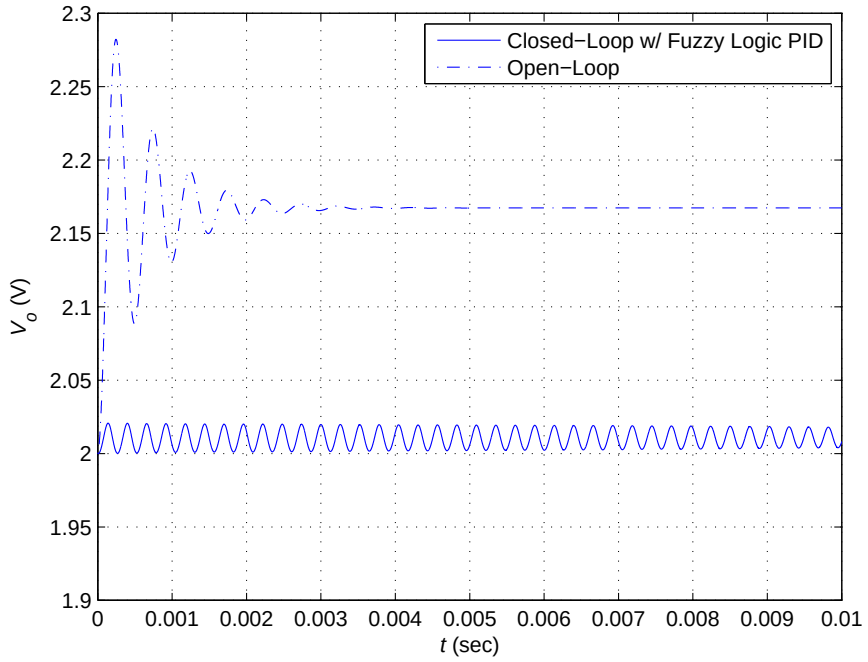

Figure 39: Comparsion of time response for 1 V change in the source between open-loop system and closed-loop system with fuzzy logic PID controller.

overshoot improves from 6 percent to less than 1 percent.

8 Conclusions

Current trends in electronics requiring operation at low voltages with higher currents. In order to supply power to these electronics, PWM power converters are required which are able to deliver these voltages and currents efficiently. One such converter capable of delivering these requirements is the switched inductor buck converter. The circuit is capable of generating lower voltages with a more median duty cycle when compared to the classical buck converter.

In addtion, digital control schemes are replacing the use of analog control schemes when controlling PWM power converters. Digital schemes, implemented through the use of microcontrollers, offer an immunity to component variations, digital system compatibility, and the ability to incorporate advanced control schemes which is not available in analog counterparts.

One advanced control scheme which is implemented with a microcontrollers is fuzzy logic control. Fuzzy logic control is a nonlinear control scheme with piecewise linear proportional, integral, and derivative gain to control the duty cycle of the system. Control of the duty cycle, in turn, controls the output voltage of the system. The fuzzy logic controller is designed to only implement proportional, integral, and derivative gains when they are appropriate to reduce the error signal of the system. Using fuzzy logic control, the time-domain response of the closed-loop system is improved with respect to the open-loop system. The overall speed of the system is also increased, as seen by the decrease of the settling time when the converter is connected to the power source. The system is also capable of fully rejecting disturbances by reducing the steady-state error to zero for a connection to a 12 V DC power source, a 1 A step change in load current, and 1 V step change in the power source voltage. In addition,

the stability of the system is improved by reducing the overshoot/undershoot in all simulations. In all, the overall performance of the system is improved compared with the open-loop operating condition.

Further invesigation of the switched-inductor buck requires modeling and running a cosimulation between MATLAB/Simulink and circuit modeling software; either Synopsys Saber or Orcad PSpice. In additon, further invesigation of the control of the swithched-inductor buck required investigation into current-mode control and using fuzzy logic to regulate it. Finally, to test the control and circuit designs, the circuit should be constructed from the corresponding components, a microcontroller programmed provide the fuzzy logic controller, and the entire system tested to ensure functionallity.

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