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Contact Resistance Measurements in GaAs MESFET's and MODFET's by the Magneto-TLM Technique

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Table I. Summary of germanium etching results

Etch	Etch rate (μm/min)	Comments
30:1:1 HNO_3:CH_3COOH:HF 10 min No agitation	0.4	Hillocks
20:1:1 HNO_3:CH_3COOH:HF 10 min No agitation	1.1	Hillocks, scratches
10:1:1 HNO_3:CH_3COOH:HF 10 min No agitation	3.4	Rough surface
18:8:5 HNO_3:CH_3COOH:HF 3 min Manual agitation	13	Polishing, few ripples, best morphology
18:8:5 HNO_3:CH_3COOH:HF 2 min Ultrasonic agitation	11	Hillocks
5:3:3 (CP-4A) HNO_3:CH_3COOH:HF 5 min No agitation	25	Hillocks
5:3:3 (CP-4A) HNO_3:CH_3COOH:HF 30s Manual agitation	26	Hillocks
10:1:1 H_2SO_4:HNO_3:HF 5 min No agitation	0.44	Hillocks, scratches
10:1:1 H_2SO_4:HNO_3:HF 10 min Ultrasonic agitation	1.2	Hillocks, scratches
1:1:10 H_2O_2:HF:H_2O 60 min No agitation	0.33	Scratches
1:1:4 H_2O_2:HF:H_2O 5 min No agitation	1.7	Scratches
10:1:2 (Caro's etch) H_2SO_4:H_2O_2:H_2O 30 min No agitation	0.01	Very slow, hillocks

HNO_3:CH_3COOH:HF etches with a high HF content were not used since they have been found to leave brown stains of insoluble GeO (3). Etches with lower HF concentrations were slower and bubbled less. These solutions still required agitation, and left ripples on the treated surfaces.

Other etch formulations were investigated in this study. Caro's etch (H_2SO_4:H_2O_2:H_2O) used in a 10:2:1 formulation by volume, was found to be nonpolishing and slow. The etch process was limited by the dissolution of GeO_2 in water (5), and was found to remove only 0.4 μm after 30 min. H_2O_2:HF:H_2O (Superoxol etchant) solutions are faster, but nonpolishing. This etch system has been investigated previously and found (6) to leave hillocks and pits on the surface. They seem to be limited by the Ge oxidation kinetics and reaction product removal, even in very dilute formulations (such as 1:1:20 by volume) (7).

A fourth wet chemical system employed was H_2SO_2:HNO_3:HF. This etch is faster than Caro's etch due to the addition of the complexing agent HF. This etch was also found to be nonpolishing and left hillocks on the treated surface, in spite of the high viscosity of H_2SO_4.

Summary

The chemical polishing of Ge substrates for subsequent epitaxy has been investigated. Various chemical etches for germanium have been studied, and the results summarized in Table I. It is found that only solutions from the HNO_3:CH_3COOH:HF family are polishing, with best results obtained from a 2-3 min treatment in an 18:8:5 parts by volume formulation.

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ABSTRACT

The standard transmission-line model (TLM) for specific contact resistivity measurements of planar contacts is improved in two ways: (*i*) the addition of a magnetic field, which gives the mobility and carrier concentration of the bulk material, and the mobility of the material under the contact; and (*ii*) an extension to two layers, which makes the model applicable to MODFET structures. The results are applied to GaAs MESFET material, and AlGaAs/InGaAs MODFET material. One conclusion concerning the latter material is that the InGaAs electrons directly beneath the annealed Au/Ge/Ni contacts have lower mobility than those in the bulk, but still maintain 2DEG character.

The continual reduction of GaAs and Si device dimensions has placed increased demands on ohmic contact performance, since it is usually necessary to keep contact resistances well below intrinsic device resistances (1). Concomitant with the need for improved contact performance is the need for new and improved contact measurement techniques. For planar contacts, a popular technique at present is based on the transmission-line model (TLM) (2), as applied to the test pattern in Fig. 1. The pa-

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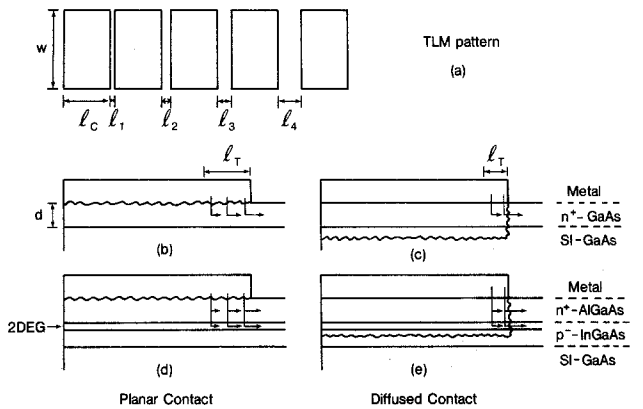

Fig. 1. (a) The TLM pattern used in this study. The nominal dimensions of l_1, l_2, l_3, l_4, l_c, and w, are 2, 4, 6, 10, 40, and 65 μm, respectively. (b) Planar and (c) diffused contacts in MESFET material. (d) Planar and (e) diffused contacts in MODFET material.

rameters deduced from this model include r_s, the sheet resistance of the bulk materials between the contacts, and $\rho_c R_s$, where ρ_c is the specific contact resistivity of the metal/semiconductor (M/S) barrier, and R_s is the sheet resistance of the material under the contacts. It is clear that we cannot determine ρ_c without assuming that $R_s = r_s$, and there is no *a priori* way of making this claim without a supplementary measurement. One such supplementary measurement involves the so-called "end resistance," which is determined by means of a third contact (3). Another way to get information on R_s is to use a magnetic field in conjunction with the usual TLM measurements. This recently-introduced technique (4), called the magneto-TLM (MTLM), determines the mobility μ_c of the material under the contact, as well as the mobility μ and sheet carrier concentration n_s of the bulk material. If $\mu_c = \mu$, then it can be safely assumed that $R_s = r_s$, and ρ_c can be determined. If $\mu_c \neq \mu$, still it may be possible to estimate R_s and thus ρ_c.

Although the usual TLM and MTLM methods work well for single-layer devices, such as GaAs metal-semiconductor field-effect transistors (MESFET's), they are not applicable to two-layer devices, such as AlGaAs/GaAs modulation-doped FET's (MODFET's). In a separate paper, we have formulated a two-layer MTLM model (5), and will apply the results here. It is shown that erroneous conclusions can be drawn from the one-layer model.

Summary of Theoretical Models

Consider the commonly-used test pattern shown in Fig. 1a. The resistance between any two ohmic pads of width w and separation l will be given by

$$R = 2R_c + r_s \frac{l}{w} \qquad [1]$$

and thus a plot of R *vs.* l will have a slope r_s/w, and a y-axis intercept, $2R_c$. If the contacts are modeled as transmission lines, and are "electrically long" ($kl_c \gtrsim 2$), then

$$R_c = \frac{R_s}{wk} = \frac{\sqrt{R_s \rho_c}}{w} \qquad [2]$$

where R_s and ρ_c were defined earlier, and $k = \sqrt{R_s/\rho_c}$, the inverse "transfer length." Unless R_s is known or can be assumed equal to r_s, ρ_c cannot be determined. For example, if there is appreciable contact diffusion, as illustrated in Fig. 1c, then it is doubtful that $R_s = r_s$.

In the MTLM, a perpendicular magnetic field is applied, and

$$r_s = r_{s_0}(1 + \mu^2 B^2) \qquad [3a]$$

$$R_s = R_{s_0}(1 + \mu_c^2 B^2) \qquad [3b]$$

where μ is the bulk mobility and μ_c is the mobility of the material under the contact. The validity of Eq. [3a] and [3b] is discussed in Ref. (6), but suffice it to say that for degenerate electrons, the case for most MESFET's and MODFET's, they hold for arbitrary B (ignoring quantum effects). It can also be argued that ρ_c is nearly independent of B (4). Thus, the one-layer MTLM gives

$$R = 2R_c(B) + r_s(B)\frac{l}{w}$$

$$= 2R_{c_0}(1 + \mu_c^2 B^2)^{1/2} + r_{s_0}(1 + \mu^2 B^2)\frac{l}{w} \qquad [4]$$

where $R_{c_0} = \sqrt{R_{s_0}\rho_c}/w$. It is clear that plots of R_c^2 *vs.* B^2, and r_s *vs.* B^2, will give μ_c and μ, respectively. Since $r_{s_0} = 1/en_s\mu$, we can also determine n_s, the bulk sheet carrier concentration. Thus, a separate Hall-effect measurement is not necessary.

For two-layer materials such as the MODFET structures shown in Fig. 1d, 1e, and 2, neither Eq. [1] nor Eq. [4] is applicable, in general. However, it is possible to solve the distributed-resistance circuit of Fig. 2, in closed form, if $\rho_{c_2} >> \rho_{c_1}$. We may note that Fig. 2 represents a much different two-layer circuit than the one solved recently in Ref. (7), since, in that work, the region under the contacts was not considered in detail.

The solution for the circuit of Fig. 2, if $k_1 l_c$ and $k_2 l_c > 2$, is (5)

$$R = 2R_c^{\text{eff}} + r_s^{\text{eff}}\frac{l}{w} = 2\left[C_1 C_2 \frac{R_{s_1}}{wk_1}\right] + [C_3 r_{s_1}]\frac{l}{w} \qquad [5]$$

where the C_i's are "correction" factors due to the second layer

$$C_1 = 1 + \frac{R_{s_1}}{R_{s_2}}\frac{1}{1 + k_1/k_2} \qquad [6a]$$

$$C_2 = \frac{1 + \dfrac{1}{1 + r_{s_2}/r_{s_1}}\left[\dfrac{k_1}{k}\dfrac{r_{s_1}}{R_{s_1}} + \dfrac{k_2}{k}\dfrac{r_{s_2}}{R_{s_2}}\left[\dfrac{1}{1 + k_1/k_2} + \dfrac{r_{s_2}}{r_{s_1}}\right]\right]\mathbf{F}(kl)}{1 + \left[\dfrac{k_2}{k}\dfrac{r_{s_2}}{R_{s_2}}\dfrac{1 + r_{s_1}/r_{s_2}}{1 + (R_{s_1}/R_{s_2})/(1 + k_1/k_2)}\right]\mathbf{F}(kl)} \qquad [6b]$$

$$C_3 = \frac{r_{s_2}}{r_{s_1} + r_{s_2}} \qquad [6c]$$

where $k_1 = \sqrt{R_{s_1}/\rho_{c_1}}$, $k_2 = \sqrt{R_{s_2}/\rho_{c_2}}$, $k = \sqrt{(r_{s_1} + r_{s_2})/\rho_{c_2}}$, and $\mathbf{F}(kl) = \sinh(kl)/[1 + \cosh(kl)]$. Note that for $kl \lesssim 1$, $\mathbf{F}(kl) \approx kl/2$, while for $kl \gtrsim 4$, $\mathbf{F}(kl) \approx 1$. Thus, the usual plot of R *vs.* l will not be linear for the two-layer case unless $l \gtrsim 4k^{-1}$, for all l. For our sample, $kl \gtrsim 4$ when $l \gtrsim 2.5$ μm, which includes three of the four l values in the TLM pattern. Note also that Eq. [5] reduces directly to Eq. [1] when $r_{s_2} \to \infty$, whereas it might have been expected that the contact-layer 2 parameters should enter, due to the possibility of current mixing still being able to occur in the contacts.

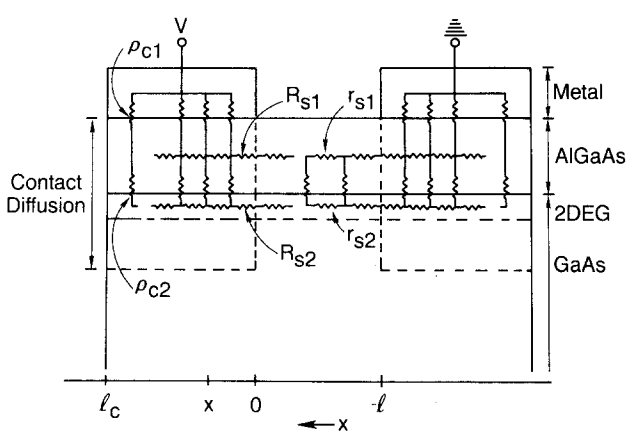

Fig. 2. A two-layer distributed-resistance circuit applicable to MODFET material. Layer 2 is assumed to be mainly due to the 2D electron gas, while layer 1 is due to parallel conduction in the doping layer.

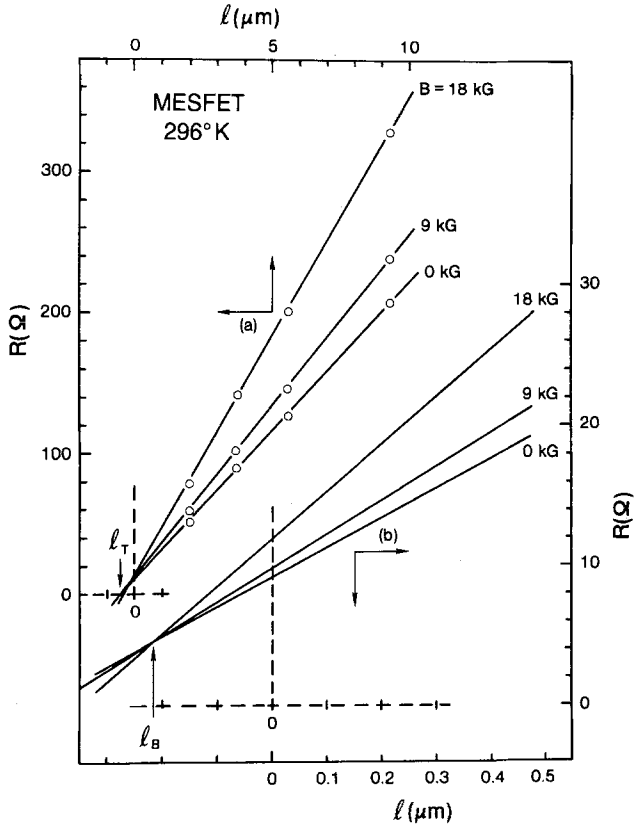

Fig. 3. Resistance vs. contact spacing for GaAs MESFET material at 296 K. Part (b) is an expansion of part (a) near the origin.

However, the theory does not allow this possibility, because of the original assumption $\rho_{c_2} >> \rho_{c_1}$, which was necessary for a closed-form solution of the differential equations. (If $\rho_{c_2} >> \rho_{c_1}$, then current entering contact-layer 1 from bulk-layer 1 will not mix into contact-layer 2, but will flow directly into the contact metal.) Fortunately, literature values (1, 7), suggest that $\rho_{c_1} \simeq 10^{-6}$ Ω-cm², and $\rho_{c_2} \simeq 10^{-5}$ Ω-cm², so that $\rho_{c_2} >> \rho_{c_1}$, as required.

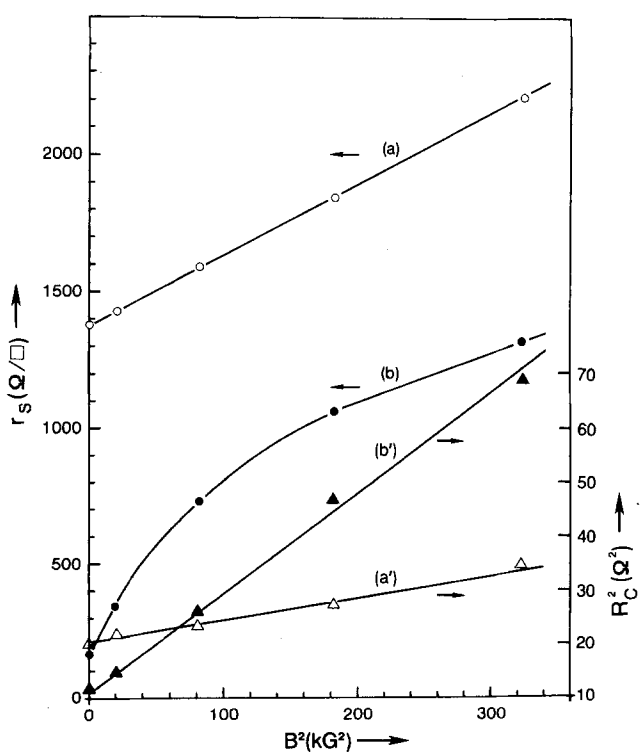

Fig. 4. Plots of bulk sheet resistance (r_s) and contact resistance squared (R_c^2) vs. B^2 for MESFET material [(a)] and (a')] at 296 K, and MODFET material [(b) and (b')] at 77 K.

Table I. Bulk and contact parameters for a MESFET (calculated from Eq. [4])

Parameter	Symbol	Value
Contact resistance	R_{c_0}	4.5Ω
Normalized contact resistance	r_{c_0}	0.29 Ω-mm
Bulk sheet resistance	r_{s_0}	1.37×10^3 Ω/□
Bulk mobility	μ	4.33×10^3 cm²/V-s
Bulk sheet carrier concentration	n_s	1.05×10^{12} cm^{-2}
Mobility under contact	μ_c	4.3×10^3 cm²/V-s
Specific contact resistivity	ρ_c	6.3×10^{-7} Ω-cm²[a]

[a]Assuming that $R_{s_0} = r_{s_0}$.

The two-layer MTLM is simply Eq. [5] along with the magnetoresistance expressions

$$r_{si} = r_{si_0}(1 + \mu_i^2 B^2) = (1 + \mu_i^2 B^2)/en_{si}\mu_i \quad [7a]$$

$$R_{si} = R_{si_0}(1 + \mu_{ci}^2 B^2) = (1 + \mu_{ci}^2 B^2)/en_{sci}\mu_{ci} \quad [7b]$$

where $i = 1$ or 2, for the two layers. We then end up with four bulk parameters, n_{s_1}, μ_1, n_{s_2}, and μ_2, and six contact parameters, n_{sc_1}, μ_{c_1}, n_{sc_2}, μ_{c_2}, ρ_{c_1}, and ρ_{c_2}.

Results and Discussion

In Fig. 3 we show the resistance *vs.* contact spacing for a GaAs MESFET with Au/Ge/Ni contacts, at 296 K. All R *vs.* l data were fitted by the linear least squares method, and the region near the origin is expanded to show the variation of R_c with B. Data for $B = 4.5$ and 13.5 kG were also taken, but are not shown in Fig. 3, for clarity. Note that Eq. [4] predicts that, if $\mu_c^2 B^2 << 1$, then the R *vs.* l curves should merge at $l_B = -wR_{c_0}\mu_c^2/R_{s_0}\mu^2$, and indeed, this is the case. In Fig. 4 we have plotted R_s *vs.* B^2 and R_c^2 *vs.* B^2 for this MESFET, curves (a) and (a'), respectively. From these straight-line plots, we get μ and μ_c, as shown in Table I along with other calculated results. Here it is seen that $\mu_c = \mu$, and thus we can be confident that $R_s \simeq r_s$, and that $\rho_c = w^2R_c^2/R_s = w^2R_c^2/r_s \simeq 6 \times 10^{-7}$ Ω-cm². Also, $n_s \simeq 1.0 \times 10^{12}$ cm^{-2}, which agrees with Hall-effect measurements. Thus, the use of the magnetic field has given several, important, additional pieces of information, and has shown that the calculated ρ_c is indeed correct.

At attempt was made to apply this same one-layer analysis to an $Al_{0.15}Ga_{0.85}As/In_{0.15}Ga_{0.85}As$ MODFET structure, which had been previously investigated by several other techniques (8, 9). If we simply draw straight lines through the raw R *vs.* l data, and then plot r_s and R_c^2 *vs.* B^2, as described above, the results are shown in curves (b) and (b'), respectively, of Fig. 4. It is obvious that the one-layer model fails badly, because the lines are not straight, especially r_s *vs.* B^2. Thus, we must apply a two-layer model.

The two-layer MTLM, consisting of Eq. [5] and [7], was fitted with a least squares routine to the 77 K MODFET data of Fig. 5. The fit is excellent, whereas the one-layer fit is very poor. The 10-parameters, which typically were fitted in about 2s on a DEC8800 computer, are presented for two temperatures and various TLM models in Table II. Some of the parameters could not be determined with good precision. However, it is clear that $\rho_{c_2} >> \rho_{c_1}$, which is necessary for the theory to be valid. The value of ρ_{c_1}, about 1×10^{-6} Ω-cm², is typical for Au-Ge-Ni/n⁺-GaAs barriers. (This MODFET had a 200Å n⁺-GaAs cap layer for parasitic resistance reduction; the rest of the structure consisted of 350Å n⁺-$Al_{0.15}Ga_{0.85}As$, 30Å undoped $Al_{0.15}Ga_{0.85}As$, 200Å p⁻-$In_{0.15}Ga_{0.85}As$, and 1 μm undoped GaAs (8).) According to the results, contact layer 1 consists of 1×10^{12} cm^{-2} electrons with a mobility of about 1200 cm²/V-s; the latter, unfortunately, is very poorly determined. This carrier concentration is lower than that in the bulk, which could be due to a highly compensated region caused by Ga out-diffusion. Contact-layer 2, on the other hand, evidently consists of a large concentration ($n_{sc_2} \simeq 1 \times 10^{13}$ cm^{-2}) of higher mobility electrons ($\mu_{c_2} \simeq 4000$ cm²/V-s). This high concentration could be due to appreciable Ge in-diffusion,

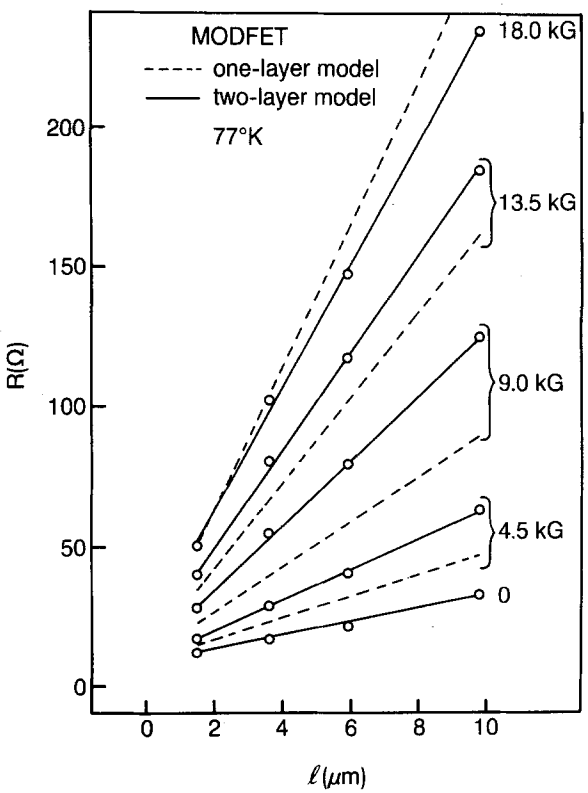

Fig. 5. Resistance vs. contact spacing for MODFET material at 77 K. The solid line is a two-layer fit, using Eq. [5] and [7], and the dashed line is a one-layer fit, using Eq. [4].

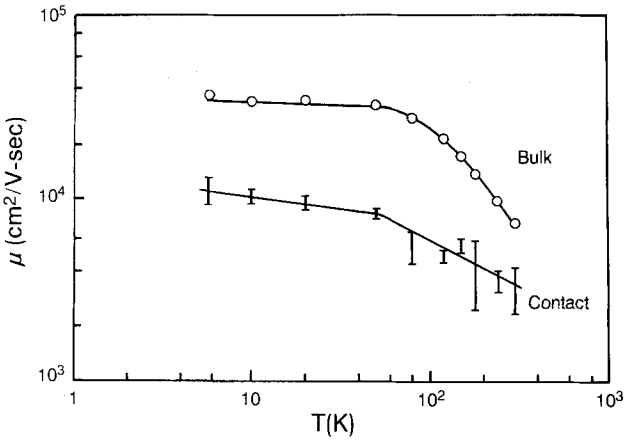

Fig. 6. Bulk 2DEG mobility (μ_2) and contact 2DEG mobility (μ_{c_2}) vs. temperature.

without as much compensation as in layer 1. The relative temperature independence of ρ_{c_1} and ρ_{c_2} suggest that each is primarily due to a tunneling mechanism. Note that this conclusion might not have been reached from either of the one-layer models, since ρ_c in these models appears (incorrectly) to have a significant temperature dependence. The interpretation of ρ_{c_2}, the specific resistivity between layers 1 and 2, may simply involve the heterostructure barriers. Indeed, calculations and measurements of $Al_{0.3}Ga_{0.7}As/GaAs$ barriers give resistivities of about 1×10^{-5} Ω-cm², close to ρ_{c_2} (7). However, the regions under the contacts are complex enough that more careful studies are needed to properly interpret ρ_{c_1} and ρ_{c_2}.

One very significant finding of this study is illustrated by the temperature dependence of μ_{c_2}, shown in Fig. 6. Also shown is the bulk 2DEG mobility, μ_2, which follows the classical 2DEG temperature dependence, and in fact agrees very well with Hall-effect data (8), considering that the latter are uncorrected for parallel conduction. The fact that $\mu_{c_2} < \mu_2$ is not surprising, since significant diffusion of the contacting materials is expected (10). What is interesting, however, is that the material under the contact appears to retain 2DEG character, as evidenced by the low-temperature behavior of the mobility. More samples will have to be studied to confirm this fact.

The bulk parameters given in Table II, n_{s_1}, n_{s_2}, μ_1, and μ_2 are all quite reasonable, and n_{s_2} and μ_2 are very consistent with Hall-effect measurements (8). The parallel conduction in the bulk AlGaAs, consisting of about 2×10^{12} electrons/cm² with 1500 cm²/V-s mobility, is quite large, but nonetheless expected from the 350Å of heavily doped material. Note that the one-layer MTLM gives mobilities which are too low, due to its neglect of parallel conduction. Also, the two-layer model shows that n_{s_1} and n_{s_2} are almost independent of temperature, which, incidently, is a significant advantage of the $Al_{0.15}Ga_{0.85}As/In_{0.15}Ga_{0.85}As$ system over the more common $Al_{0.3}Ga_{0.7}As/GaAs$ system (8). The reason is that the DX-center concentration is much lower for the former material so that low-temperature freeze-out is not as severe a problem.

In conclusion, we have shown that the addition of a magnetic field makes possible much more detailed studies of the bulk and contact regions, within the transmission-line model. The recently derived two-layer model works well for MODFET structures, and is especially valuable in conjunction with temperature-dependent investigations of the various parameters. However, some of the parameters in this model are not well determined for our sample, or need further interpretation, and thus much more work needs to be done.

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Table II. Calculated bulk and contact electrical parameters for a MODFET

		Bulk				Contact					
		n_{s_2}	n_{s_1}	μ_2	μ_1	n_{sc_2}	n_{sc_1}	μ_{c_2}	μ_{c_1}	ρ_{c_2}	ρ_{c_1}
Model	T(K)	10^{12} cm^{-2}		10^4cm²/V-s		10^{12} cm^{-2}		10^4 cm²/V-s		10^{-6} Ω-cm²	
Two-layer[a]	300	1.2 ± 0.1	2.3 ± 0.4	0.72 ± 0.02	0.15 ± 0.05	11 ± 2	0.7 ± 0.2	0.4 ± 0.1	0.12 ± 0.07	9 ± 4	1.0 ± 0.5
(mag. field)	77	1.3 ± 0.1	2.7 ± 0.5	2.73 ± 0.02	0.11 ± 0.02	8 ± 5	0.4 ± 0.3	0.6 ± 0.1	0.06 ± 0.03	7 ± 4	1.0 ± 0.5
One-layer[b]	300	1.8 ± 0.1		0.58 ± 0.02		1.8 ± 0.1		0.56 ± 0.02		0.97 ± 0.02	
(mag. field)	77	1.3 ± 0.1		2.3 ± 0.1		1.3 ± 0.1		1.3 ± 0.1		2.4 ± 0.1	
One-layer[c]	300	$r_s = (6.1 \pm 0.1) \times 10^2$ Ω/□				$R_s = r_s$ (assumed)				0.99 ± 0.02	
(no mag. field)	77	$r_s = (2.0 \pm 0.1) \times 10^2$ Ω/□				$R_s = r_s$ (assumed)				2.5 ± 0.1	

[a]Calculated from least squares fit to Eq. [5] and [7].
[b]Calculated from fit to Eq. [4] at low B. Assumption that $n_{bulk} = n_{contact}$.
[c]Calculated from Eq. [1] and [2]. Assumption that $R_s = r_s$.

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Trench Etches in Silicon with Controllable Sidewall Angles

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ABSTRACT

This paper describes the role of the temperature of the silicon wafer in controlling a deep trench etch sidewall angle and also the etch rate. In addition, we discuss the role of pressure in controlling etch rate and selectivity. This work was performed in a Tegal 1500 Test Bench. The temperature of the wafer could be held fixed as a function of time at any temperature between 20° and 200°C. Our chemistry is chloroform, $CHCl_3$ with O_2 and N_2 as additives. We have found that the sidewall angle of the trench (the angle that the sidewall makes with a normal to the wafer surface) could be varied continuously from about 32° at 40°C to 7° at 190°C. The sidewalls are typically planar and relatively smooth. The bottom of the etch becomes increasingly planar as sidewall angle decreases. In order for the above processes to occur, there must be a small flow of N_2 through the chamber, *e.g.*, 3-5 sccm. Results from the simulation code SAMPLE suggest that the rate of deposition of a material on the etch surface can control sidewall angle. We theorize that a chlorinated hydrocarbon polymer is being deposited, and that the wafer temperature is controlling the rate of deposition of the polymer. In addition to sidewall angle, for zero O_2, increasing wafer temperature over the range stated above can cause the etch rate to increase with increasing temperature by 1800 Å/min at a nominal etch rate of 4000 Å/min. By adding 10% O_2 to the gas mixture, the etch rate becomes insensitive to temperature. By increasing the total gas pressure to 1.2 torr, an etch rate of 8000 Å/min has been obtained, with an attendant selectivity in excess of 15.

Deep trenches in silicon have several important applications, such as device isolation and trench capacitors. For both applications, a trench that has a depth of two to several micrometers (μm) and a width which can be submicron to several micrometers is required. The sidewall profile of the trench is a critical characteristic because it can determine the success of these applications.

Deep trench isolation technology has been demonstrated to improve the device performance and integration density in bipolar devices (1, 2) and bulk CMOS devices (3). Trench isolation has several advantages. First, trench isolation reduces the width of the isolation region significantly due to its vertical wall. Second, the deep trench reduces the lateral NPN parasitic transistor gain and thus reduces susceptibility to latchup for a given n to p spacing. Finally, trench isolation gives higher packing density for the same latchup performance since the trench width is about 1 μm in comparison to the minimum 8 μm spacing required for conventional LOCOS isolation (4).

Morie *et al.* (5) obtained a depletion capacitor by using $CBrF_3$ gas at a pressure of 15 mtorr to etch a trench 0.6 μm wide and more than 1.5 μm deep. Then the trench was refilled with a polysilicon layer on top of 250-300Å of oxide. A capacitance of more than 40 fF was obtained for a cell size less than 35 μm^2. Arai (6) has reported that for a cell size of 35 μm^2, and using 15 nm of SiO_2, a doped face trench capacitor with a capacitance of 23 fF was obtained for zero trench depth; for 3 μm trench depth, the other quantities being the same, 70 fF was obtained.

In this paper, we discuss work which has been done to construct deep trenches with the attributes which make them particularly applicable to the two applications discussed above: a sidewall angle which is fully controllable since it has been shown (7) that filling the trench without a void forming depends on the sidewall angle; planar sidewalls which are relatively smooth; a planar trench bottom with a rounded corner at a junction of the bottom and a sidewall; etch rate and selectivity which are acceptable in a manufacturing environment.

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We will emphasize the importance of controlling the wafer temperature. For example, we will show that trench sidewall angle is a sensitive function of wafer temperature. To a lesser extent, etch rate and selectivity are also effected by this parameter. For example, the sidewall angle can be varied from 32° to 7° by changing the wafer temperature from 40° to 190°C, respectively. Etch rate can be increased by 1800 Å/min as temperature of the wafer is varied over the same range. Finally, we will show that etch rate is a sensitive function of total gas pressure. By changing the total gas pressure from 300 to 1.2 torr, the etch rate will increase from 3000 to 8000 Å/min. The selectivity at the latter pressure exceeds 15.

In the next section, we define trench parameters. In the following sections we discuss: equipment used; work we have done in computer simulating our trench etches, and physical mechanisms the simulation suggests; a quantitative study of the temperature dependence of sidewall angle; and, the parameters which affect etch rate and selectivity. The final section is a summary and discussion of the paper.

Trench profile.—A sketch of the trench profile that we wish to achieve is shown in Fig. 1; it is characterized by a width a, depth h, and sidewall angle θ, measured with respect to the normal to the wafer surface. It is highly desirable that these three parameters should remain independently controllable. For the process that we have developed, we will show that this is the case.

For our process, the width at the top of the etch, a, is determined by and is nearly identical with the width of the window in the mask, *i.e.*, the mask line width. This parameter remains fixed during the etch time. As we have stated above, the sidewall angle θ is an extremely sensitive function of the wafer temperature. The etch depth is sensitive to the total gas pressure and, of course, the etch time. It is a weak function of wafer temperature.

A scanning electron micrograph (SEM) of a trench which looks similar to the sketch in Fig. 1 is shown in Fig. 2a. Notice that the sidewalls and trench bottom are planar, and that these surfaces are relatively smooth.