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ULTRA LOW POWER READ-OUT INTEGRATED CIRCUIT DESIGN

A thesis submitted in partial fulfillment of
the requirements for the degree of
Master of Science in Engineering

By

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B.E., East China Institute of Technology, China, 2006
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Wright State University

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WRIGHT STATE UNIVERSITY

GRADUATE SCHOOL

August 15, 2012

I HERBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Jian Chen ENTITLED Ultra Low Power Read-Out Integrated Circuit Design ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Engineering

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ABSTRACT

Jian Chen. M.S.Egr., Department of Electrical Engineering, Wright State University, 2012. Ultra low Power Read-Out Integrated Circuit Design.

Carbon nanotubes (CNTs) are widely studied by the researchers in recent years, as they have small size, large strength, highly electrical and thermal conductivity. The single-walled CNT (SWNT) is readily changed in electrical resistance when exposed to gas, and has significant use in environmental monitoring, agriculture and fishing industry, chemical industry and even security. A read-out integrated circuit (ROIC) is required to detect the resistive change.

In this thesis, an ultra-low power, wide dynamic detecting range and small size CMOS ROIC design is presented. This ROIC can interface wide dynamic range signal up to more than two orders (100pA-60nA) from deployable sensors using automatic gain control (AGC) unit. A novel technology of sub-threshold technique is applied in this design, which can save up to 96% (from 25.2mW to 0.89mW) power consumption comparing to the circuit operating in super-threshold. To improve the accuracy of calibrated readout current, compensation factor derived from the analysis of simulation results is finally added. The proposed circuit also has the capability to output 8 bit digital signal that can be transmitted wirelessly to the data center for further signal processing.

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1 INTRODUCTION

1.1 Background

During recent years, researchers are showing great interests on carbon nanotubes (CNTs) because of their small size, large strength, highly electrical and thermal conductivity. Consequently, CNTs are implanted as sensing materials in gas, pressure, strain, chemical and biomedical sensors, known as CNTs sensors [1]. With the readily changing in electrical resistance of the semiconducting single-walled CNT (SWNT) based sensors when exposed to gaseous molecules, which makes it has the capability of detecting small concentration of toxic gas or other kind of gas molecules, and has significant use in environmental monitoring , agriculture and fishing industry, chemical industry and even security [2-3].

Considering the accuracy for the signal detecting from sensors, it is important to design a read-out integrated circuit (ROIC) with high resolution, wide dynamic range, anti-noise and easy to control to account for process variation in the manufacturing of CNTs. Most of researchers focused on the methods of detecting the change from CNTs when exposed to gas. The change can be modeled as resistance change. To detect the resistance change, two mainly conversion approaches resistance-to-current and resistance-to-voltage are found in the existed literature.

For the resistance-to-current, the resistance change is first converted to current change by applying a constant voltage on the CNTs sensor [4-9]. The next step is trying

to detect the current. One traditional architecture of detecting the current is converting the current signal from sensor to voltage using an op-amp, known as trans-impedance amplifier (TIA) [10-12], but it should have high performance requirements for this op-amp, such as high gain, small offset voltage and very low leakage current, otherwise, it is hard to detect the weak current signal. Another traditional one is adopting capacitive trans-impedance amplifier (CTIA) [13-15], also known as resistive-to-time (RTC), it reduces the noise and shows good linearity, but requires long measurement time when estimating high resistance values [16].

The resistance-to-voltage method is biasing a fixed current source for the chemical CNTs based sensors [17-20], and then resistance change is converted to voltage change according to Ohm's law. The depicted architectures in [17-20] are limited for the relatively small resistance variations.

1.2 Motivation

In energy constrained applications such as read-out integrated circuit design for CNTs based biomedical, chemical sensors, or other portable devices, where the low power dissipation is the priority. Ultra-low power circuit design with capability of operating at low frequency is very desirable in these applications.

According to the existed literature, most ROIC designers for CNTs based sensors are focused on the methods to increase the measurement accuracy and already obtained some improvements, but didn't pay much attention to the power consumption. Considering that the input range is fixed for an ADC working normally, automatic gain control (AGC) is needed in ROIC to handle wide sensing range.

Hence, the goal of this thesis is:

- Design an ultra-low power ROIC using novel sub-threshold technology
- Design an automatic gain control (AGC) circuit to maximize the detecting range

1.3 Document Organization

The thesis is organized as follows: Chapter1 introduces the background and motivation for ROIC design. Chapter 2 briefly discusses the properties of CNTs based biomedical or chemical sensors and also the analysis of components, such as operational amplifier, analog to digital conversion. Chapter 3 describes the ROIC design in sub-threshold, which includes CVC, AGC and ADC design. It discusses the comparison in power consumption for ROIC between super-threshold and sub-threshold, and analyze the comparison between input current from sensor and the calibrated output current. Compensation technology is applied to improve conversion accuracy. Finally, chapter 4 gives the conclusion and future work.

2 THEORY OVERVIEW

2.1 Carbon nanotubes (CNTs) based sensor

Sensors are these devices detecting or measuring physical and chemical quantities such as gas concentration, temperature, pressure, and etc. In recent years, researchers are showing great interests on carbon nanotubes (CNTs) because of their small size, large strength, highly electrical and thermal conductivity, low cost, high specific surface area. Consequently, CNTs are implanted as sensing materials in gas, pressure, strain, chemical and biomedical sensors, known as CNTs sensors.

Based on the arrangement of graphene cylinders, CNTs can be categorized by two types: single-walled nanotubes (SWNTs) and multi-walled nanotubes (MWNTs). Considering CNTs structures are susceptible to structural instability as they have high aspect ratio. MWNTs have worse defined shapes of cylinder than SWNTs, and hence have higher possibilities of structure defects. Consequently, people prefer to use SWNT in their research. With the easily changing in electrical resistance of the semiconducting SWNT based sensors when exposed to gaseous molecules, SWNTs has the capability of detecting even small concentration of toxic or other kind of gas molecules, and has significant use environmental monitoring , agriculture and fishing industry, chemical industry and even security. Fig. 2.1 is the model of SWNT.

Fig. 2.1 Single-Wall Nanotube (SWNT) Model

As shown in Fig. 2.1, fixed gate or fixed drain to source voltage is applied to the SWNT sensor to measure the current flowing through it. The basic principle behind gas detection or any other detections is the change in the electrical properties, such as resistance, permittivity, resonate frequency and etc when exposed to different gases (N_2, CO_2, SO_2) or concentration variation. In this thesis, a chemical CNTs sensor model is studied. Its resistance is very sensitive to the concentration. To facilitate the detection, the resistance change can be transferred to current change from sensor applying a fixed voltage drop from drain-to-source based on the Ohm's Law ($I=V/R$). Therefore, the final task is trying to find an effective approach to detect the current change from sensor.

2.2 Operational amplifier

Operational amplifiers, also known as op-amp, are the most significant part in linear integrated circuits. Op-amps have different performances based on their topologies. Such as one stage op-amp has limited gain, cascade op-amp has increased gain but has poor output swing and two stages op-amp is more complex in architecture but providing high gain and high output swing. Considering the high gain and high swing needed in this

ROIC design, two stages op-amp is selected. Fig. 2.2 shows a two stage op-amp schematic circuit (a), block diagram (b) and symbol (c).

Fig. 2.2 Two-stage op-amp: (a) Schematic, (b) Block diagram (c) Symbol

As shown in Fig. 2.2(a) typical two stages op-amp includes a differential amplifier and an inverter amplifier. Differential amplifier provides high gain and reduces noise, while inverter amplifier provides extra gain and large swing. In the following sections, some of the design parameters, such as input common mode range (IMRR), common mode rejection ratio (CMRR), gain, phase Margin (PM), gain etc will be discussed.

2.2.1 Input Common Mode Range (IMRR)

Common mode means connecting inverting terminal and non-inverting terminal together, then the two input voltage will change in the same direction. To keep all the transistors working in saturation region, input voltages must be constrained in certain range [21].

Connecting two input terminal together, it can be obtained,

$$V_{g1} = V_{g2} \quad (2.1)$$

To keep transistor M1 saturated, following inequality equation must be satisfied,

$$\begin{cases} V_{ds1} \geq V_{gs1} - V_{tn} \\ V_{gs1} > V_{tn} \end{cases} \quad (2.2)$$

Applying $V_{ds1} = V_{d1} - V_{s1}$, then we obtain,

$$V_{g1} \leq V_{d1} + V_{tn} \quad (2.3)$$

Since

$$V_{d1} = V_{dd} - V_{sd3} = V_{dd} - V_{sg3} \quad (2.4)$$

Substituting Eq. (2.4) into inequality Eq. (2.3) yields,

$$V_{g1} \leq V_{dd} - V_{sg3} + V_{tn} \quad (2.5)$$

Considering the current through transistor M3 (in saturation region) is,

$$I_{sd3} = 0.5I_{sg5} = 0.5\beta_3(V_{sg3} - |V_{tp}|)^2 \quad (2.6)$$

$$\text{After calculation, then } V_{sg3} = \sqrt{2I_{sd3}/\beta_3} + |V_{tp}| \quad (2.7)$$

Combine Eq. (2.7) and Inequality Eq. (2.5), we get,

$$V_{g1} \leq V_{dd} - \sqrt{2I_{sd3}/\beta_3} - |V_{tp}| + V_{tn} \quad (2.8)$$

If we keep reducing V_{g1} to a certain value, transistor (M5) will be out of saturation.

So, to keep M5 in saturated, the voltage relationship is given by,

$$V_{ds5} \geq V_{gs5} - V_{tn} \quad (2.9)$$

$$I_{ds5} = 0.5\beta_5(V_{gs5} - |V_{t5}|)^2 \quad (2.10)$$

Calculate Eq. (2.9), it is easy to get,

$$V_{gs5} \leq \sqrt{2I_{ds5}/\beta_5} + V_{tn} \quad (2.11)$$

$$\text{Similarly, we can get } V_{gs1} = \sqrt{2I_{ds1}/\beta_1} + V_{tn} \quad (2.12)$$

Substitute Eq. (2.11) into Inequality Eq. (2.9) yields,

$$V_{ds5} \geq \sqrt{2I_{ds5}/\beta_5} + V_{tn} - V_{tn} = \sqrt{2I_{ds5}/\beta_5} \quad (2.13)$$

As described in Fig. 2.2, we have,

$$V_{gs1} = V_{g1} - V_{s1} = V_{g1} - V_{d5} \quad (2.14)$$

$$\text{And} \quad V_{ds5} = V_{d5} - V_{ss} \quad (2.15)$$

Hence,

$$V_{g1} = V_{gs1} + V_{d5} = V_{gs1} + V_{ds5} + V_{ss} \quad (2.16)$$

Similarly,

Combine Eq. (2. 12), Eq. (2. 15) and Inequality Eq. (2.13) yields,

$$V_{g1} \geq \sqrt{2I_{ds1}/\beta_1} + \sqrt{2I_{ds5}/\beta_5} + V_{tn} + V_{ss} \quad (2.17)$$

Finally, we obtain the range of input gate voltage for transistor M1,

$$\sqrt{2I_{ds1}/\beta_1} + \sqrt{2I_{ds5}/\beta_5} + V_{tn} + V_{ss} \leq V_{g1} \leq V_{dd} - \sqrt{2I_{sd3}/\beta_3} - |V_{tp}| + V_{tn} \quad (2.18)$$

Where $\beta_1 = 0.5 \mu_n W_1/L_1$ and $\beta_3 = 0.5 \mu_p W_3/L_3$, μ_n/μ_p are the mobility of electron and hole respectively. If known the current, size, power supply, then the input range would be readily obtained.

To simplify the calculation in our design, inequality Eq. (2.18) can be changed into,

$$V_{tn} + V_{ss} \leq V_{g1} \leq V_{dd} - |V_{tp}| \quad (2.19)$$

Therefore, the input range of two stages op-amp can be approximately acquired with just knowing power supply. For example, with 1.8V power supply ($V_{dd} = 0.9V$ and $V_{ss} = -0.9V$), $V_{tn} = 0.3$, $V_{tp} = -0.32$, then the input range is from -0.6V to 0.58V. If reduce the power supply to 0.8 V ($V_{dd} = 0.5V$ and $V_{ss} = -0.5V$), then the input range will be decreased to (-0.2 to 0.18).

2.2.2 Common Mode Rejection Ratio (CMRR)

CMRR is the parameter to evaluate the ability for input noise rejection. The equation is given by,

$$CMRR = \frac{A_d}{A_c} \quad (2.20)$$

Where A_d is the differential gain given by different input voltage, and A_c is common mode gain provided with same input. Ideally, common mode gain is zero and the CMRR is infinite according to Eq. (2.20). However the two input voltages are not the same because of the noise or any other influent factors, such as input variation. Hence, the smaller A_c means less distortion from noise, which also means the larger CMRR, the better for the noise rejection [21].

2.2.3 Phase Margin (PM)

Phase margin is the difference between the phases, generally measured in degree, which is widely used in stability measuring of a system in frequency domain. In system design, the larger PM (system will be more stable) is preferred, typical PM value is 45° , but prefer 60° for practical design. Recalling the multiple op-amp stage design, the performances of op-amps are varied due to mutual influence among them.

2.2.4 Closed loop op-amp gain

Closed loop op-amp gain, is the significant parameter in the op-amps design especially in sub-threshold design. The high gain would increase the performance of the entire system [21].

Fig. 2.3 General block diagram of closed-loop Op-amp

Fig. 2.3 is the general block diagram of a closed-loop Op-amp, where $A(j\omega)$ is the open loop gain and $F(j\omega)$ is the closed loop gain, the transfer function is given by,

$$\frac{V_{out}}{V_{in}} = \frac{A(s)}{1+A(s)} = \frac{A(j\omega)}{1+A(j\omega)F(j\omega)} \quad (2.21)$$

If $A(j\omega)F(j\omega) \gg 1$, then Eq. (2.21) can be simplified as,

$$\frac{V_{out}}{V_{in}} = \frac{1}{F(j\omega)} \quad (2.22)$$

Therefore, if open-loop gain is large enough, the closed-loop gain depends on external feedback circuit.

Fig. 2.4 Closed-loop Op-amp

To better comprehend the concept of closed loop gain, a more specific example is presented. Fig. 2.4 is the schematic of closed-loop op-amp, where the external circuit composed by two resistors R_1 and R_2 in series. As seen in Fig. 2.4, I_{nn} is negligible as the input resistance of op-amp is infinite. According to KCL, Eq. (2.23) can be obtained,

$$\frac{V_{in}-0}{R_1} = \frac{0-V_{out}}{R_2} \quad (2.23)$$

Applying calculation, then

$$V_{out} = -\frac{R_2}{R_1} V_{in} \quad (2.24)$$

Where the ratio of R_2 and R_1 is the feedback gain, which is the reciprocal of $F(j\omega)$

2.2.5 Slew Rate (SR)

Slew rate is the changing rate (response speed) for the output signal in electronic circuits design. The measured two points are selected at 10% and 90% respectively, as depicted in Fig. 2.5. Considering some deviations between rising SR and falling SR,

usually the average value can be used. However, the best design is to keep $SR_{rising} = SR_{falling}$

$$\text{For the rising SR} \quad SR_{rising} = \frac{dV_{out}}{dt} = \frac{V_2 - V_1}{t_2 - t_1} \quad (2.25)$$

$$\text{For the falling SR} \quad SR_{falling} = -\frac{dV_{out}}{dt} = \frac{V_2 - V_1}{t_4 - t_3} \quad (2.26)$$

Finally, the average slew rate is given by Eq. (2.27),

$$SR = \frac{1}{2} (SR_{rising} + SR_{falling}) = (V_2 - V_1) \left(\frac{1}{t_2 - t_1} + \frac{1}{t_4 - t_3} \right) \quad (2.27)$$

Fig. 2.5 Slew Rate (SR)

2.3 Analog to digital convertor (ADC)

Analog to digital convertor is the device that convert continuous signal to discrete data. In the real world, most things can be higher or lower, louder or quieter, on a sliding scale, which are characterized by analog signal. However, the analog signal is easily got lost, distorted and sometimes even impossible to be recovered by the receiver due to the effects of random noise [22]. Digital signal can reduce noise effectively and it is also easy to manipulate, compatible with digital systems, such as microprocessor. In terms of conversion method, ADCs are classified by direct-conversion (flash ADC, pipeline ADC,

SAR ADC) and indirect conversion (digital ramp ADC, delta-sigma ADC, counter ramp ADC). ADCs also have other classifications based on power consumption, operating speed, resolution, number of bits and even the complexity. Flash ADC is easily to be implemented and widely used in current integrated circuit design, which is the architecture used in our ROIC design. To better comprehend the operating principle and to facilitate the design, some of the important technical standards are illustrated in the following sections.

2.3.1 Resolution

Resolution, also called Least Significant Bit (LSB) is the minimum change for the input signal that can be detected by the ADC, and is expressed as Eq. (2.28).

$$Resolution = \frac{1}{N} = \frac{FSR}{2^n} = \frac{V_{refp} - V_{refn}}{2^n} \quad (2.28)$$

Where n is the number of bits, and FSR is the full scale range. N is the number of gradations ($N = 2^n$), V_{refp} and V_{refn} are the positive, negative reference voltage respectively. The number of bits can be characterized the resolution, as listed in Table 2.1.

Table 2.1 The number of bits (n) vs number of gradations (N)

Number of bits (n)	Number of gradations (N)
4	16
8	256
12	4096
16	65536

2.3.2 Sampling Rate [23]

Sampling rate defines the number of samples taken from analog signal to make digital signal in one second, which indicates the speed of ADC. In virtue of Nyquist Sampling Theorem, to avoid aliasing in frequency domain, the sampling frequency is at least two times larger than the maximum frequency of the signal, is given by,

$$f_s \geq 2f_{max} \quad (2.29)$$

2.3.3 Quantization Error [23]

- Signal-to-Noise-Ratio (SNR)

Signal-to-Noise-Ratio is a measure of comparison between signal and background noise. It defines the ratio of the signal power to the sum of all other noise power excluding the first nine largest spur and dc [23].

$$SNR = 10 \log \left(\frac{p_{signal}}{\sum p_{noise}} \right) = 20 \log \left(\frac{A_{signal}}{\sum A_{noise}} \right) = A_{signal}(dB) - A_{noise,dB}(dB) \quad (2.30)$$

- Signal-to-Noise-And-Distortion (SINAD)

SINAD is the ratio of the signal power to sum of the all other noise excluding dc.

$$SNR = 10 \log \left(\frac{p_{signal}}{\sum (p_{noise} + p_{distortion})} \right) \quad (2.31)$$

- Effective Number of Bits (ENOB)

ENOB is a measure of the quality for the analog to digital conversion. The relationship between ENOB and SNR or SINAD is described as below,

$$ENOB_{SNR} = \frac{SNR - 1.76}{6.02} \quad (2.32)$$

$$ENOB_{SINAD} = \frac{SINAD - 1.76}{6.02} \quad (2.33)$$

- Spur-Free Dynamic Range (SFDR)

SFDR is the ratio of the signal power to the largest spur whether harmonically related or not, which can be expressed by,

$$SFDR = Signal(dB) - largest\ Spur\ (dB) \quad (2.34)$$

2.3.4 Integral Non-Linearity (INL) [23]

INL is the maximum difference between the actual and ideal finite resolution characteristic measured vertically in percent or LSBs, as shown in

Fig. 2.6 INL and DNL

2.3.5 Differential Non-Linearity (DNL) [23]

DNL is a term defining the deviation between adjacent codes measured at each vertical step in percent or LSBs, which is expressed as below,

$$DNL = (D_{cx} - 1)LSBs \quad (2.35)$$

Where D_{cx} is the size of the actual vertical step in LSBs

3 READ-OUT INTEGRATED CIRCUIT DESIGN OPERATING IN SUBTHRESHOLD

3.1 Introduction

To detect the resistance change when resistive CNTs sensors are exposed to gas, two mainly conversion approaches resistance-to-current and resistance-to-voltage are adopted. Each of approach also has different architectures to implement.

According to the existed literature, most of researchers focused on the architectures to implement a read-out integrated circuit (ROIC) with high resolution, wide dynamic range, anti-noise and easy to control to account for process variation in the manufacturing of CNTs, and already obtained some improvements but didn't pay much attention to the power consumption. However, in energy constrained applications such as read-Out integrated circuit design for CNTs based biomedical, chemical sensors, or other portable devices, where the low power dissipation is the priority. Therefore, ultra-low power circuit design with capability of operating at low frequency is very desirable in these applications. In this thesis, a ROIC for the resistive CNTs based sensors applying sub-threshold technology is presented. Meanwhile the ROIC also includes automatic gain control unit to extend the reading dynamic range.

3.2 Implementation of sub-threshold ROIC

The proposed sub-threshold ROIC includes current to voltage converter (CVC), automatic gain control (AGC), multiplexer, buffer and analog to digital conversion

(ADC), as shown in Fig. 3.1, which can be used to detect the current from the sensor such as carbon nanotube sensor. This ROIC has wide dynamic current reading range and extremely low power consumption after applying automatic gain control (AGC) and sub-threshold technology. In this circuit, the current flowing to the sensor is transferred to voltage (V_0) after through the transistor M1. M1 is operating in linear region act as an active resistor. Hence Fig. 3.1 can be simplified as Fig. 3.2. In Fig. 3.2, R_{M1} is the resistance of transistor M1, R_{sensor} is the resistance of sensor, V_{ref} is the reference voltage applied on one terminal of sensor, and V_s is the source voltage of M1. If R_{M1} is fixed, then V_0 is give by,

$$V_0 = \frac{R_{M1}V_{ref} + V_s R_{sensor}}{R_{M1} + R_{sensor}} \quad (3.1)$$

As shown in Fig. 3.1, after initial I-V conversion, V_0 goes into DC level shifter to shift DC voltage to zero and multistage amplifiers. Meanwhile AGC determines which stage's output is selected to send to next stage. After that a unit gain buffer is added to drive the ADC. Finally, interfaces ADC to convert analog signal to digital signal for future digital signal processing. The detail discussions will be given in the following sections.

In this thesis, all the components are implemented in 180nm CMOS technology. To compare the difference in power dissipation and other performances, three sets of power supplies ($V_{dd}=0.5V/V_{ss}=-0.5V$; $V_{dd}=0.4V/V_{ss}=-0.4V$; $V_{dd}=0.3V/V_{ss}=-0.3V$) are used.

Fig. 3.1 Block diagram of ROIC

Fig. 3.2 Simplified block diagram of ROIC

3.2.1 Sub-threshold technology

Sub-threshold technology is a terminology that operating transistors in sub-threshold region by providing gate-to-source voltage lower than threshold voltage ($V_{gs} < V_{th}$). The characteristic of transistor working in sub-threshold was studied since 1970s [24]. It is known that a minority channel is formed When V_{gs} is larger than V_{th} , here calls super-threshold, or strong inversion. Ideally, when V_{gs} is lower than V_{th} , the channel between source and drain is off. However, some of the more energetic electrons can still flow from source to drain due to Boltzmann distribution of electron energies, and a weak

current created in the channel, known as leakage current, sub-threshold current, weak inversion current. Study found that the current is decreasing exponentially when the gate-to-source voltage is scaling down after below threshold voltage V_{th} , and is related to the thermal voltage, transistor size, sub-threshold slope parameter and etc. The relationship can be expressed as following two equations [25]:

$$I_{d_subthreshold} = I_0 e^{\frac{V_{gs}-V_{th}}{nV_T}} \left(1 - e^{\frac{-V_{ds}}{V_T}} \right) \quad V_{gs} < V_{th} \quad (3.2)$$

When $V_{gs} = V_{th}$, the drain to source current is given by,

$$I_0 = \mu_{n(p)} C_{ox} \frac{W}{L} (n - 1) V_{th}^2 \quad (3.3)$$

Where the parameters in Eq. (3.2) and (3.3) are defined as:

W	Effective width of the channel
L	Effective length of the channel
n	Sub-threshold slope parameter
V_T	Thermal voltage ((KT/q) =26 mV at 300K)
$\mu_{n(p)}$	Carrier mobility for n and p channel device
C_{ox}	Gate oxide capacitance per unit area

The incentive of operating the circuit in weak inversion is to be able to exploit the sub-threshold leakage current as the operating drive current. From equation (3.2), the sub-threshold current is exponentially related to the gate voltage, which means it will give an exponential increasing delay. However, the simulation results show that the reduction in power dissipation (PD) outweighs the increase in delay, it means the power delay product (PDP) in sub-threshold circuits is less than the one working in strong

inversion circuits. As listed in Table 3.1, the comparisons in the delay and PD between sub-threshold and strong inversion for single inverter, nand2 and nor2 gate, it is found that their power consumption from sub-threshold region is much less than that from strong inversion and delay is larger when gates working in sub-threshold region than that in strong inversion region, but the power delay product in sub-threshold region gained a lot when comparing to that working in strong inversion region. Therefore, circuits working in weak inversion have improved performance in the power delay product.

Table 3.1 Comparisons between sub-threshold and super-threshold
for single inverter, nand2 and nor2 gate

		Delay (s)	Power (W)	PDP (W.S)	PDP Ratio of super- to sub-
Inverter	Super-threshold	5.55p	10.5 μ	58.28E-18	64.1
	Sub-threshold	2.60n	0.35n	0.910E-18	
Nand2	Super-threshold	8.93p	9.39 μ	83.85E-18	69.4
	Sub-threshold	3.45n	0.35n	1.208E-18	
Nor2	Super-threshold	13.8p	13.7 μ	189.1E-18	47.5
	Sub-threshold	8.65n	0.46n	3.979E-18

Fig. 3.3 Schematic of Op-amp

To illustrate sub-threshold technology, a two stage operational amplifier design process is presented. As shown in Fig. 3.3, the two stage operational amplifier has two power supply $V_{dd}=0.4V$ and $V_{ss}=-0.4$, and $V_{bias}=-0.1789$.

At the beginning, DC analysis is applied to find the V_{bias} value for $V_{out}(DC) = 0$. The following procedures are used:

Step1: Sweep the biased voltage till get the zero output voltage;

Step2: Record the value of bias voltage when output voltage is zero;

Step3: Measure the dc voltage for all the other nodes at the value of bias voltage recorded in the second step. All the node DC voltages are marked in Fig. 3.3. According to the Eq. 3.2, all the transistors in op-amp are working in sub-threshold region. For example, transistor M5, $V_{gs5}=-0.1789-0.4=0.2211V$ less than $V_{th}(V_{th}=0.38V)$. Therefore M5 working in sub-threshold region.

As known, Op-amp is the key component in the CVC design. Consequently, the performance of Op-amp will affect the design of DC level shifter and multi-stage amplifiers. For instance, as shown in Fig. 3.8, to shift the median input voltage (V_{in}) to zero in DC level shifter block, appropriate value of V_{adjust} should be given, as listed in Table 3.2, the deviation between simulated V_{adjust} and calculated V_{adjust} is expressed by Error%.

$$Error\% = \left| \frac{V_{adjust_sim} - V_{adjust_cal}}{V_{adjust_cal}} \right| \times 100\% \quad (3.4)$$

Table 3.2 Error percentage vs power supply and gain

		$V_{dd} = 0.9V$ $V_{ss} = -0.9V$ Gain=51.8dB		$V_{dd} = 0.5V$ $V_{ss} = -0.5V$ Gain=52.3dB		$V_{dd} = 0.5V$ $V_{ss} = -0.5V$ Gain=65.2dB	
V_{in}	V_{adjust} (calculate)	V_{adjust} (simulation)	Error%	V_{adjust} (simulation)	Error%	V_{adjust} (simulation)	Error%
-0.1	-0.4	-0.3919	2.025	-0.356	11.5	-0.398	0.475
-0.06	-0.24	-0.2351	2.042	-0.201	16.3	-0.239	0.417
-0.03	-0.12	-0.1175	2.083	-0.102	15.0	-0.119	0.333
-0.01	-0.04	-0.03917	2.075	-0.034	15.0	-0.039	0.350
0.03	0.12	0.1175	2.083	0.105	12.5	0.119	0.333
0.06	0.24	0.2348	2.167	0.211	12.1	0.239	0.333
0.1	0.4	0.3911	2.225	0.330	17.5	0.398	0.325

It is observed that error% is about 2% with 1.8V power supply and gain of 51.8dB, while it is up to 17% with 1.0V power supply and gain of 52.3dB. However, the error% is reduced to 0.5% when increase the gain to 65.2dB and keep 1.0V power supply. Hence, the gain of sub-threshold should be larger than the one from super-threshold to get closely error percentage.

Table 3.3 Performance comparisons in op-amp with different power supply

Working region	v_{dd} (v)	v_{ss} (v)	v_{bias} (v)	Gain (dB)	PM (deg)	UGB (MHz)	CMRR (--)	PD (W)	SR (v/uS)	C_L (pF)
Super-threshold	0.9	-0.9	-0.2067	51.8	108.8	138.7M	58.4	921 μ	131	1
Sub-threshold	0.5	-0.5	-0.2116	65.15	59	579k	1810	620n	0.3	1
Sub-threshold	0.4	-0.4	-0.1789	65.19	61	99.3k	1614	76.8n	0.05	1
Sub-threshold	0.3	-0.3	-0.1349	63.85	62	20.4k	1185	11.4n	0.009	1

Table 3.3 gives the comparison of simulation results for op-amp between super-threshold and sub-threshold, where DC analysis, AC analysis and transient analysis are applied for the op-amp. First, doing DC analysis is to find the V_{bias} value for $V_{out}(DC) = 0$, second doing AC analysis by sweeping the frequency to measure gain, phase margin

(PM) and unit gain bandwidth (UGB), common mode range ratio (CMRR). Finally, the slew rate also recorded using transient analysis.

It can be seen from Table 3.3 that the power consumption (PD) is reduced almost four orders (from 921 μ W to 11.4nW) when the power supply is decreased from 1.8V to 0.6V. Op-amp also operating in acceptable frequency (UGB=20.4k) even with 0.6V power supply. So sub-threshold technology is quite attractive for the applications of ultra low power and low speed.

3.2.2 Sub-threshold CVC Design

As shown in Fig. 3.4, CVC includes two stages. The first stage converts the current directly into voltage V_0 based on Ohm's Law. The second stage includes DC shift, 1st stage amplification and 2nd stage amplification.

Fig. 3.4 Block diagram of CVC

• Stage 1 Design

The basic principle for detecting current signal is the conversion of current to voltage. Ideally current signal can be treated as current source (I_{in} see Fig. 3.5) with very

large inner resistance. The principle diagram in which positive terminal connects to the ground measuring current signal can be seen in Fig. 3.5.

Fig. 3.5 Diagram for traditional I-V converter

The output voltage is proportional to the input current if input impedance and open-loop gain are infinite:

$$V_0 = -I_{in}R \quad (3.5)$$

Theoretically, relatively large output voltage would be obtained if resistor R is large enough even though input current signal is pretty weak. For example, $R = 10^{12} \Omega$, $I_{in} = 1pA$, then $V_0 = -I_{in}R = -1V$. However, the totally ideal operational amplifier does not exist in reality, as the input impedance is not infinite and the increasing in R is also limited by the input impedance. Meanwhile, the variation of manufacture technology and process should also be given a consideration, such as offset voltage V_{offset} , leakage current I_B and etc. Actually, considering the leakage current I_B , the output voltage of Fig. 3.5 becomes $V_0 = -(I_{in} - I_B)R$, if I_B is larger than I_{in} , then I_{in} will not be measured. Additionally, the open-loop gain is not infinite. The characteristic of relationship between input and output is expressed as following equation:

$$V_0 = -I_{in}R + \left(V_{offset} - \frac{V_0}{A_v} \right) + I_B R \quad (3.6)$$

From Eq. (3.6), it can be seen that several conditions should be satisfied if measuring weak current signal, they are listed as follows:

- ◇ Input impedance $R_{in} \gg$ feedback resistor R
- ◇ Leakage current $I_B \ll$ input current I_{in}
- ◇ Small offset voltage V_{offset} and temperature drift

For using sub-threshold technique, leakage current will no longer be able to be ignored, and must be considered.

However, in this thesis, the above requirements are not needed as the op-amp is not included in I-V conversion part. As illustrated in Fig. 3.6, one terminal of the sensor connects to the ground ($V_{ref}=0$), the other one connects to the drain terminal of transistor M_1 . V_{ctrl} and V_s are the gate voltage and source voltage of M_1 respectively. After I-V conversion, the voltage signal V_0 goes into unit gain buffer to avoid the feedback current to the sensor and the next application stage which will be discussed later. The active transistor working in linear region can be treated as a resistor, so the circuit (a) in Fig. 3.6 can be simplified as (b) in Fig. 3.6. Based on the principle of Ohm's Law ($V=IR$), and the current from sensor can be developed by Eq. (3.7),

$$I_{sensor}R_{M1} = V_0 - V_s \quad (3.7)$$

The main advantage of this design is the current will flow directly from V_d to V_s terminal, no DC current will flow to and from the unit gain buffer due to the inherent capacitor at the gate terminal of the transistor.

Fig. 3.6 Model for Sensor and transistor

Considering the inherent capacitor for gate of transistor, a long settling time is needed before outputs a steady voltage value for weak current. This will be an issue when operating in the high speed (MHz, GHz) applications. However, the design of this circuit is applied in low speed area: biochemical sensing and chemical detecting and etc.

Another obviously advantage of using active resistor can be observed when considering the process error. As we know, process variation will cause the resulting resistance to differ from the one expected during the CMOS fabrication process, which will reduce the accuracy for the subsequent stages. However, with the using of active transistor M_1 , the resistance value can be adjusted through a control voltage V_{gs} . In this design, V_{ctrl} is the gate voltage and V_s is the source voltage for transistor M_1 . The expression to the resistance value of active transistor working in linear region is show in Eq. 3.8.

$$R_{M1} = \frac{L}{\beta W (V_{gs} - V_t)} \quad (3.8)$$

$$V_{gs} > V_t \text{ and } V_{ds} < V_{gs} - V_t$$

Where

L Length of transistor

W Width of transistor

V_{gs} Voltage from gate to source

β A function of electron mobility or hole mobility and oxide thickness.

Fig. 3.7 I-V Performance Evaluation with Input Current Sweep

The circuit in Fig. 3.6 is implemented by using 180nm CMOS technology, where the sensor is modeled as a varying current source. Fig. 3.7 is the simulation result with V_0 versus current. As seen in Fig. 3.7, an ideal current source is used to test the I-V conversion circuit with input currents of 0 to 100 nA. The purpose is to adjust the transistor width to length ration for M_1 that yields a resistance of around 1 M Ω to cover the potential current range of the sensor. The value used for the control voltage V_{gs} is also another important design parameter to ensure the transistor operates in linear region. The results are shown in Fig. 3.7 and Table 3.4. Note that the voltage drop across the transistor M_1 is $V_0 - V_g$. For a given value of 1M Ω ($R_{M1_estimated}$), 1nA of current will

be converted to approximately 1mV. Therefore, it is important to preserve the linear relationship between the input current and output voltage V_0 . As shown in table 3.4, the conversion error is given by,

$$Conversion\ Error\% = \frac{|R_{M1_{simulated}} - R_{M1_{estimated}}|}{R_{M1_{estimated}}} \times 100\% \quad (3.9)$$

$$\text{Where } R_{M1_{simulated}} = (V_0 - V_s) / I_{M1_{simulated}}$$

It can be seen that the conversion error is about 5% when the input current below 60nA, so in the following analysis, estimated value of 1 M Ω for R_{M1} will be used. Meanwhile, the variation of R_{M1} can be calibrated to generate data similar to the Table 3.4 after fabrication.

Table 3.4 I-V performance Evaluation with Input Current

I_{input} (nA)	V_{out} (mV)	V_s (mV)	V_{conv_M} (mV)	Simulated Resistance R_{M1} (M Ω)	Conversion Error %
0	-400	-400	0	0.000	0.0
1	-399	-400	1	1.000	0.0
2	-398	-400	2	1.000	0.0
3	-397.1	-400	2.9	0.967	3.3
4	-396.1	-400	3.9	0.975	2.5
5	-395.1	-400	4.9	0.980	2.0
6	-394.1	-400	5.9	0.983	1.7
7	-393.1	-400	6.9	0.986	1.4
8	-392.1	-400	7.9	0.988	1.2
9	-391.2	-400	8.8	0.978	2.2
10	-390.2	-400	9.8	0.980	2.0
20	-380.1	-400	19.9	0.995	0.5
30	-369.8	-400	30.2	1.007	0.7
40	-359.2	-400	40.8	1.020	2.0
50	-348.3	-400	51.7	1.034	3.4
60	-337.1	-400	62.9	1.048	4.8
70	-325.5	-400	74.5	1.064	6.4
80	-313.6	-400	86.4	1.080	8.0
90	-301.2	-400	98.8	1.098	9.8
100	-288.6	-400	111.4	1.114	11.4

- Stage 2 Design

In Fig. 3.4, stage 2 design comprises of DC level shift block and 1st stage amplification, and the 2nd stage amplification. DC shift is used to set the middle value of V_0 to be zero.

Fig. 3.8 is the circuit of combined DC level shift and 1st stage amplification, after DC level shift, the voltage signal V_0 added by the absolute value of V_{mid} (the median value of V_0), meanwhile it is also amplified by A_{v1} (the gain of first stage amplification) times, the relationship is expressed as Eq. (3.12).

Fig. 3.8 DC level shift and 1st stage amplification of CVC

Assume it is an ideal op-amp, we obtain

$$\frac{V_0 - V_1}{R_2} = \frac{V_{adjust} - V_0}{R_1} \quad (3.10)$$

Then

$$V_1 = \left(1 + \frac{R_2}{R_1}\right) V_0 - \frac{R_2}{R_1} V_{adjust} \quad (3.11)$$

Set $V_0 = V_{mid}$, to get V_1 be zero,

$$V_{adjust} = \left(1 + \frac{R_1}{R_2}\right) V_0. \quad (3.12)$$

With this V_{adjust} value, DC level shifter shifts middle value of V_0 to zero, which means shifting all the values of V_0 by $|V_{mid}|$. Note that V_{mid} is a negative number because $V_{ref} = 0$ in Fig. 3.6.

Thus
$$V_1 = (V_0 - V_{mid})A_{v1} \quad (3.13)$$

Where
$$A_{v1} = 1 + \frac{R_2}{R_1} \quad (3.14)$$

However, for sub-threshold region, the leakage current to the gate must be considerate. So Eq. (3.11) is no longer valid. According simulation results, a modification factor is added in Eq. (3.11)

$$V_1 = \left(1 + \frac{R_2}{R_1}\right)V_0 - \frac{R_2}{R_1}(V_{adjust} + \delta) \quad (3.15)$$

Comparing Eq. (3.11) and Eq. (3.15), it is find that V_1 would still be zero by adjusting V_{adjust} even though the Equation changed.

Fig. 3.9 is the schematic circuit of a unit gain buffer, where the inverting terminal and output terminal are connected together, is given by,

$$V_{adjust} = V_1 \quad (3.16)$$

Fig. 3.9 Unit Gain Analog Buffer

Substituting Eq. 3.16 into Eq. 3.11 yields,

$$V_1 = \left(1 + \frac{R_2}{R_1}\right)V_0 - \frac{R_2}{R_1}V_1 \quad (3.17)$$

Simplify Eq. (3.17), finally get,

$$V_1 = V_0 \quad (3.18)$$

Hence, unit gain analog buffer is obtained just simply connecting inverting terminal and output terminal each other. Note that V_0 is the input signal while V_1 is the output signal.

To provide extra gain for the weak voltage signal, a second stage amplifier is added. As discussed before, the gain is highly related to the ratio of resistance, see Eq. (3.14). High gain requires large ratio of $\frac{R_2}{R_1}$, then the resistance will pretty large and increase the hardware overhead needed for fabricating on-chip. However, if using multi-stage gain distribution, the resistor value will be reduced a lot while still satisfy overall gain required in the second stage. The schematic of second stage amplification depicted in Fig. 3.10 includes three stages of operational amplifiers in non-inverting configuration. Each stage's gain is the ratio of resistor they are given by,

Fig. 3.10 Schematic of 2nd stage amplification

$$Av_{2_1} = \frac{R_2}{R_1} \quad (3.19)$$

$$Av_{2_2} = \frac{R_4}{R_3} \quad (3.20)$$

$$Av_{2_3} = \frac{R_6}{R_5} \quad (3.21)$$

The entire gain Av_2 for second stage is the product of smaller gain of three sections (Av_{2_1} , Av_{2_2} and Av_{2_3} , as described in Fig. 3.10), and is given by,

$$Av_2 = Av_{2_1}Av_{2_2}Av_{2_3} \quad (3.22)$$

The Cadence schematic simulation result shows that the gain for the second stage is approximately 15.822.

3.2.3 Sub-threshold AGC Design

Fig. 3.11 is the block diagram of sub-threshold automatic gain control (AGC). The AGC circuit is designed to control the system gain and increase the ROIC interfacing sensor dynamic range. It includes three differential op-amps (Diff_comp), labeled as C1, C2 and C3, and two multiplexers, where Diff_comp block includes a comparator and a D type flip flop and Mux block is a 2-to-1 multiplexer, clk is the clock signal into the Diff_comp. The input voltage signal V_1 is directly coming from the DC shift and first stage amplification as shown in Fig.1, and its amplitude range is from -160mV to 160mV. The polarity of V_1 is to be determined by the comparator C1 which is included in Dif_comp, where non-inverting terminal connecting to the ground. Meanwhile, V_1 also goes into comparators C2 and C3 to compare with the negative reference voltage ($V_{ref1}=-10\text{mV}$) and positive reference voltage ($V_{ref2}=10\text{mV}$) respectively. The reference voltage can be adjusted according to the designing requirements for different applications.

After comparing with the reference voltage V_{ref1} and V_{ref2} , two outputs (S2 and S3) from comparator C2 and C3 are obtained. One of the outputs S2 or S3 will be picked up depends on the polarity of V_1 . For instance, if $V_1 < 0$, then S1=1 and S3 will be selected by multiplexer m1. If $V_1 > 0$, then S1=0 and S2 will be selected by multiplexer m1.

$$V_{out} = (V_0 - V_{mid})(A_{v1}(1 - S) + A_{v1}A_{v2}S) \quad (3.26)$$

Considering

$$V_{out} = A_v(V_0 - V_{mid}) \quad (3.27)$$

Thus the equivalent gain (the gain after applying AGC) is,

$$A_v = A_{v1}(1 - S) + A_{v1}A_{v2}S \quad (3.28)$$

From Eq. (3.28), it is clearly found that automatic gain control is well implemented.

For example, if $S=0$, then the total gain $A_v = A_{v1}$, else if $S=1$, then the total gain

$A_v = A_{v1}A_{v2}$. The simulation results can be seen in Fig. 3.12 and Table 3.5.

Table 3.5 Results of CVC ($V_{dd}=0.4V$, $V_{ss}=-0.4V$)

I_{in} (nA)	V_0 (mV)	V_1 (mV)	V_2 (mV)	V_{out} (mV)	S	A_{v1}	A_{v2}	A_v	V_{mid} (mV)	V_{ctrl} (mV)	V_s (mV)
60.0	-236.3	161	-197.2	161	0	5.063	15.198	5.063	-268.1	400	-300
54.1	-243.2	125.8	-197.2	125.9	0	5.063	15.198	5.063	-268.1	400	-300
48.1	-250.1	90.94	-197.2	91.04	0	5.063	15.198	5.063	-268.1	400	-300
42.1	-256.8	56.95	-197.2	57.07	0	5.063	15.198	5.063	-268.1	400	-300
36.1	-263.4	23.77	-197.2	23.85	0	5.063	15.198	5.063	-268.1	400	-300
30.1	-269.8	-8.659	-131.6	-131.6	1	5.063	15.198	76.9475	-268.1	400	-300
24.1	-276.1	-40.38	368.2	-40.38	0	5.063	15.198	5.063	-268.1	400	-300
18.1	-282.2	-71.44	399.7	-71.44	0	5.063	15.198	5.063	-268.1	400	-300
12.1	-288.2	-101.9	399.7	-101.9	0	5.063	15.198	5.063	-268.1	400	-300
6.1	-294.1	-131.7	399.7	-131.7	0	5.063	15.198	5.063	-268.1	400	-300
0.1	-299.9	-161	399.7	-161	0	5.063	15.198	5.063	-268.1	400	-300

Fig. 3.12 Transient analysis for ROIC ($V_{dd}=0.4V$, $V_{ss}=-0.4V$): (a) is the current from sensors using PWL current, (b) is the intermediate output of CVC after DC shift & 1st stage amplification, (c) is the output of CVC after 2nd stage amplification without using AGC, (d) is the final output of CVC using AGC.

As listed in table 3.5, I_{in} is the current to be detected from sensor ranging from 100pA to 60nA; V_0 is the voltage after I-V conversion which are all negative number; V_1 is the voltage after 1st stage amplification, which are shifted by median value of V_0 and also amplified by 5.063 times; V_2 is the voltage after 2nd stage amplification without AGC, most of value are out of the input range of ADC; A_{v1} is the gain of 1st stage amplification; A_{v2} is the gain of 2nd stage amplification; A_v is the gain after applying AGC; S is the control signal from AGC, it is clearly observed that when the signal after first stage amplification is still low enough, for example, $V_1=-8.658mV$ (marked red color in table) within the range of -10mV to 10mV, control signal will be 1 and the V_1 will be

amplified by extra 15.158 times. In the last right two columns (V_{ctrl} and V_s) are the input control terminals to maintain a $1M\Omega$ resistance for the active transistor M1. V_{mid} is the median value of V_{1max} and V_{1min} , and is used to determine the adjustment voltage for DC shift.

Fig. 3.12(a) depicts output current from sensors ranging from 100pA to 60nA. As illustrated in Fig. 3.12(b), after DC level shift and 1st stage amplification, the current are converted to voltage signal ranging from -161 mV to 161 mV, which is within the input range of ADC (-0.2V to 0.2V). Fig. 3.12(c) and (d) show the output voltage without using AGC and using AGC respectively, it is observed that lots of current signal can't be detected without using AGC, as output voltage after 2nd stage amplification reach in saturation. However, after applying AGC, all the current are well detected and transferred to voltage signal. If the converted signal (V_1) is too weak (for instance, $|V_1|=8.658mV$, less than 10mV), then the control signal blue line in Fig. 3.12(d) from AGC change to high level, and V_1 will be amplified by further stage to reach in -131.6mV. If signal V_1 is over 10mV, then control signal will be at low level. Finally, V_1 serves as the final analog output of ROIC.

The results in Fig. 3.12 and Table 3.5 are simulated under 0.8V power supply. Considering the large improvement in power consumption by reducing the power supply, can we keep reducing the power supply to $V_{dd}=0.3V$, $V_{ss}=0.3V$? However, AGC is no longer operating normally, as depicted in Fig. 3.13, the control signal is always at high level, nothing related to the value of V_1 coming from the DC shift and first stage amplification as shown in Fig. 3.1. Hence, some modifications are required to make the CVC work in the future.

Fig. 3.13 Final analog Output signal (V_{out})

As discussed in chapter 2.2.1, the input range of ADC is related to the power supply. With the power supply scaling down, correspondingly the input range is reducing. Therefore, to improve the entire performance of ROIC, multi-power supply is recommended. For example, distributes 0.8V to CVC and 1.0V to ADC.

3.2.4 Calibration Method

To convert voltage back to current, calibration method is applied after read the voltage output from ROIC. After calibration, it is convenient to use compensation technology to improve the accuracy of current detecting.

Fig. 3.14 shows the block diagram of Read-Out Integrated Circuit including active transistor, 1st stage and 2nd stage amplification, AGC, Multiplexer, Buffer and ADC.

Fig. 3.14 Block Diagram of ROIC

Where

I_{in} = the current to be detected from sensor

V_0 = the voltage after I-V conversion

V_1 = the voltage after 1st stage amplification

V_2 = the voltage after 2nd stage amplification

A_{v1} = the gain of 1st stage amplification

A_{v2} = the gain of 2nd stage amplification

A_v = the gain after applying AGC

S = the control signal from AGC

V_{analog} = the analog output signal

$V_{digital}$ = the digital output signal

The voltage drop across active transistor M1 is $(V_0 - V_s)$, and applying Ohm's Law, we obtain

$$I_{sensor}R_{M1} = V_0 - V_s \quad (3.29)$$

Reviewing Chapter 3.2.3, the relationship among A_v , A_{v1} , A_{v2} and S is given by,

$$A_v = A_{v1}(1 - S) + A_{v1}A_{v2}S \quad (3.30)$$

Since

$$V_{out} = A_v(V_0 - V_{mid}) \quad (3.31)$$

Substituting Eq. (3.30) into Eq. (3.31) yields

$$V_{out} = (V_0 - V_{mid})(A_{v1}(1 - S) + A_{v1}A_{v2}S) \quad (3.32)$$

Thus we have

$$V_0 - V_{mid} = \frac{V_{out}}{A_{v1}(1-S) + A_{v1}A_{v2}S} \quad (3.33)$$

$$V_0 = \frac{V_{out}}{A_{v1}(1-S) + A_{v1}A_{v2}S} + V_{mid} \quad (3.34)$$

Combining Eq. (3.29) and Eq. (3.34), then get

$$I_{sensor}R_{M1} = \frac{V_{out}}{A_{v1}(1-S) + A_{v1}A_{v2}S} + V_{mid} - V_s \quad (3.35)$$

Finally

$$I_{sensor} = \frac{1}{R_{M1}} \left(\frac{V_{out}}{A_{v1}(1-S) + A_{v1}A_{v2}S} + V_{mid} - V_s \right) \quad (3.36)$$

Hence, if given the value of A_{v1} , A_{v2} , S , V_{mid} , V_s and measured result V_{out} , then the current can be readily obtained.

For example, $A_{v1}=5.089$, $A_{v2}=15.822$, $V_s=-400\text{mV}$. From simulation of DC analysis using ideal current source ranging from 100pA to 60nA, we get $V_{0min}=-399.9\text{mV}$, $V_{0max}=-337.1\text{mV}$, and also know the value of active transistor $R_{M1}=1\text{M}\Omega$, then

$$V_{mid} = 0.5(V_{0min} + V_{0max}) = -368.5\text{mV} \quad (3.37)$$

From transient analysis, the measured output voltage is 159.5mV and -93.87mV respectively

Case 1 $I_{input}=60\text{nA}$, $V_{out} = 159.5\text{mV}$ and $S=0$, then

$$I_{sensor} = \frac{1}{R_{M1}} \left(\frac{V_{out}}{A_{v1}(1-S) + A_{v1}A_{v2}S} + V_{mid} - V_s \right)$$

$$= \frac{1}{1M} \left(\frac{159.5mV}{5.089(1-0)+5.089 \times 15.822 \times 0} - 368.5mV + 400mV \right) \quad (3.38)$$

$$= 62.84nA$$

Case 1 $I_{input}=30nA$, $V_{out} = -93.87mV$ and $S=1$, then

$$I_{sensor} = \frac{1}{R_{M1}} \left(\frac{V_{out}}{A_{v1}(1-S)+A_{v1}A_{v2}S} + V_{mid} - V_s \right)$$

$$= \frac{1}{1M} \left(\frac{-93.87mV}{5.089(1-1)+5.089 \times 15.822 \times 1} - 368.5mV + 400mV \right) \quad (3.39)$$

$$= 30.33nA$$

Similarly, all the measured output voltage can be converted back to current using Eq. (3.36). More calculations are tabulated in Table 3.6 and Table 3.7.

Table 3.6 Comparison of input and calibrated current ($V_{dd}=0.5V$, $V_{ss}=-0.5V$)

I_{in} (nA)	V_{out} (mV)	S	V_{mid} (mV)	Av	I_{cal} (nA)	Error (%)
60.0	159.5	0	-368.5	5.089	62.8421	4.7368
54.1	125.9	0	-368.5	5.089	56.2396	3.9549
48.1	92.03	0	-368.5	5.089	49.5841	3.0855
42.1	58.86	0	-368.5	5.089	43.0661	2.2948
36.1	26.34	0	-368.5	5.089	36.6759	1.5952
30.1	-93.87	1	-368.5	80.5182	30.3342	0.7779
24.1	-37.58	0	-368.5	5.089	24.1155	0.0640
18.1	-68.76	0	-368.5	5.089	17.9885	0.6160
12.1	-99.53	0	-368.5	5.089	11.9421	1.3047
6.1	-129.9	0	-368.5	5.089	5.97435	2.0597
0.1	-159.8	0	-368.5	5.089	0.09894	1.0611

Fig. 3.15 Comparison between Readout and Input current ($V_{dd}=0.5V$, $V_{ss}=-0.5V$)

As seen in Table 3.6, comparison between input current and calibrated current with 1V power supply ($V_{dd}=0.5V$, $V_{ss}=0.5V$), where the input current I_{in} , the converted back current I_{cal} , and percentage error are listed. When control signal $S=1$, automatic gain control is in effective and changes the gain 5.089 to 80.5182. So the weak voltage signal amplified by one more stage. In the column (Error%), the maximum error percentage is 4.7%. Fig. 3.15 shows the comparison between input current and converted back current, it is observed that error percentage is increasing when input current over 36.1nA, and reach in maximum value when $I_{in}= 60nA$.

Table 3.7 shows the information about input current and calibrated output current with 0.8V power supply ($V_{dd} = 0.4V$, $V_{ss} = -0.4V$). Note that the gain for the 1st stage and 2nd stage has a little bit difference with the gain provided by 1.0V power supply. The maximum error percentage 6.16% is also increased when served with a lower power

supply. Similarly, as depicted in Fig. 3.16, the error percentage is increasing when input current is over 42.1nA, and get the peak value when $I_{in}=60\text{nA}$.

Table 3.7 Comparison of input and calibrated current ($V_{dd}=0.4\text{V}$, $V_{ss}=-0.4\text{V}$)

I_{in} (nA)	V_{out} (mV)	S	V_{mid} (mV)	A_v	I_{cal} (nA)	Error (%)
60.0	161	0	-268.1	5.063	63.6993	6.1655
54.1	125.9	0	-268.1	5.063	56.7667	4.9292
48.1	91.04	0	-268.1	5.063	49.8814	3.7036
42.1	57.07	0	-268.1	5.063	43.1719	2.5463
36.1	23.85	0	-268.1	5.063	36.6106	1.4145
30.1	-131.6	1	-268.1	76.9475	30.1897	0.2981
24.1	-40.38	0	-268.1	5.063	23.9245	0.7283
18.1	-71.44	0	-268.1	5.063	17.7898	1.7138
12.1	-101.9	0	-268.1	5.063	11.7736	2.6976
6.1	-131.7	0	-268.1	5.063	5.88775	3.4794
0.1	-161	0	-268.1	5.063	0.10067	0.6715

Fig. 3.16 Comparison between Readout and Input current ($V_{dd}=0.4\text{V}$, $V_{ss}=-0.4\text{V}$)

3.2.5 Optimization applying compensation technology

- Establishment of fitting function for compensation factor α

Compensation factor α is derived from the analysis of simulation results, which is added to the initial calibrated current to reduce the error of current detecting. More details are discussed in the section.

Table 3.8 Comparison of input current and calibrated output current after compensation

$$(V_{dd}=0.5V, V_{ss}=-0.5V)$$

I_{in} (nA)	V_{out} (mV)	$I_{calibrated}$ (nA)	$(I_{calibrated} - I_{input})$ nA	Compensation Factor α (nA)	Error%(before Compensation)	Error%(after compensation)
60	159.5	62.84211	2.84211	2.8	4.736851	0.070184
58	148	60.58233	2.58233	2.6	4.452301	0.030458
56	136.6	58.34221	2.34221	2.4	4.182516	0.103199
54	125.2	56.10208	2.10208	2.2	3.892746	0.181328
52	113.9	53.88161	1.88161	2.0	3.618476	0.227678
50	102.7	51.68078	1.68078	1.8	3.361564	0.238436
48	91.48	49.47603	1.47603	1.6	3.075056	0.258278
46	80.36	47.29092	1.29092	1.4	2.806351	0.237127
44	69.3	45.11761	1.11761	1.2	2.540015	0.187258
42	58.31	42.95805	0.95805	1.0	2.281064	0.099889
40	47.37	40.80831	0.80831	0.8	2.02078	0.020780
38	36.49	38.67037	0.67037	0.6	1.764125	0.185178

To find an appropriate fitting function for compensation factor, more simulation data are connected. From Fig. 3.15 and Fig. 3.16, we already known that the error percentage is increasing when input current larger than 36.1nA. As tabulated in Table 3.8, the comparison of input current and calibrated output current after compensation with $V_{dd}=0.5V$, $V_{ss}=0.5V$, where the error percentage from 1.76% increases up to 4.73% while input current varies from 38nA to 60nA. It is observed that all the calibrated output current is larger than the input one, and difference steadily goes from 0.67 to 2.84.

If we give a compensation factor to the calibrated current subtracting $I_{calibrated}$ by an arithmetic progression (as shown in table 3.10, the initial term is 0.6V, the common difference is 0.2V), then all the error percentage are decreased, especially the maximum error percentage degrading from 6.16% to 0.25%. Therefore, it is very helpful to reduce the error using compensation technique.

For convenient, the minimum calibrated output current is expressed by I_{omin} (38.67nA) and the maximum output current is written as I_{omax} (62.84nA) when input current varies from 30nA to 60nA. Similarly, the smallest and largest compensation factor is seen as α_{min} (0.6nA) and α_{max} (2.8nA) respectively. Considering the discussion above, the compensation factor α can be calculated as below,

Compensation factor:

$$\alpha = \alpha_{min} + \frac{I_0 - I_{omin}}{I_{omax} - I_{omin}} (\alpha_{max} - \alpha_{min}) \quad (3.40)$$

For example, the calibrated current is $I_0=48\text{nA}$, substituting all the parameters into Eq. (3.40) yields,

$$\alpha = 0.6\text{nA} + \frac{48 - 38.67}{62.84 - 38.67} (2.8 - 0.6)\text{nA} = 1.449\text{nA} \quad (3.41)$$

Comparing α calculated by Eq. (3.40) to the one (1.6nA) from Table 3.8, both of them are pretty close.

Similarly, the same analysis is applied for the comparison of input current and calibrated output current after compensation with $V_{dd}=0.4\text{V}$, $V_{ss}=-0.4\text{V}$, as shown in Table 3.9, where the error percentage from 1.72% increases up to 6.16% while input current varies from 38nA to 60nA. It is observed that all the calibrated output current is

larger than the input one, and difference steadily goes from 0.65 to 3.70. If we give a compensation factor to the calibrated current subtracting $I_{calibrated}$ by an arithmetic progression (as shown in table 3.11, the initial term is 0.85V, the common difference is 0.25V), then all the error percentage are decreased, especially the maximum error percentage degrading from 6.16% to 0.74%.

Table 3.9 Comparison of input current and calibrated output current after compensation

$$(V_{dd}=0.4V, V_{ss}=-0.4V)$$

I_{input} (nA)	V_{out} (mV)	$I_{calibrated}$ (nA)	$(I_{calibrated}$ $-I_{input})$ nA	Compensation Factor α (nA)	Error%(before Compensation)	Error%(after compensation)
60	161	63.69933	3.69933	3.60	6.165547	0.998881
58	149	61.32919	3.32919	3.35	5.739987	0.739987
56	137	58.95906	2.95906	3.10	5.284028	0.4626
54	125.2	56.62842	2.62842	2.85	4.867448	0.237818
52	113.5	54.31754	2.31754	2.60	4.456806	0.033729
50	101.9	52.02641	2.02641	2.35	4.052815	0.147185
48	90.37	49.7491	1.7491	2.10	3.643961	0.314372
46	78.95	47.49352	1.49352	1.85	3.246786	0.448866
44	67.63	45.25769	1.25769	1.60	2.858393	0.550698
42	56.39	43.03767	1.03767	1.35	2.470632	0.624606
40	45.45	40.87689	0.87689	1.10	2.192228	0.307772
38	34.19	38.65291	0.65291	0.85	1.718193	0.650228

For convenient, the minimum calibrated output current is expressed by I_{omin} (38.65nA) and the maximum output current is written as I_{omax} (63.69nA) when input current varies from 30nA to 60nA. Similarly, the smallest and largest compensation factor is seen as α_{min} (1.1nA) and α_{max} (3.1nA) respectively. In virtue of the discussion above, same fitting equation with Eq. 3.40 is obtained by only changing some initial parameters (I_{omin} , I_{omax} , α_{min} and α_{max}). For example, the calibrated current is $I_0=48$ nA, then the compensation factor will easily be acquired and has the approximately value for the ideal one.

$$\alpha = \alpha_{min} + \frac{I_0 - I_{omin}}{I_{omax} - I_{omin}} (\alpha_{max} - \alpha_{min}) \quad (3.42)$$

$$= 1.1nA + \frac{63.69 - 38.65}{63.69 - 38.65} (3.1 - 1.1)nA = 1.847nA$$

To sum up, the fitting function for compensation factor can be expressed by Eq. (3.40). Some initial parameters changes are required if power supply varied.

- Verification

Table 3.10 and Table 3.11 are the comparison in performance between before-compensation and after-compensation, where I_{cal1} is the initial calibrated output current calculated by the Eq. 3.36 before compensation, and I_{cal2} is the calibrated output current after compensation, and α is the compensation factor getting from Eq. 3.40. Note that I_{cal1} is obtained by different power supply, 1.0V in Table 3.10 while 0.8V in Table 3.11. The performance is evaluated by the error percentage of deviation to input current, which is given by,

$$Error\% = \left| \frac{I_{cal} - I_{in}}{I_{in}} \right| \times 100\% \quad (3.43)$$

To better observe the performance after applying compensation technology, all the results are drawn in Fig. 3.17 with 1.0V power supply ($V_{dd}=0.5V$, $V_{ss}=-0.5V$) and Fig. 3.18 with 0.8V power supply ($V_{dd}=0.4V$, $V_{ss}=-0.4V$).

Table 3.10 Performance comparison between before-compensation and
after compensation with power supply ($V_{dd}=0.5V$, $V_{ss}=-0.5V$)

I_{in} (nA)	Compensation Factor α (nA)	I_{cal1} (nA)(after compensation)	I_{cal2} (nA)(after compensation)	Error%(before Compensation)	Error%(after compensation)
60.0	2.80	62.8421	60.0421	4.7368	0.0702
54.1	2.08	56.2396	54.1596	3.9549	0.1101
48.1	1.58	49.5841	48.0041	3.0855	0.1994
42.1	1.08	43.0661	41.9861	2.2948	0.2705
36.1	0.00	36.6759	36.6759	1.5952	1.5953
30.1	0.00	30.3342	30.3342	0.7779	0.7780
24.1	0.00	24.1155	24.1155	0.0640	0.0643
18.1	0.00	17.9885	17.9885	0.6160	0.6160
12.1	0.00	11.9421	11.9421	1.3047	1.3049
6.10	0.00	5.97435	5.97435	2.0597	2.0598
0.10	0.00	0.09894	0.09894	1.0611	1.0611

Table 3.11 Performance comparison between before-compensation and after-
compensation with power supply ($V_{dd}=0.4V$, $V_{ss}=-0.4V$)

I_{in} (nA)	Compensation Factor α (nA)	I_{cal1} (nA)(before compensation)	I_{cal2} (nA)(after compensation)	Error%(before Compensation)	Error%(after compensation)
60.0	3.60	63.6993	60.0993	6.1655	0.1655
54.1	2.55	56.7667	54.2167	4.9292	0.2157
48.1	1.89	49.8814	47.9914	3.7036	0.2258
42.1	1.23	43.1719	41.9419	2.5463	0.3755
36.1	0.00	36.6106	36.6106	1.4145	1.5952
30.1	0.00	30.1897	30.1897	0.2981	0.7779
24.1	0.00	23.9245	23.9245	0.7283	0.0640
18.1	0.00	17.7898	17.7898	1.7138	0.6160
12.1	0.00	11.7736	11.7736	2.6976	1.3047
6.10	0.00	5.88775	5.88775	3.4794	2.0597
0.10	0.00	0.10067	0.10067	0.6715	1.0611

Fig. 3.17 Performance comparison between before-compensation and after-compensation with power supply ($V_{dd}=0.5\text{V}$, $V_{ss}=-0.5\text{V}$). Red line is the input current, blue line is the calibrated output current.

Fig. 3.18 Performance comparison between before-compensation and after-compensation with power supply ($V_{dd}=0.4\text{V}$, $V_{ss}=-0.4\text{V}$). Red line is the input current, blue line is the calibrated output current.

As depicted in Fig. 3.17 and Fig. 3.18, no observable deviation between input current and calibrated output current after compensation. From Table 3.10 and Table 3.11, it is

observed the accuracy is improved a lot when the input current over 36.1nA, additionally, maximum estimated error percentage decreased from 4.73% to 2.05% with 1V power supply, and from 6.16% to 2.05% with 0.8 power supply.

3.2.6 8-bit ADC Design

After I-V conversion, the signal will go to computer or other digital devices to do signal processing. However, analog signal is not recognized by digital devices and is also easily distorted by the noise. Consequently, an analog to digital converter is quite necessarily. As shown in Fig. 3.19, the analog signal is first sampled, quantized to a digital format of ones and zeros, and finally converted to a workable binary number format through the encoder. The digitized data can then be processed, modulated/demodulated, and transmitted through different signal.

Fig. 3.19 Analog to Digital Conversion

The flash ADC is used to implement analog to digital conversion, as shown in Fig. 3.20. For convenient, a 3-bit ADC is presented due to the same principle of 3-bit and 8-bit ADC. As learnt in CMOS analog integrated circuit design, a N-bit flash ADC consists of 2^N resistors, $2^N - 1$ comparators, and a $2^N - 1$ to N encoder. Thus 3-bit flash ADC requires 8 equal value resistors, 7 comparators and a 7-to-1 encoder [26].

Fig. 3.20 Flash Analog to Digital Convertor

The series of equal value resistors forms a voltage divider, which creates seven reference voltages to sample the analog input. Then the comparators are used to compare the input analog value with the seven reference voltages at fixed time intervals. Zero indicates that the current voltage value is less than the reference voltage compared with and one indicates the opposite. Generally, a clock with a fixed period and 50% duty cycle is used here for sampling at fixed time intervals. At the end of quantization, a 7-bit thermometer code composed of zeroes and ones is obtained, and then is converted to a workable numerical format for post processing.

Table 3.12 is used to convert the 7-bit thermometer code to 3-bit binary number. The order of bits for thermometer code is from top-to-bottom, or from most to least significant bits, in Fig. 3.20.

Table 3.12 Digital Output Codes

Decimal	Thermometer	Binary
0	0000000	000
1	0000001	001
2	0000011	010
3	0000111	011
4	0001111	100
5	0011111	101
6	0111111	110
7	1111111	111

Considering that all the components in ROIC are implemented in the 180nm CMOS technology and provided by multiple power supply (0.8V to CVC, and 1.0V to ADC), which determines the output range of I-V converter (from -0.2V to 0.2V) based on the principle explained in section 2.2.1.

In this thesis, a 8-bit flash ADC is presented. Its components include comparators, operational amplifiers, D flip flops, XOR gates, OR gates, resistors, 2-bit flash ADCs, 6-bit flash ADCs and multiplexers. The overall schematic of 8-bit flash ADC is shown in Fig. 3.21. For comparison, two different power supply ($V_{dd} = 0.9V / V_{ss} = -0.9V$ and $V_{dd} = 0.5V / V_{ss} = -0.5V$) are provided. Note that the power supply (1.0V) for ADC part is larger than the one (0.8V) in I-V conversion part. Given the output range of I-V converter is from -0.16V to 0.16V, the power supply should be around 1.0V according to the Eq. 2.19. Therefore a second power supply ($V_{dd} = 0.5V / V_{ss} = -0.5V$) applied for the ADC part.

Fig. 3.21 Schematic of 8-bit flash ADC in sub-threshold

As shown in Fig. 3.21, 8-bit ADC mainly comprises of four 6-bit ADCs and one 2-bit ADC. At first, according to 2-bit ADC, the interval $(-0.2V \text{ to } 0.2V)$, which includes the output range of I-V converter $(-0.16V \text{ to } 0.16V)$ divided by four sections, the outputs of 2-bit ADC to be served as control signal for the 4-to-1 multiplexer depends on the input signal V_{in} . For example, $0.1V < V_{in} \leq 0.2V$, then $V_{out7} = 1$, $V_{out6} = 1$, this will choose one of inputs (D3) of all the six 4-to-1 multiplexers to the next stage. More details can be found in the following sections.

Fig. 3.22 8-bit flash ADC Transient Analysis

The transient analysis of the 8-bit ADC schematic design is shown in Fig. 3.22. The input frequency here is given at 1.5625 kHz while the clock frequency is 12.5 kHz. The corresponding period is 80 μ s, therefore the ADC samples at the falling edge of the clock pulse as indicated in the Fig. 3.22 at every 80 μ s. After conversion, the above simulation results visually demonstrates that the digital signal closely match with the original analog input signal.

To evaluate the performance of the 8-bit flash ADC, spectral analysis using Discrete Fourier Transform (DFT) is also presented. Fig. 3.23, is the spectral analysis of 8-bit flash ADC. Two typical approaches are used in estimate the performance of the ADC from observing the spectrum of the digital output. Both involve measuring the power of the primary signal against other peaks in the spectrum. The line has the largest amplitude is the digitized signal at the frequency of 1.5625 kHz. The first one measures the dB

difference between the primary signal and the next highest spur, refers as the signal to noise and distortion ratio (SINAD). The spurs can be noise due to quantization or harmonics of the primary signal. As shown in Fig. 3.23, SINAD=56.07dB, which is approximately equal to 6.02 times the effective number of bits for ADC. Consequently, after minor calculation, the ENOB is nearly 8. The second one measures the dB difference between the primary signal and the next highest noise spur (excluding the harmonics of the primary signal), here calls the spurious free dynamic range (SFDR).

Fig. 3.23 The Discrete Fourier Transform (DFT) Analysis for 8-bit flash ADC

SFDR=76.34dB, which is 9 times the effective number of bits for ADC. Therefore, the same approximately value for ENOB (8) is obtained. The test here just verifies the ADC operating normal at the frequency of 1.5625 kHz, it may not the case with higher sampling frequency, however, note that the sampling frequency is 1.5625 kHz, which is faster than the required sampling frequency of sensor with slow changing speed.

3.3 Simulation Results

3.3.1 Comparison in power consumption

Table 3.13 Comparisons in power consumption

	Working region	V_{dd} (v)	V_{ss} (v)	V_{bias} (v)	f_{in} (kHz)	f_{clk} (kHz)	Working Or not	Power (W)
Current-to -Voltage converter (CVC)	Super-threshold	0.9	-0.9	-0.35	1	10	Yes	4.31m
	Super-threshold	0.5	-0.5	-0.2116	1	10	Yes	0.13m
	Sub-threshold	0.4	-0.4	-0.1789	1	10	Yes	0.53 μ
	Sub-threshold	0.3	-0.3	-0.1349	1	10	No	0.21 μ
8-bit Flash ADC	Super-threshold	0.9	-0.9	-0.35	1.5625	12.5	Yes	22.1m
	Super-threshold	0.5	-0.5	-0.2116	1.5625	12.5	Yes	0.85m
	Sub-threshold	0.4	-0.4	-0.1789	1.5625	12.5	Yes	0.46m
Total ROIC	CVC	0.4	-0.4	-0.1789	0.1	10	Yes	25.2m
	ADC	0.5	-0.5	-0.2116	0.1	1	Yes	
	CVC	0.9	-0.9	-0.35	0.1	10	Yes	0.89m
	ADC	0.9	-0.9	-0.35	0.1	1	Yes	

In Table 3.13, the comparisons in power consumption (PD) are obtained by using transient analysis, where f_{in} and f_{clk} is the input frequency and clock frequency. As listed in Table 3.13, f_{in} and f_{clk} keep their value fixed while the power supply is varied to avoid the influence for the comparison in PD. It is found that when power supply reduces from 1.8V to 1.0V, the PD for CVC goes down from 4.31mW to 0.13mW, and for ADC decreases from 22.1mW to 0.85mW. The power dissipation for both CVC and ADC save up to 96%. If the power supply is reduced to 0.8V ($V_{dd}=0.4V$, $V_{ss}=-0.4V$), then some transistors will begin to reach in sub-threshold region, and more energy will be saved. As shown in Table 3.13, the power consumption for CVC is reduced one order of magnitude (from 0.13mW by using 1.0V power supply to 0.53 μ W by using 0.6V power supply), and for ADC is reduced 50% more (from 0.85mW by using 1.0V power supply to 0.46mW by using 0.8V power supply). If the power supply reduced to 0.6V, the AGC

unit is no long working normally. The total PD of ROIC is also saved up to 96% (from 25.2mW by using 1.8V power supply for both CVC and ADC to 0.89mW by using 0.8V power supply to CVC and 1.0V power supply to ADC).

3.3.2 Evaluation for entire system

Fig. 3.24 Schematic of Read-Out Integrate Circuit (ROIC)

Fig. 3.24 is the schematic circuit of ROIC, where two power supplies (0.8V for CVC and 1.0V for ADC) are provided, I_{sensor} (ranging from 0.1nA to 24.1nA) is the input current from sensor, V_{analog} and $V_{digital}$ are the analog output and digital output respectively. The current is firstly transferred to voltage (V_{analog}) and then converted to digital signal after analog to digital converter. The simulation results can be seen in Fig. 3.25 and Fig. 3.26.

Fig. 3.25 Analog and weighted sum digital output ($f_{in}=100$ Hz)

Fig. 3.26 Comparison between analog and weighted sum digital output ($f_{in}=100$ Hz)

Note that the digital output in Fig. 3.25 and Fig. 3.26 is the weighted digital outputs (bout7~bout0). Fig. 3.25 shows the analog output (V_{analog}) and digital output ($V_{digital}$), where $V_{digital}$ is calculated by the Eq. 3.44. Fig. 3.26 shows the comparison between

$$V_{digital} = (bout0 + bout1 * 2 + bout2 * 4 + bout3 * 8 + bout4 * 16 + bout5 * 32 + bout6 * 64 + bout7 * 128) * \frac{2V_{ref}}{1.0 * 255} - V_{ref} \quad (3.44)$$

analog output and digital output. The comparison evaluated by the error percentage is given by Eq. 3.45,

$$Error\% = \frac{|V_{digital} - V_{analog}|}{V_{analog}} \times 100\% \quad (3.45)$$

Table 3.14 tabulates the input current from sensor replaced by the Piece Wise Linear (PWL) current source ($f_{in}=100\text{Hz}$), analog output, digital output codes, weighted sum digital output and error percentage. It can be seen that digitized output signal matches well with the analog output, as the maximum error percentage is less than 1% (less than 1LSB). Note that 1 LSB=0.4V/256=1.5625mV. Fig. 3.27 is the Analog Outputs with different input frequency varying from 100 Hz to 1 kHz. It is observed that the analog output is acceptable (comparing to PWL) and the digital output is also following the analog output when given 400 Hz input frequency. However, the analog output can't reach in steady status as the rising time is almost equal the period of output signal when given 1 kHz input frequency. Hence the maximum operating frequency for the proposed ROIC in this thesis can be reached at 400Hz. In the future, if require higher operating frequency, buffer tree should be added between CVC and ADC to drive large quantities of comparators in flash ADC.

Fig. 3.27 Analog Outputs and weighted digital outputs with different input frequency: (a)

$f_{in} = 100$ Hz (b) $f_{in} = 400$ Hz (c) $f_{in} = 700$ Hz (d) $f_{in} = 1$ kHz

Table 3.14 Input current ($f_{in} = 100$ Hz), analog output and digital output

I_{sensor} (nA)	V_{analog} (mV)	$V_{digital}$ (V7~V0)	$V_{digital}$ (mV) (Weighted Sum)	$(V_{analog} - V_{digital})$ (mV)	Error (%)
0.1	-161.3	00011000	-162.4	1.10(<1 LSB)	0.681959
6.1	-131.8	00101011	-132.5	0.70(<1 LSB)	0.531108
12.1	-101.9	00111110	-102.7	0.80(<1 LSB)	0.785083
18.1	-71.43	01010010	-71.37	0.06(<1 LSB)	0.083998
24.1	-40.37	01100110	-40.00	0.37(<1 LSB)	0.916522

4 CONCLUSION AND FUTURE WORK

4.1 Conclusion

A novel read-out integrated circuit (ROIC) applying sub-threshold technology to provide extremely low power consumption has been proposed. This ROIC includes automatic gain control (AGC) block to widen the dynamic detecting range. It shows that power consumption can be saved up to 96% (from 25.2mW to 0.89mW) and detecting dynamic range can be extended up to more than two orders ranging from 100pA to 60nA. The digital signal from ROIC has low quantization error (less than 1 LSB).

The proposed circuit is implemented under 180 nm CMOS technology process. Simulation results show that the circuit operating normally with 0.8V power supply to CVC and 1.0V to ADC.

4.2 Future work

Dual slope ADC, Successive approximation (SAR) ADC consume much less power compared to flash ADC, if replaced flash ADC with dual slope ADC in the future ROIC design, the total power consumption will be reduced further more.

Additional, if keep reducing the power supply to 0.6 volts, the total power dissipation will be reduced even more, however, the automatic gain control (AGC) part is no longer working normally. A new sub-threshold AGC will be needed.

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