

Wright State University

## CORE Scholar

---

Computer Science & Engineering Syllabi

College of Engineering & Computer Science

---

Fall 2009

### CEG 453/653: Embedded Systems

Jack Jean

*Wright State University - Main Campus, jack.jean@wright.edu*

Follow this and additional works at: [https://corescholar.libraries.wright.edu/cecs\\_syllabi](https://corescholar.libraries.wright.edu/cecs_syllabi)



Part of the [Computer Engineering Commons](#), and the [Computer Sciences Commons](#)

---

#### Repository Citation

Jean, J. (2009). CEG 453/653: Embedded Systems. .  
[https://corescholar.libraries.wright.edu/cecs\\_syllabi/928](https://corescholar.libraries.wright.edu/cecs_syllabi/928)

This Syllabus is brought to you for free and open access by the College of Engineering & Computer Science at CORE Scholar. It has been accepted for inclusion in Computer Science & Engineering Syllabi by an authorized administrator of CORE Scholar. For more information, please contact [library-corescholar@wright.edu](mailto:library-corescholar@wright.edu).

## CEG 453/653 EMBEDDED SYSTEMS

Fall 2009, 2:45-3:35 PM, Mon., Wed., Fri., at 146 RC

**Instructor:** Jack Jean

**Office Hours:** 12:30 -1:20 PM & 3:40-4:30 PM, M., W., F.; 334 RC, 775-5106,  
jack.jean@wright.edu

**Textbook: Embedded Systems: Design and Applications with the 68HC12 and HCS12** (1st edition), Steven Barrett and Daniel Pack, Pearson, 2004.

### **Weekly Schedule:**

Week	Contents	Materials to Read
1	Overview, Lab Preparation, C Language	Chap. 1, Chap. 3
2	Timer, Output Compare	Sec. 4.14
3	Simple Parallel I/O	Class Notes
4	Interrupts and Resets	Sec. 4.10
5	MIDTERM; ADC	Sec. 4.22, Sec. 4.23
6	ADC, Input Capture	Sec. 4.14
7	More Timer Functions, SCI and SPI	Sec. 4.15-4.19, 4.24
8	Parallel I/O, Hardware Design Issues	Chap. 5, Sec. 6.3, Sec. 6.6
9	Embedded System Examples, RTOS	Chap. 7, Chap. 8
10	RTOS	Chap. 8

**Grading:** Final letter grade: 90+ (A), 80+ (B), 70+ (C), 60+ (D), otherwise (F).

- Lab. - 30%. **You must attain at least 60% in Laboratory to pass this course.**
- HW - 10%
- Quiz - 10%. Unannounced quizzes (closed book and notes) will be given at the beginning of classes.
- Midterm - 20%; Oct. 9, Friday; open book and notes.
- Final - 30%; November 18, Wednesday, 3:15 PM- 5:15; Not comprehensive, open book and notes.
- Students taking CEG653 will be assigned more analysis works for assignments/tests.

## Schedule of Laboratory Experiments:

Week	Lab No.	Experiment
1		No Lab
2	1	Laboratory Familiarization (10%)
3	2	Speaker Control (20%)
4	2	
5	2	Keypad Scanning (20%)
6	2	
7	3	ADC and DAC Interface (20%)
8	3	
9	4	System Integration (20%)
10	4	

Unannounced quizzes (10%) will be given in the lab to test your preparation and understanding of lab assignments.

Section	Lab Time
1	12:15-2:05 Wednesday
2	2:10-4 Thursday
3	12:15-2:05 Friday
4	12:15-2:05 Monday

Everyone is required to attend weekly 2-hour Labs in Room 339, Russ Center (RC). You will have 24-hour ID-card access to 339 RC to work on your own. Both Theory and practical Laboratory experience are important. You must attain a passing grade in Laboratory to pass this course.

For each lab (except Lab 1), you need to turn in your prelab answers two days (excluding weekends) before your scheduled lab section for grading. You may turn in the prelab answers either in person to the lab instructor or simply slide them under the door of RC339A (the small office at the left hand side right after you enter the lab). For Lab 1, bring your prelab answers to your scheduled lab section for grading.

The lab instructor, his office, office hours, and email address are as follows.

- Mr. Srikanth Nadella
- Office: RC 339A (inside the lab)
- Office Hours: to be arranged
- Email: nadella.2@wright.edu