Computer Science & Engineering Syllabi   College of Engineering & Computer Science

Spring 2008

CEG 360/560-01: Digital System Design

Meilin Liu
Wright State University - Main Campus, meilin.liu@wright.edu

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CEG360/560, EE 451/651 Digital System Design

Winter 2008
Wright State University

Lecturer
Meilin Liu
Office: 353 Russ Engineering Center
Phone: 937-775-5061
Office Hours: Tuesday/Thursday 1:35-3:00 pm
Email: meilin.liu@wright.edu
Web: www.wright.edu/~meilin.liu

Class
- Tuesday/Thursday 12:20 – 1:35 pm Russ Engineer Center 154
- Lab each week, starting from the first week of class

Course Description
Design of digital systems. Topics include flip-flops, registers, counters, programmable logic devices, memory devices, register-level design, and microcomputer system organization. Students must show competency in the design of digital systems. 3 hours lecture, 2 hours lab. Prerequisite: CEG 260.

Text
Required: Vahid, Frank (2007). "Digital Design", First Edition, John Wiley and Sons, ISBN 978-0-470-04437-7.
Reference: Logic and Computer Design Fundamentals, Mano and Kime, any edition, New Jersey: Prentice-Hall.

Prerequisites: CEG 260 or equivalent

1. Fundamentals of Boolean Algebra, including the minimization of logic functions to SOP or POS form.
2. Analysis of logic circuits.
3. The design and testing digital designs using SSI and MSI components.
4. Optimizations techniques to minimize gate count, IC count, or time delay.
5. The design and use of simple memory devices and sequential circuits
6. Decoders, multiplexers, and bus logic.
7. Documentation standards for logic designs.

Objectives: This course has two primary objectives. The first is content-based. We hope to teach students the fundamental principles of design for sequential digital devices. At the end of this course, each passing student should be able to:

1. Describe all the basic types of flip-flops with their characteristics.
2. Describe the characteristics of standard sequential devices, including counters and registers.
3. Describe the characteristics of a variety of programmable devices, including PLDs, RAMs, and ROMs.
4. Discuss basic microcomputer organization.

The second objective is skill-based. Students will exercise their ability to apply these principles in practical application though laboratory projects. At the end of this course, each passing student should be able to:

1. Analyze a given sequential circuit, producing an appropriate state table and state diagrams.
2. Design sequential systems of moderate complexity to satisfy given specifications for function and predict its timing behavior.
3. Produce an appropriate state table and state diagrams for a sequential system.
4. Utilize CAD tools to implement and debug simulations of any combinational or sequential design of moderate complexity.
5. Rigorously apply accepted standards to document sequential logic designs to their work.

Required Work

Lab	40%	(There is a lab schedule available)
Homework	10%	Lots of homework problems!
Quizzes	30%	(1/2 hour examanations, 3 out of 4)
Final Exam	20%	

Grading
The base scale is: A: 90-100, B: 80-89, C: 70-79, D: 60-69, F: 0-59. This is the highest requirement that will be used. The scales may be lowered or revised if necessary.

You must achieve a minimum of 60% in the lab section and all labs must be completed to pass the course. Lab is a crucial element for learning design fundamentals.

Laboratory Projects:

The laboratory projects are designed to help you learn the course concepts and are the primary course "homework". The laboratory projects may be very time consuming if you are not comfortable with the necessary concepts before beginning the project. Each lab consists of one or more "pre-lab" designs which must be turned in before your scheduled "in-lab" section where you will be asked to demonstrate and answer questions about your project.

Students must attend their scheduled lab section every week. This is the only time that a lab instructor is guaranteed to be present to sign-off in-lab demonstrations and to explain concepts necessary for the next pre-lab homework. Some pre-labs require that students have access to the laboratory tools. Student ID cards will permit access to the Lab in 355 RC at any time in which a scheduled lab section of CEG 260 or CEG 360 is not using the room. Students may perform their inlab work at home by installing the software that comes with the most recent version of the textbook.

Points will be deducted for projects submitted late. No points will be awarded for projects that are more than one week late. Corrupt files or other computer problems will not be considered a sufficient excuse to extend this deadline. It is your responsibility to back-up your work. I strongly suggest that you save your work to multiple storage media to aid in the recovery of corrupt files.

Examinations: Four 1/2-hour midterm examinations and one final examination will be administered as announced throughout the quarter. Midterm examinations are "extended homeworks" and are designed to encourage students to cover course material at a steady pace and to provide feedback throughout the quarter. All students may drop their lowest quiz grade

automatically. Thus, make-ups of 1/2-hour examinations are only permitted for documented emergencies on two or more quiz dates.

It is neither possible, nor desirable, to discuss every nuance of the material covered in this course during our limited class time. Students should be aware that although we will discuss the most important materials in class, the textbook contains important facts that may not be discussed in class. Students should not only be able to discuss course concepts in detail, but they should also be able to demonstrate their mastery by applying these concepts on examinations to related problems with which they have no previous experience.

Undergraduate students: The examinations will be closed-book but undergraduate students may use one sheet of 8.5 x 11" notes (double-sided) as reference. Four such sheets may be used on the Final.

Graduate Students: Graduates students are expected to master this material and commit it fully to memory. Graduate students may not use notes during the examination.

Midterm examinations will occur at the normally scheduled class time and location unless announced otherwise in class. The final examination is cumulative and will take place during the university scheduled time period in the normally scheduled class location unless announced otherwise in class.

Homeworks:

The homeworks are designed to help you learn the course concepts and prepare you for the exams.

A penalty of 10% deduction each day for late submission of homework will be given and after one week, 0 point will be given.

Policies and Notes

- Attendance: Attendance is not required, but strongly recommended. If you are not a regular attendee, it will be your responsibility to seek out what material was covered in the lecture and learn it. Most of my exam questions will be taken directly from ideas covered during the lecture, so it greatly helps if you attend!

- I will utilize webCT (wisdom.wright.edu) to post updates to the course, solutions, assignments, announcements, schedule, etc. Get in the habit of checking it regularly.

- Always make back ups of all of you work. Never have just one copy of anything!

- If you are going to miss an exam, for any reason, discuss it with me in advance. If it is an emergency situation, please notify me as soon as possible

- You can reach me a number of ways. Email is normally the best. You can also reach me by phone during the day at 775-5601. If you need human contact either stop in during my office hours, make an appointment by email.

- There are technologies we will use in this class that you may not already know, such as working with tools in lab. We will cover some of these technologies or they will be discussed in lab. If you have trouble, please don't hesitate to come and talk with one of the teaching assistants or me.

- Students are encouraged to get together in small study groups to discuss the course topics and homework problems. Small group discussion and collaboration is a vital aid to mastering the concepts presented in this course. Modern designs are rarely the work of a single engineer! Being able to communicate and work in teams is a necessary skill for any computer engineer. However, **students must work on all graded course assignments and examinations on an individual basis.**

- The key to learning in this class will be spending time working through the problems. Don't wait until 2 hours before something is due to try to learn the concept. This normally ends in a disaster! Stay up with the readings and try to work through some of the problems in the book. There will be lots of problems, so try and work through them when you get them and don't wait until the end. This is not a class where 3 hours of "cramming" right before the midterm/final will translate into a good grade!

- *Conduct for Laboratory Assignments:* Students may discuss "general concepts" of laboratories assignments with each other, but may not, under any circumstances, work with anyone on their actual implementation. If you work with other student on "general concepts" be certain to acknowledge the collaboration and its extent in the assignment. Unacknowledged collaboration will be considered dishonest. Sharing (or copying) schematics or datafiles (including work from previous quarters) is strictly disallowed. If the same work is turned in by two or more students I will consider all students involved equally culpable. You are responsible for ensuring that other students do not have access to your work - do not give another student access to your account, do not leave printouts in the recycling bin, pick up your printouts promptly, do not leave your workstation unattended, etc. If you suspect that your work has been compromised notify your instructor immediately.

- *Conduct for Examinations:* The academic code demands that no student should have an unfair advantage over any other student during examinations. Thus, it is strictly forbidden for any student to refer to information from previous offerings of this course unless this information is provided by the instructor to all students fairly. Thus, the use of test banks of previous quizzes or asking questions about examinations or laboratory assignments to prior students is strictly forbidden.

- *Additional Needs:* Students with disabilities or any additional needs are encouraged to set up an appointment at their convenience to discuss any classroom accommodations that may be necessary.

Academic Misconduct
In this class, the only way to truly learn the concepts to is do the work yourself. I encourage working with other people on the course concepts. When you begin to write the assignment, complete and submit your own work.

Work that has obviously been copied or in the more extreme case, when the original author's name has not even been changed, both parties will receive a 0 grade for that assignment. Both parties will also be turned over to the Office of Judicial Affairs.

Schedule

Section I: Digital System Analysis and Review

DATE	TOPIC / ACTIVITY	HOMEWORK ASSIGNMENT
T 4/1	Class overview, review of combinational digital devices, and bistable elements	Review: Vahid, Ch. 1, 2, 6.2, Appendix A; (Review: Mano, Ch. 1-5); Prepare for entrance survey (ungraded quiz); Lab #0
R 4/3	Entrance survey and completion of combinational review	Review: Vahid, Ch. 4.3, 4.4, 4.5, 4.8, 4.9; (Review: Mano, Ch. 1-5); Lab #0
T 4/8	Review of sequential devices, clocked synchronous state machines, characteristic equations, timing	Read: Vahid, Ch. 3.1, 3.2, 3.5; (Read: Mano, Ch. 6.0-6.3); Lab #1a
R 4/10	CSSM analysis, input/excitation equations, state tables, CSSM models, state diagrams, CSSM timing	Read: Vahid, Ch. 3.3; (Read: Mano, Ch. 6.4, Class notes, Timing Tutorial); Study for Half-hour Exam #1; Lab #1a
T 4/22	Half-hour Exam #1	Refer to next section

Section II: Digital System Design and Synthesis

DATE	TOPIC / ACTIVITY	HOMEWORK ASSIGNMENT
T 4/15	Translating a design into a state diagram	Read: Vahid, Ch. 3.3; (Read: Mano, Ch. 6.5); Lab #1b
R 4/17	Designing with state diagrams, implementing a design with D-type or JK-type flip-flops	Read: Vahid, Ch. 3.4, 5.4; (Read: Mano, Ch. 6.6); Lab #1b
T 4/22	State minimization and assignment in CSSM design	Read: Vahid, Ch. 6.3; (Read: Mano, Ch. 6.5); Lab #2a
R 4/24	Muxes as next-state generators, ad-hoc design, finite memory machines, hierarchical design/testing.	Read: Class Notes; Study for Half-hour Exam #2; Lab #2a
T 5/6	Half-hour Exam #2	Refer to next section

Section III: Design with MSI, LSI, and VLSI Devices

DATE	TOPIC / ACTIVITY	HOMEWORK ASSIGNMENT
T 4/29	Registers, counters, and register transfers	Read: Vahid, Ch. 4.1, 4.2; (Read: Mano, Ch. 7.1, 7.6); Lab #2b
R 5/1	Registers, counters, and register transfers	Read: Class notes; (Read: Mano, Ch. 7.1, 7.6); Lab #2b
T 5/6	Design decomposition	Read: Vahid, Ch. 5.6, Ch. 7; (Read: Mano, Ch. 3.6); Lab #3a
R 5/8	LSI/VLSI Devices: PLDS, ROM, and RAM	(Read: Mano, Ch. 9); Study for Half-hour Exam #3; Lab #3a
T 5/20	Half-hour exam #3	Refer to next section

Section IV: Digital System Organization

DATE	TOPIC / ACTIVITY	HOMEWORK ASSIGNMENT
T 5/13	Register files, function units, and datapath control words	Read: Vahid, Ch. 5.1-5.3; (Read: Mano, Ch. 7.2-7.3, 7.5); Lab #3b
R 5/15	Pipelining	Read: Vahid, Ch. 6.5; (Read: Mano, Ch. 10.1-10.6, 12.1); Lab #3b
T 5/20	The control unit: design, hardwired vs. microprogrammed control, programmable control units, the machine cycle	(Read: Mano, Ch. 8.1, 8.4, 8.7); Lab #4a
R 5/22	A simple computer architecture (lab 4)	Read: Vahid, Ch. 8.1-4; (Read: Mano, Ch. 10); Lab #4a
T 5/27	ISA design: CISC vs. RISC, data and control hazards;	(Read: Mano, Ch. 12.1-12.3); Lab #4b
R 5/29	Contemporary microcomputer architecture	Lab #4b
T 6/3	Half-hour Exam #4; Instructor evaluation; Exit survey	Study for final examination; Lab #4c

Final Examination

DATE	TOPIC / ACTIVITY	HOMEWORK ASSIGNMENT
R 6/5	Course Review	Study for final examination; Lab #4c
Tuesday June 10th	Final examination	1:00-3:00 pm; Regularly scheduled class room

Always have readings scheduled for that day complete prior to the class meeting