Spring 2012

CEG 260-01: Digital Computing Hardware/ Switching Circuits

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CEG/EE 260 Digital Computing Hardware/Switching Circuits

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Course Description
We will discuss and cover basic digital, combinational and sequential logic systems. Labs will be used to gain valuable practical experience in implementing elementary circuits and logic designs.

Goals
There are several goals to accomplish in CEG/EE 260
1. Master numbering systems and basic circuit theory
2. Gain practical experience in analyzing and designing logic systems
3. Develop a foundation for further study in this area
4. Enjoy the process!

Lecturer
Meilin Liu
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Class
- Monday/Wednesday 2:45 – 4:00 pm MC RC 153
- Lab each week, starting from the second week of class

Text
Required: Logic and Computer Design Fundamentals, M. Morris Mano and Charles R. Kime, ISBN: 013198926X, Publisher: Prentice-Hall, Fourth Edition, 2007.

Reference: Vahid, Frank (2007). "Digital Design", First Edition, John Wiley and Sons, ISBN 978-0-470-04437-7.

Required Work

Lab	30%	(There is a lab schedule available)
Homework	10%	Lots of homework problems!
Quizzes	10%	Pop Quizzes to keep everyone up with the class readings!
Midterm Exam I	15%	
Midterm Exam II	15%	
Final Exam	20%	

Grading
The base scale is: A: 90-100, B: 80-89, C: 70-79, D: 60-69, F: 0-59. This is the highest requirement that will be used. The scales may be lowered or revised if necessary.

You must achieve a minimum of 60% in the lab section and all labs must be completed to pass the course. Lab is a crucial element for learning design fundamentals.

Policies and Notes

- Attendance: Attendance is not required, but may be documented by the pop up quizzes. If you are not a regular attendee, it will be your responsibility to seek out what material was covered in the lecture and learn it. Most of my exam questions will be taken directly from ideas covered during the lecture, so it greatly helps if you attend!

- I will utilize Pilot (pilot.wright.edu) to post updates to the course, assignments, solutions, announcements, and schedule, etc. Get in the habit of checking it regularly.

- Always make back ups of all of you work. Never have just one copy of anything!

- If you are going to miss an exam, for any reason, discuss it with me in advance. If it is an emergency situation, please notify me as soon as possible

- You can reach me a number of ways. Email is the best way to reach me. You can also reach me by phone during the day at 775-5601. If you need human contact either stop in during my office hours, make an appointment by email.

- There are technologies we will use in this class that you may not already know, such as working with tools in lab. We will cover some of these technologies or they will be discussed in lab. If you have trouble, please don't hesitate to come and talk with one of the teaching assistants or me.

- The key to learning in this class will be spending time working through the problems. Don't wait until 2 hours before something is due to try to learn the concept. This normally ends in a disaster! Stay up with the readings and try to work through some of the problems in the book. There will be lots of problems, so try and work through them when you get them and don't wait until the end. This is not a class where 3 hours of "cramming" right before the midterm/final will translate into a good grade!

Academic Misconduct

In this class, the only way to truly learn the concepts to is do the work yourself. I encourage working with other people on the course concepts. When you begin to write the assignment, complete and submit your own work.

Work that has obviously been copied or in the more extreme case, when the original author's name has not even been changed, both parties will receive a 0 grade for that assignment. Both parties will also be turned over to the Office of Judicial Affairs.

Schedule

(The schedule may subject to change.)

Week	Contents	Read	Labs
1	Intro to digital design, number systems, gates	1.1-1.6, 2.1	
2	Boolean algebra and combinational circuit design	2.2-2.3	Lab 0,1
3	Boolean algebra, Karnaugh maps	2.4	Lab 1
4	Karnaugh maps; **TEST #1**	2.5	Lab 2
5	Karnaugh maps, circuit design and analysis, Technology Parameters	2.6-2.9, 3.1-3.5,6.1	Lab 2
6	Decoders, encoders, and multiplexers, comparators	3.6-3.9	Lab 3
7	Comparators, adders, Latches, Flip-flips; **TEST #2**	4.1-4.4	Lab 3
8	Flip-flips, Registers; Sequential Circuit Analysis	5.1-5.3	Lab 4
9	Sequential Circuit Analysis; Binary arithmetic, adders, subtractors	5.4, 7.1	Lab 4
10	Binary arithmetic, adders, subtractors; Propagation delay; Programmable Logic Array	5.4, 6.2,6.8	
	Final Exam: Wednesday, June 6th, 2012, 3:15 – 5:15 pm in the same classroom.		

Always have readings scheduled for that day complete prior to the class meeting