High-frequency Wide-Range All Digital Phase Locked Loop in 90nm CMOS

Prashanth Muppala
Wright State University

Follow this and additional works at: https://corescholar.libraries.wright.edu/etd_all

Part of the Electrical and Computer Engineering Commons

Repository Citation
Muppala, Prashanth, "High-frequency Wide-Range All Digital Phase Locked Loop in 90nm CMOS" (2011). Browse all Theses and Dissertations. 1056. https://corescholar.libraries.wright.edu/etd_all/1056

This Thesis is brought to you for free and open access by the Theses and Dissertations at CORE Scholar. It has been accepted for inclusion in Browse all Theses and Dissertations by an authorized administrator of CORE Scholar. For more information, please contact library-corescholar@wright.edu.
HIGH-FREQUENCY WIDE-RANGE ALL DIGITAL PHASE LOCKED LOOP IN
90 NM CMOS

A thesis submitted in partial fulfilment
of the requirements for the degree of
Master of Science in Engineering

By

Prashanth Muppala

2011
Wright State University
I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Prashanth Muppala ENTITLED High-frequency wide-range all digital phase locked loop in 90 nm CMOS BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Engineering

Saiyu Ren, Ph.D.
Thesis Director

Kefu Xue, Ph.D.,
Chair, Department of Electrical Engineering

Committee on
Final Examination

Saiyu Ren, Ph.D.

Raymond.E.Siferd, Ph.D.

Chien-In Henry Chen, Ph.D.

Andrew Hsu, Ph.D.
Dean, School of Graduate Studies
ABSTRACT

Muppala, Prashanth M.S.Egr., Department of Electrical Engineering, Wright State University, 2011. High-frequency wide-range all digital phase locked loop in 90 nm CMOS

This thesis presents a high-frequency wide tuning range all digital phase locked loop (ADPLL) in 90 nm CMOS process with 1.2 V power supply. It operates in the frequency range of 2 – 7.2 GHz with wide linearity and high resolution. The ADPLL uses a wide frequency range digital controlled oscillator (DCO) and averaging technique to obtain fast lock time. The operation of the ADPLL includes both a frequency acquisition state and a phase acquisition state. A novel architecture is implemented in a coarse stage to obtain a monotonically increasing wide frequency range DCO for frequency acquisition and a fine control stage is used to achieve resolution of 0.1 MHz for phase tracking and maintenance. Design considerations of the ADPLL circuit components and implementation using Cadence tools are presented. Spectre simulations demonstrate a significant improvement compared to recent architectures with 15 ps of peak-peak jitter and a root mean square value of 4 ps when locked at 5.12 GHz. The power consumption at 5.12 GHz is 5 mW and the locking time is 3.5 μs.
# Table of Contents

1. Introduction ............................................................................................................. 1

   1.1. Phase Locked Loop Fundamentals................................................................. 3

   1.2. Phase Detector................................................................................................. 4

   1.3. Voltage Controlled Oscillator (VCO)............................................................ 7

   1.4. Loop Filter....................................................................................................... 8

   1.5. Frequency Synthesis....................................................................................... 9

2. Architecture Overview .............................................................................................. 12

   2.1. ADPLL Architecture....................................................................................... 12

   2.2. Locking Algorithm........................................................................................ 14

3. Hardware implementation .......................................................................................... 20

   3.1. Digitally Controlled Oscillator...................................................................... 20

   3.2. Phase Frequency Detector............................................................................. 30

   3.3. Control Unit.................................................................................................... 37

   3.4. Frequency Divider......................................................................................... 43

4. Experimental Results ............................................................................................... 49

5. Conclusion ............................................................................................................... 56

6. Future work .............................................................................................................. 57

7. References ............................................................................................................... 58
List of Figures

Figure 1: Block diagram of a basic PLL system .................................................. 3
Figure 2: Phase detector characteristics ............................................................. 5
Figure 3: Multiplier based phase detector ......................................................... 5
Figure 4: VCO characteristics ........................................................................... 7
Figure 5: Block diagram of frequency synthesizer ............................................. 10
Figure 6: Overall architecture of the ADPLL .................................................... 12
Figure 7: Frequency acquisition flowchart ....................................................... 15
Figure 8: Phase acquisition flow chart ............................................................... 16
Figure 9: Frequency tracking example .............................................................. 18
Figure 10: Dynamically changed capacitive loading ........................................ 20
Figure 11: Stage selective ring oscillator ........................................................... 21
Figure 12: Inverter used in this ADPLL .............................................................. 23
Figure 13: Ring oscillator with each stage connected to tri-state buffers ........... 26
Figure 14: Control word Vs DCO frequency ...................................................... 28
Figure 15: DCO with 32 nand gates fine stage ................................................... 29
Figure 16: bi-directional shift register to control the fine stage ......................... 30
Figure 17: Basic Phase frequency detector ....................................................... 31
Figure 18: State transition table of the PFD ....................................................... 33
Figure 19: A and B are in Phase ...................................................................... 33
Figure 20: A is lagging B ................................................................................. 34
Figure 21: A is leading B ................................................................................. 34
Figure 22: Schematic of the PFD used in this work ......................................... 35
Figure 23: Simulations of the PFD .................................................................. 37
Figure 24: 10-bit up-down counter .................................................................39
Figure 25: First 5 registers in the up-down counter ........................................39
Figure 26: Register used in the up-down counter ............................................40
Figure 27: JK flip-flop from D-flipflop .............................................................40
Figure 28: Output of the up-down counter .......................................................41
Figure 29: Schematic of the 32 bit bi-directional shift register .........................42
Figure 30: D Flip-flop connected as a divide by 2 circuit and its output .............44
Figure 31: Divide by 4 circuit .........................................................................44
Figure 32: Divide by 16 circuit .......................................................................45
Figure 33: Output waveforms of the divide by 16 circuit .................................46
Figure 34: Schematic of the frequency divider used in this work .....................47
Figure 35: Schematic of the first stage flip-flop in the frequency divider ..........48
Figure 36: Simulation output of the ADPLL showing feedback signal tracking
    reference signal.........................................................................................50
Figure 37: Eye-diagram of the ADPLL when locked at 5.12GHz .....................52
Figure 38: The reference signal locked to the feedback signal .......................53
List of Tables

Table 1: DCO frequency variation with control code..................................................28
Table 2: DCO frequency coarse and fine resolution.....................................................29
Table 3: Comparing the proposed design with recent architectures from literature....54
ACKNOWLEDGEMENT

First of all, I would like to thank Dr. Saiyu Ren, my thesis advisor for her support and guidance throughout my thesis. Her motivation, expertise and research ideas made me to progress in the right direction. I am grateful to Dr. Raymond Siferd and Dr. Henry Chen, who were kind enough to accept the invitation and serve as the thesis committee members. I am indebted to many of my colleagues in the VLSI lab and friends for the support and guidance provided. Without them this research would not have been possible. I would like to thank the Department of Electrical Engineering, Wright State University for providing me with all the facilities and resources which led to the successful completion of this project

I would like to use this opportunity to thank Mr. Krishna Reddy for his support to me and my family without which my higher studies would have remained as a dream. My deepest gratitude is to my father, mother, sister and brother-in-law for their unfailing support and inspiration to do research. Finally I would like to thank my friends for the support they showed me. Their encouragement and belief in me made this possible.
Dedicated to my family and friends
1. Introduction

The phase-locked loop (PLL) plays a vital role in today’s communication systems. Phase Locked Loop is a class of circuit, primarily used in the field of communication. Also suitable for wide range of applications in Amplitude Modulated Radio Receivers, frequency demodulators, frequency synthesizers, dividers and multipliers. It was first explained in early 20th century, whose applications were in the field of television for the synchronization of the horizontal and vertical scans. Many applications were found as the integrated circuit technology advanced. First Phase locked loop IC was designed using only analog components in mid 20th century. Since then, it has got very wide applications mainly because of its simplicity and reliability.

PLL is generally implemented using analog components, which suffer from high noise due to matching, process variations in the layout and large die area. Research is currently being conducted to make a fully digital phase locked loop to replace current analog phase locked loops for system-on-chip applications. Fully digital PLLs have better noise immunity and better tolerance to bias drifts and PVT variations [1, 2]. They also provide the advantage of implementation using automatic CAD tools which reduces the turnaround time and is also easier to integrate and migrate over various applications and fabrication processes [3].

An analog Phase locked loop is a closed loop system which has a phase-frequency detector (PFD), charge pump, loop filter, voltage/current controlled
oscillator and a divider. Most digital PLLs are the exact digital versions of their analog counterparts, where a digital PFD, digital integrator, digital filter, and a digital divider are used in digital PLLs [4]. Conventional Phase locked loops inherently take a long time to lock since the output frequency undergoes the entire iterative process before reaching natural convergence [5].

In addition, analog phase locked loop uses analog components for the oscillator which produce continuous frequency oscillations. Unlike their analog counterparts, fully digital phase locked loops make use of digital oscillators which cannot give continuous oscillation frequencies. To overcome this, a high resolution digital control oscillator (DCO) is needed.

With the growing importance in high speed wireless applications, a wide range oscillator is required to operate at lower power consumption with smaller feature size. Due to reasons explained above, digital oscillators are preferred over analog ones. The previous work in [6-17] proposes a DCO architecture which operates from 300-600 MHz when implemented in 90nm, 1.4 V CMOS process. A 2.7 – 4.2 GHz all digital phase-locked loops (ADPLL) are discussed in [7, 8]. A new DCO implemented in 0.13µm, 1.2V with operating range from 0.5 - 4 GHz is presented in [9]. Paper [10] discusses about wide range 0.5 – 8 GHz oscillator in 65 nm SOI with 8mW/GHz power dissipation. A fast settling time ADPLL with tuning word estimating and presetting is specified in [11]. Most of the research on ADPLL’s [12-17] so far discusses about narrow range high resolution oscillators in CMOS processes and techniques to reduce the settling time of the ADPLL.

In this thesis, an all-digital phase locked loop with a high-resolution and wide frequency range digitally controlled oscillator (DCO) is presented. It uses a phase-
frequency detector instead of a phase detector, DCO instead of a VCO, control circuit imitating the functionality of a loop filter and a fixed frequency detector. This design is very much suitable for SoC applications and can be automatically implemented with standard cell libraries.

1.1. Phase Locked Loop Fundamentals

A Phase Locked Loop is a closed loop system. The VCO signal of the PLL is fed back to its input and eventually obtains lock to the reference input from an ideal source like a crystal oscillator. PLL has these three main functional units

1. Phase Detector (PD)

2. Loop Filter (LF)

3. Voltage controlled oscillator (VCO)

![Block diagram of a basic PLL system](image)

**Figure 1: Block diagram of a basic PLL system**

Figure 1 shows the block diagram of a PLL system. Phase detector compares the phases of the output and the reference signals. It generates an output voltage as there is a phase difference between the output and the reference signals, which is
related linearly to the phase error between the two signals. This voltage controls the oscillator frequency. As this output is feedback, the entire system tries to achieve a stable state. The system gets stable when phase error is ‘0’. Thus the PLL tries to match the output of the oscillator with the reference signal. The PLL is now in lock condition.

The VCO operates initially at a free running frequency which is in general set to be the middle frequency of the oscillator range. When a reference signal of frequency other than the free-running frequency is given as reference input to the phase detector, the VCO will start changing its frequency and tries to lock to the input reference signal. All this happens only if the reference signal provided is within the lock range of the oscillator. The time taken to acquire lock from once a reference input is given is called as ‘locking time’ of the PLL. With tens of GHz being the operating speeds, it is very important to have the locking time as small as possible. Each and every block of the PLL are discussed in more detail below.

1.2. Phase Detector

As discussed earlier, the phase detector takes two inputs, one from the reference source which provides an ideal input reference and the other from VCO. It generates an error which corresponds to the phase difference between its two inputs. Let $\theta_d$ represents the phase difference between the input phase and the VCO phase. Figure 2 shows the general characteristics of the phase detector. It can be stated that its characteristics are periodic with the period equal to the period of the reference signal. If we speak in terms of the phase difference, we say that these characteristics have
period of $2\pi$. It also clearly shows that the phase error is linearly related to the phase difference between its two inputs.

Figure 2: Phase detector characteristics

The phase detector is a simple multiplier. An analog multiplier is shown below in Figure 3. It may have a gain, which we call it as $K_{pd}$.

Let's consider two sinusoid signals $s_1(t)$ and $s_2(t)$. Both are of same frequency but phase shifted. Now if we multiply these two signals as shown in Figure 3

$$S_3(t) = s_1(t) \ast s_2(t) \quad \text{-----------------}(1)$$
\[ S_1(t) = A_1 \cos [\omega t + \theta_1(t)] \] \[ S_2(t) = A_2 \sin [\omega t + \theta_2(t)] \]

The output of the multiplier is

\[ S_3(t) = K_m A_1 A_2 \cos [\omega t + \theta_1(t)] \sin [\omega t + \theta_2(t)] \]

By using simple trigonometric identities the above equation (4) can written as

\[ S_3(t) = 0.5 K_m A_1 A_2 \sin[\theta_1(t) - \theta_2(t)] + 0.5 K_m A_1 A_2 \sin[2 \omega t + \theta_1(t) + \theta_2(t)] \]

From the above equation 5 we can say that \( S_3(t) \) has a term containing the phase difference of \( S_1(t) \) and \( S_2(t) \). The other term in \( S_3(t) \) contains twice the frequency of the inputs and this can be filtered out which leaves us with only the phase difference between the input signals.

There are couple of ways to implement a multiplying phase detector circuits. Some of the very widely detectors are listed below.

1. XOR gate
2. JK flip-flop
3. Phase-Frequency detector (PFD)
1.3. Voltage Controlled Oscillator (VCO)

The Loop filter charges and discharges the capacitor with the help of a charge pump making the voltage on the capacitor variable corresponding to the phase error. The design of the PLL is quite straightforward as the voltage is directly proportional to the frequency. Characteristics of a voltage-controlled oscillator are shown below in Figure 4.

\[ \omega_o \]

\( \omega_o \)

\( \omega_i \)

\( V_{d0} \)

\( V_d \)

Figure 4: VCO characteristics

The frequency is a linear function of the voltage and hence the curve is a straight line. If \( V_d \) is changed, the output frequency of the VCO varies proportionally
with a constant slope as shown in Figure 4. The VCO characteristics are limited by its operating frequency range and voltage. Outside its operating range, it may show a non-linear relationship between voltage and frequency of oscillation. As per the specifications given, the required range can be chosen.

Several types of VCO’s are used over the last few decades. Broadly, they can be classified as Ring oscillators and LC tank oscillators. Several papers have been written to improve the performance and range of operation.

1.4. Loop Filter

Loop filter decides the stability of the PLL design. The locking time and the tracking phenomenon is dependent on the filter used in the design. The general purpose of the loop filter is to eliminate higher order frequencies and any harmonics. These spurious frequencies cause unwanted signals at the input of the VCO and make the system unstable. A basic RC low pass filter can be used as a loop filter. All the noise has to be terminated before reaching VCO. Hence, higher order filters are quite often used to be more robust.

A loop filter generally consists of a charge pump circuit followed by a RC circuit. The charge pump circuit controls the drive-in and drive-out current to the capacitor from the outputs of the phase detector. The driving current changes the charge on the capacitor and hence changes the voltage too.

The drawback of using higher order loop filters is that, it is hard to design them and it takes a lot of area and they are very sensitive to the dc drifts. Hence several researchers suggested a digital approach to implement loop filter functionality.
Some of them include designing a IIR or FIR filter, or programming a microcontroller to generate the required voltage and control signals.

1.5. Frequency Synthesis

Very often requirement in today’s communication systems is to generate multiple frequencies from a single reference clock source. The device which generated it is called as frequency synthesizer. In all radio applications, we have a single reference clock we need to tune to several frequencies as a requirement and all these applications make use of frequency synthesizer

Also most of the wireless communication systems need to generate high frequency signals with a good accuracy. A frequency synthesizer becomes very handy in such applications. They are also used in signal generators, system analyzers, JBERT’ s in clock data recovery circuits.

Frequency synthesizer is a very popular application in communication systems where PLL is used to simplify its design. By introducing a fixed frequency divider in the feedback loop from output to input, we can generate a highly accurate higher frequency signal. This technique can further be extended to construct a frequency synthesizer. Figure 5 depicts the circuit configuration to achieve frequency synthesis using PLL’s.
Figure 5: Block diagram of frequency synthesizer

The oscillator frequency is dependent on the voltage generated due to the phase error. As it has negative feedback, it tries to make the resultant phase error to be zero. For this, the VCO either increases or decreases accordingly the frequency of oscillation. After some considerable amount of tracking, eventually the frequency divided signal locks to the reference signal. Thus the VCO frequency is $N \times f_{\text{ref}}$ when locked. This relation can be expressed as in equation (6)

$$f_{\text{ref}} = \frac{f_{\text{osc}}}{N} \quad \text{(6)}$$

The output oscillator frequency is equal to

$$f_{\text{osc}} = N \times f_{\text{ref}} \quad \text{(7)}$$

From the above equation, it implies that for a given input reference signal, we can get a $N$-times faster signal using a divide by $N$ circuit. Thus this achieves frequency multiplication. Also, it can be observed that if the reference signal is kept constant and ‘$N$’ in the frequency divider is varied, we can get multiple oscillation
frequencies at the output which are an integer multiple of the reference frequency. This technique of generating multiple frequency signals from a constant reference is known as frequency synthesis and has a variety of applications in real time world.

This thesis is organized as follows. Chapter 2 explains the architecture and the algorithms used to obtain the frequency and phase acquisition. The components of the ADPLL design: DCO, Control Unit, and PFD are discussed individually in Chapter 3. The novel DCO architecture is discussed in more detail. Chapter 4 shows simulation results of the proposed ADPLL followed by conclusion in chapter 5 and references in chapter 6.
2. Architecture Overview

2.1. ADPLL Architecture

This work emphasizes on the design of a wide frequency range digitally controlled oscillator with high resolution. The lock process occurs in two stages, namely frequency acquisition and phase acquisition. Figure 6 below shows the block diagram of the ADPLL architecture used in this work. The DCO frequency is varied by ten binary control signals, En1 to En10 in the frequency acquisition stage, where En10 is the most significant bit (MSB).

![Figure 6: Overall architecture of the ADPLL](image-url)
Various combinations of these ten bits produce different frequencies from 1.9 to 7.8 GHz at the output of the DCO with a resolution of 1-2 MHz per increment in count. The control circuitry generates these ten bits in frequency locking mechanism based on the outputs of the PFD.

When frequency acquisition is completed, the DCO frequency is near to the target or reference frequency signal. At this stage the phase acquisition starts and the control circuitry produces a 32-bit thermometer code to vary the frequency of the DCO in steps of 0.1 MHz covering a range of 1.6 MHz equally above and below the locked frequency in the frequency acquisition state. The frequency of the DCO changes in small steps and locks to the reference signal in phase acquisition mode. The phase acquisition mode continues to maintain the phase of the DCO with reference signal.

The PFD takes the frequency divided oscillator frequency as an input and compares it with the frequency/phase of the reference signal. It generates up and down pulses which generates an event signal, direction signal and an internal clock to monitor the control circuitry. An up signal means the reference signal is leading the feedback signal and hence the control word is changed to speed up the oscillator frequency. Similarly, a down signal corresponds to reference signal lagging the feedback signal and so the frequency of the oscillator is decreased. A direction signal is internally generated from up and down signals. If there are more number of up pulses than down pulses, then the direction signal is high indicating to increase the frequency and vice-versa. The control circuitry changes the control code to accomplish speed up and slow down processes depending on the direction signal. A regular asynchronous counter is used as frequency divider in the feedback path.
2.2. Locking Algorithm

The lock process is divided into 2 modes of operation. One is frequency acquisition mode and the other is phase acquisition mode. The algorithm for frequency acquisition is shown in Figure 7 and Figure 8 gives the algorithm for phase acquisition. Initially, the ADPLL operation starts in the frequency acquisition mode. It starts oscillating at the lowest frequency and then tries to reach the target frequency depending on the 10-bits coarse code generated from control circuitry. The digital control oscillator will generate frequencies corresponding to the 10-bit coarse code. It will overshoot the target frequency and starts to slow down the DCO output and this transient phenomenon continues until it gets stabilized. To reduce this settling time a new approach is used called averaging technique in this design.
Figure 7: Frequency acquisition flowchart
Figure 8: Phase acquisition flow chart
An averaging mechanism is used to speed up the frequency acquisition process. The direction signal determines the change in DCO frequency during the lock process. If the direction is high, the DCO frequency increases and if it’s low, the DCO frequency decreases as shown in Figure 9.

While locked to the target, the DCO signal frequency overshoots the target frequency and then it starts to go down. This point is where speed up to speed down transition happens. Likewise, a speed down to speed up transition happens when the DCO frequency undershoots while trying to lock to the target frequency. When a transition from speed up to speed down or speed down to speed up happens, the control codes are stored in registers.

Maximum control code is obtained when there is a speed up to speed down transition (or an up to down transition in the direction signal as shown in the Figure 9). Likewise, minimum control code is obtained when there is a transition from speed down to speed up (or at a down to up transition in the direction signal shown in Figure 9). If two consecutive maximum control codes and two consecutive minimum control codes differ by a small gap (less than four) then the new control code is loaded as the average of maximum and minimum control codes. This ends the frequency acquisition.

At this stage the target frequency is very close to the DCO frequency but not exactly the same. During the entire process of frequency acquisition only the coarse control code is varied by the control circuitry. A ten bit bi-directional loadable counter is used as the control block in this mode.
When the DCO frequency is close to the target frequency, the frequency acquisition ends and the phase acquisition mode starts. In phase acquisition mode, 32 bit fine control code is varied and DCO frequency changes in very small steps until the phase of feedback signal matches the reference signal. The phase acquisition continues to maintain the phase of the feedback signal with reference signal.

To get a good jitter and fast locking time, an average mechanism proposed in [18] is used. The maximum and minimum fine control codes in phase acquisition mode of the DCO are stored and when these are repetitive for consecutive cycles, we
take the average of those codes, and load the shift register with that value. With this, the ADPLL locks much faster and reduces the locking time.

If the feedback signal leads the reference, then the phase error polarity is considered as positive. So to compensate this, the DCO frequency is decreased until phase error becomes negative. This may lead to under-estimation of the target frequency and hence starting another cycle of catching up. Similarly, the DCO frequency is gradually increased until phase error becomes positive. The target frequency is approximately located near the average of maximum and minimum control codes. This average value is loaded in the 32-bit shift register and phase acquisition process repeats to make sure the phase of the DCO signal is in phase with the REF signal. When a new frequency signal is given as the REF frequency, a reset signal is made high which returns back the control to frequency acquisition from phase acquisition.
3. **Hardware implementation**

3.1. **Digitally Controlled Oscillator**

Like VCO in linear PLL’s, DCO is the oscillator of the ADPLL. It is the block which generates different frequencies for different input control signals. In most digital PLL’s a ring oscillator with little variations is used as the DCO. Common ring oscillator configurations used in digital PLL’s are shown in Figures 10 and 11.

![Diagram of Digitally Controlled Oscillator](image)

**Figure 10: Dynamically changed capacitive loading**
There are four important techniques of digital oscillator design [12, 13] of which two are shown above. One of the techniques is based on changing the delay by turning on or off the fixed capacitances, whereas the other uses the number of stages in the ring using a multiplexer dynamically. Having multiple capacitances of different values will need more area and power. If more number of stages is used we will not get good linearity and higher frequency range of oscillation. Also there is a trade-off between the resolution required and the frequency range in the DCO design that can be achieved. The frequency of ring oscillator can be modified in several different ways. One of them is to change the delay by selecting the number of inverters in the ring oscillator using control signals and multiplexers.
One more way of changing the propagation delay is by using a series of tri-state buffers parallel to the inverters in the ring oscillator. By using tri-state buffers connected to each inverter stage, when the tri-state buffer is on, the effective resistance of that stage decreases and more current passes through it. Hence depending on how many tri-state buffers are on, the more current will flow through that state. More current gives rise to higher frequency of oscillation. The tri-state buffer logic gives good frequency resolution but cannot give the wide frequency range. Hence a novel DCO is designed which uses the tri-state buffers and dynamically changing the drive strength of each stage. The components used in the DCO are a 2-input NAND gate, 2 inverters and 381 (127*3) tri-state buffers.

The vital component of the ADPLL design is the DCO. The DCO architecture uses a three stage ring oscillator to obtain high frequencies and array of tri-state buffers for good resolution. Multiple size transistors are used in the pull-up and pull-down networks of the inverter and nand gate in the DCO to have different driving capability. Two control bits are used to select which transistor in the pull-up and pull-down should be turned on. Figure 12 shows the architecture of an inverter array whose driving capability is determined by control signals En8, En9 and En10.
Different widths give different driving currents and hence different frequency ranges of oscillation. Similarly, the drive strengths of inverters are also varied. This change of drive strengths results in very high frequency range of operation. If bigger width transistors are turned on, then more current passes through each stage, resulting in an increase of operating frequency. Suppose $W_0 > W_1 > W_2 > W_3 > W_4$ in Figure 12, then the highest frequency range when $P_0$ is ‘1’, followed by the next highest frequency range when $P_1$ is ‘1’, and so on. A similar multiple drive strength two-input nand gate is used as the first stage of the ring oscillator. The widths of the transistors ($W_0$, $W_1$, $W_2$, $W_3$ and $W_4$) are to be chosen in such a way that the DCO frequency is monotonically increasing with respect to control word.
In order to have good resolution, an array of tri-state inverters is used as shown in Figure 1. Each stage has 127 tri-state inverters connected as an array. These 127 tri-state inverters are divided into seven stages. The first stage consists of only one tri-state inverter, second stage has two \(2^{2-1}\), third stage has four \(2^{3-1}\), fourth stage has eight \(2^{4-1}\), and the last stage has \(2^{6-1}\) tri-state buffers. The number of tri-state inverters per stage increases by a factor of two. These eight stages are controlled by eight control signals. So, these eight control signals, \(En1\) to \(En7\) plus the other three, \(En8\), \(En9\) and \(En10\) are used to change the widths of the transistors in each stage of the ring oscillator form the 10-bit controllable coarse code.

It is important to note in Figure 13 that the first stage of tri-state inverters for all the three stages of ring oscillator is controlled by \(En1\). Similarly second stage of tri-state inverters for all three stages of ring oscillator is controlled by \(En2\). Likewise the third, fourth to eighth stage are controlled by \(En3\), \(En4\) to \(En7\), respectively. The frequency of the DCO depends on the number of tri-state inverters that are on. The more the number of tri-state inverters that are on, the higher the oscillating frequency.

The output frequency of inverter is dependent on high-to-low and low-to-high propagation delays of each stage. However, these delays change across the process, voltage, temperature variations and other transistor parasitics. The DCO output frequency is given by the following equations.

\[
f_{osc} = \frac{I}{T_{delay}} \tag{8}
\]

\[
T_{delay} = 2*t_{dco} * s \tag{9}
\]

\[
T_{dco} = R_{dco} * C_{dco} \tag{10}
\]

\[
R_{dco} = \frac{R_{ring}}{R_{Eab}} \tag{11}
\]
\[ C_{dco} = C_{\text{ring}} + C_{\text{Enh}} \quad (12) \]

\[ R_{\text{Enh}} = \frac{R}{(2^6 \cdot \text{En}7 + 2^5 \cdot \text{En}6 + \ldots + 2^1 \cdot \text{En}2 + 2^0 \cdot \text{En}1)} + 1) \quad (13) \]

\[ C_{\text{Enh}} = [(2^6 \cdot \text{En}7 + 2^5 \cdot \text{En}6 + \ldots + 2^1 \cdot \text{En}2 + 2^0 \cdot \text{En}1} + 1) \cdot C] \quad (14) \]

Where \( s \) is the number of inverters cascaded, \( t_{\text{delay}} \) is the delay of single stage of the ring oscillator. The \( R_{\text{dco}} \) is the total resistance of the ring oscillator including the resistance due to tri-state buffers. \( C_{\text{dco}} \) is the total capacitance due to ring oscillator capacitance and tri-state buffers. The resistance and capacitance of the three series connected tri-state buffers are \( R \) and \( C \) respectively. Figure 13 shows the connection of tri-state inverters for all the three-stages of the ring oscillator. En1 to En10 forms the course control code of the DCO. These bits are modified during frequency acquisition mode.
Figure 13: Ring oscillator with each stage connected to tri-state buffers

For much finer resolution, fine control logic is introduced at the output of the third stage. The fine control circuit consists of 32 2-input nand gates connected in parallel. One input of all these nand gates is connected to the third stage of the ring oscillator as in Figure 15. The fine-tune stage controls the output capacitance by changing the number of nand gates that are turned on.
As shown in Figure 15, the control signals (S<1> to S<32>) are used to control the inputs of these gates. If the input to the nand gate is ‘1’, it provides more capacitive load at the output. If more number of gates are on (input is ‘1’), then it acts as more capacitive load on the ring oscillator which reduces the frequency by a very small value. Initially, 16 gates are on when the phase acquisition mode starts. Depending on the up/down signals from PFD, the frequency is either increased or decreased by turning off gates or turning on the gates off and on, respectively.

When phase acquisition starts, if the output of PFD is up, then the control circuit generates a fine code which turns only 15 nand gates on and this increases the DCO frequency. If it is down, then the control circuit generates bits such that 17 nand gates are on, thus reducing the frequency. A 32-bit bi-directional loadable shift register is used in this mode as control logic. If the direction signal is high, then the contents of the shift register are left shifted and bit ‘0’ is pushed into S<32>. This makes only 15 nand gates on and hence the capacitive load decreases and the frequency increases. Likewise, if the direction is low, the contents of the shift register are right shifted and bit ‘1’ is pushed into S<1>, turning 17 nand gates on. This reduces the frequency of the DCO as the capacitive loading at the output increases.
Table 1 below shows the DCO frequency ranges corresponding to different combinations of Enable Signals.

Table 1: DCO frequency variation with control code

<table>
<thead>
<tr>
<th>En&lt;10&gt;</th>
<th>En&lt;9&gt;</th>
<th>En&lt;8&gt;</th>
<th>Lowest Freq (GHz)</th>
<th>Highest Freq (GHz)</th>
<th>Resolution(ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1.98</td>
<td>3.849</td>
<td>1.93</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>3.823</td>
<td>5.32</td>
<td>0.61</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>5.314</td>
<td>6.372</td>
<td>0.24</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>6.32</td>
<td>7.159</td>
<td>0.15</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>7.115</td>
<td>7.809</td>
<td>0.1</td>
</tr>
</tbody>
</table>

Hence from the table, the digital controlled oscillator of this design operates from 1.98 GHz – 7.809 GHz. It has 10 binary enable signals. The graph in Figure 14 shows how the frequency changes as the control word changes from 0 to 639.

![DCO frequency Vs Control Word](image)

**Figure 14: Control Word VS DCO frequency**
Table 2: DCO frequency coarse and fine resolution

<table>
<thead>
<tr>
<th>En&lt;10&gt;</th>
<th>En&lt;9&gt;</th>
<th>En&lt;8&gt;</th>
<th>Coarse Resolution (MHz)</th>
<th>Fine Resolution (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>28.4</td>
<td>1.775</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>17.2</td>
<td>1.075</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>9.73</td>
<td>0.608</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>7.68</td>
<td>0.48</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>6.09</td>
<td>0.381</td>
</tr>
</tbody>
</table>

The 32-bit bi-directional shift register used in the phase acquisition mode with default value “1111_1111_1111_1111_0000_0000_0000_0000” is shown in Fig. 17. This default value sets exactly half the number of nand gates on and rest off. A binary ‘1’ is pushed if a shift right operation is performed to increase the number of on transistors. Similarly a binary ‘0’ is pushed from left if a shift left is performed. Shifting right leads to decrease the DCO frequency whereas speeding up can be achieved by shifting left.

To improve the resolution of the DCO, a fine delay control is used. The fine delay cell consists of 32 nand gates connected in parallel at the output of the DCO as shown in Figure 15.
When the input to the nand gate is '1', the output of the DCO sees more capacitive load for the same drive strength. Hence the frequency of oscillation goes down. The sizing of these nand gates is chosen such that the minimum resolution is 1 MHz at the output of the DCO. By default 16 nand gates will be turned ON. If the fine stage is ON, then depending on the clock and the up-down signal, the capacitive load is changed by turning ON/OFF the nand gates. To increase the frequency, the number of nand gates that are ON should decrease and vice-versa. This fine stage is controlled by a 32-bit bi-directional shift register.

### 3.2. Phase Frequency Detector

Different phase detectors have been proposed by researchers over the years. A simple multiplier can be used as a phase detector. Linear PLL’s used to make use of analog multipliers as phase detectors. Many digital multipliers were also proposed using the switching technique. Everyone had its own advantages and disadvantages and most often a trade-off is made among the simplicity, accuracy and performance.
Among the many, there are three phase detectors that are very widely used in synthesis.

- Phase-Frequency detector
- EXOR Phase Detector
- JK flip-flop

The Phase/frequency detector turns out to be the best one among all of the above. It offers an unlimited pull-in range which guarantees digital phase locked loop acquisition even under the worst operating conditions. A conventional schematic diagram of the phase/frequency detector is shown below in Figure 17.

![Figure 17: Basic Phase frequency detector](image)

This circuit uses two D-Flip-flops and an AND gate. In the figure above, the D- inputs of both the flip-flops are connected to ‘1’. Each of them is separately triggered using reference and the feedback clock respectively.
These are asynchronous flip-flops. If the input to the clear pin is ‘1’, then irrespective of the clock the present state, the output is cleared and goes to ‘0’. So, if there a logic ‘1’ on the outputs of UP and DOWN, the and gate will generate an output ‘1’ clearing UP and DOWN.

Depending on the operation describe above, the PFD can be in one of the four states:

- UP = 0, DOWN = 0
- UP = 0, DOWN = 1
- UP = 1, DOWN = 0
- UP = 1, DOWN = 1

Since we are using an AND gate to clear the flip-flop when UP=1 and DN=1, we end up only having 3 states. So, now the refined states are shown below.

- UP = 0, DOWN = 0  {state 2}
- UP = 0, DOWN = 1  {state 0}
- UP = 1, DOWN = 0  {state 1}

Now, we have 3 states and to design this we can use an FSM. We need two flip-flops as the number of states is 3. Figure 18 shows state transition table of the FSM of the phase frequency detector. State 0 corresponds to UP=0 DN=0, State 1 corresponds to UP=1 DN=0 and the other combination is State 2.
Figures 19, 20, 21 shows the possibility of the states and their corresponding outputs.

Figure 18: State transition table of the PFD

Figure 19: A and B are in Phase
Figure 20: A is lagging B

Figure 21: A is leading B label down
The phase/frequency detector (PFD) detects the phase and frequency difference between reference signal and the DCO output frequency divided signal. This sends up and down pulses to the control circuitry which forms a direction signal. If the direction signal is high, then the output frequency should be increased and vice-versa. When feedback signal leads the reference signal, a down pulse is generated which tries to reduce the frequency of the DCO. Similarly when REF signal leads the feedback signal, an up signal is generated to increase the frequency of the DCO.

The Figure 22 below shows the phase-frequency detector used in this work. The concept behind its operation is the same as the above discussed. Since, the inputs to the PFD which are reference signal and the feedback signal will be of high frequencies, a high speed flip-flop is used instead of a normal master-slave flip-flop.

![Figure 22: Schematic of the PFD used in this work](image-url)
The exclusive-or of UP and DOWN signals gives the EVENT signal. This EVENT signal is used to clock the bi-directional shift register and the bi-directional up-down counter. This speeds up the lock-up process and helps in achieving less lock time. To control the direction of the count a DIRECTION signal is generated from the UP and DOWN pulses. The bi-directional shift register and bi-directional counter are not clocked when not needed to avoid unnecessary power dissipation.

Figure 23(a) below shows the PFD output when the reference signal is slower than feedback signal and as a result a series of down pulses can be seen. The direction signal will also be low indicating the control circuit to decrease the frequency for every rising edge of the event signal.
Figure 23: Simulations of the PFD

(a) REF signal is faster than DCO signal. (b) REF signal is slower than DCO signal resulting in DOWN pulses

Likewise, Fig 24(b) below shows reference signal faster than feedback signal and up pulses are observed. The direction signal is high indicating to speed up the DCO frequency for every rising edge of the event signal. When both reference signal and the feedback signal have same frequency and phase, event signal will be low and hence the frequency and phase of the DCO will be locked at that point.

3.3. Control Unit

The control unit takes the output of the PFD and generates a control code to change the DCO frequency. The control unit outputs either a 10-bit control code or a 32-bit control code depending on its operating mode. A frequency acquisition
operating mode would produce 10-bit control bit, whereas in phase acquisition, it generates 32 control bits. The main blocks in the control unit are a 10-bit bi-directional loadable up-down counter for the coarse code and a 32-bit bi-directional loadable shift register for the fine tune code. The 10-bit coarse code initially starts from the minimum value (all 0’s), which corresponds to lowest frequency, and then continues to increase to reach the target frequency. Once the frequency acquisition completes, the DCO frequency will be very close to the target frequency.

The control unit saves the 10-bit coarse control word which corresponds to this frequency and starts phase acquisition. The 32-bit fine control code is initially set such that half of the nand gates are on and the rest are off. This fine code is now either right or left shifted to decrease or increase the frequency of the DCO signal, respectively, in very fine steps of 0.1MHz in this case. The phase acquisition mode attempts to maintain the DCO signal in synchronous to the reference signal using an averaging algorithm to reduce jitter. Few adders, registers and more logical blocks are used in this control unit to achieve this functionality. But, the main blocks which control the DCO are bi-directional shift register and up-down counter. Figure 24 is a top level schematic circuit for a 10 bit up-down counter, where 10 registers are connected one after another with a common clock. Figure 25 more clearly shows how the first five registers are connected in this up-down counter. The rest five are also connected in the same fashion. Figure 26 shows each register used in the counter and JK flip-flop used in register is formed from D flip-flop as shown in Figure 27.
Figure 24: 10-bit up-down counter

Figure 25: First 5 bits of the up-down counter
Figure 26: Register used in the up-down counter

Figure 27: JK flip-flop from D-flipflop
In this output waveform of Figure 28, the top signal is the decimal representation of 10-bits output of the counter. The middle signal is the direction signal which when ‘1’ represents to increase the count and when ‘0’, decreases the count. The last signal is the clock signal to trigger the registers used in this counter. Figure 29 below is the schematic of the bi-directional shift register used.
Figure 29: Schematic of the 8 bit bi-directional shift register
The fine tune code is controlled by a 32-bit bi-directional loadable shift register (bsr). The Figure 29 above shows an 8-bit bsr which can be cascaded 4 times to form a 32-bit bsr.

3.4. Frequency Divider

The design of a frequency divider is an important factor in the performance of phase locked loops. Any noise from the frequency divider will be added to the PLL as it is in the feedback path and so the locking gets difficult. Basic gates and flip-flops can be used to design frequency dividers. A Simple D Flip-flop can be used to design a divider of two. Figure 30 (a) shows the circuit which implements a divide by two logic using D-flip-flop and Figure 30 (b) its output waveform.
The output of the D flip-flop QB is connected as an input to the flip-flop and it is triggered by a clock input with frequency $f_{\text{clock}}$. Figure 30 (a) shows the circuit as described. From Figure 30 (b), it can be observed that, the frequency of the output of the D-flipflop, Q is half ($f_{\text{clock}}/2$) that of the input clock frequency. Thus this circuit can be used a divide by two circuit. Similarly if we connect two D-flipflops as shown in Figure 31, the output frequency ($f_{\text{clock}}/4$) will be 4 times divided by the input frequency.

**Figure 30:** D Flip-flop connected as a divide by 2 circuit and its output

**Figure 31:** Divide by 4 circuit
Likewise, Figure 32 shows a divide by 16 circuit and it can be expected that the output will have a frequency which is 16 times slower than the input frequency. The waveform in Figure 33 shows the output of the frequency divider used in this work shown in the Figure 34. The input to the circuit is the clock signal shown in the top of the waveform. The output at point A can be seen at the second from the top of the output waveform. It is the FClock divided by 2. At point B, the signal at A is divided by two and it can be seen in the middle signal in the Figure 33. The outputs at C and D are the input signal FClock divided by 8 and divided by 16 signals respectively.
Figure 33: Output waveforms of the divide by 16 circuit (give some description of A, B, C, D)
The input of the frequency divider is the output of the DCO and its output is given to the phase frequency detector for comparison with respect to reference signal. Since the input to the frequency divider is coming from DCO, it can range from 2-8 GHz. Hence the first flip-flop DFF1 has to be fast enough to respond to the high frequency clock. Hence a high-speed dynamic flip-flop is used for the first stage. The first stage flip-flop in the frequency divider is shown in Figure 35.
Figure 35: Schematic of the first stage flip-flop in the frequency divider

This flip-flop is observed to be working at frequencies up to 10 GHz. Though it does not give a 50% duty cycle signal at the output, it is compensated in the stages after that. The output at the divide by 4\textsuperscript{th}, 8\textsuperscript{th} and 16\textsuperscript{th} stages is still a nice 50% duty cycle square wave.
4. **Experimental Results**

The proposed low complexity wide range ADPLL is designed using a 90nm CMOS process with 1.2V power supply and simulated to test its performance. A reference signal in the range 118.7 – 493.75 MHz is given as an input to the ADPLL. As shown in Figure 36, initially, a reference signal of 320 MHz frequency is given as input and it can be observed that the DCO frequency starts at the lowest frequency, 119 MHz, and tries to catch the target frequency of 320 MHz. Approximately after 2.5 µs, the feedback signal has locked to the target frequency and it maintains the same frequency and phase until 6 µs. At 6 µs, the reference signal frequency is changed to 120 MHz and hence the frequency tracking starts again. The feedback signal tries to catch the new reference signal frequency at 120 MHz and it locks after 10.2 µs.

Different input reference frequencies are given to the ADPLL using a multiplexer and Figure 36 shows the DCO frequency locked to both the reference frequencies. The hopping time, which is defined as the time needed for the DCO frequency to become stable and lock to the reference signal after a new frequency has been applied, is 3.75 µs in this case. At this point, the DCO signal oscillates at sixteen times of the reference signal frequency.
In an ideal oscillator, the period of oscillation can be considered as constant. However, in practice, due to some noise variations, the period of oscillation may not be the same for all cycles. The deviation of the oscillation period from its mean period is called jitter. The root mean square (RMS) value of this deviation for infinite number of cycles is called as RMS jitter. While the difference between maximum and minimum value of deviation is called as peak-to-peak jitter [19].

Figure 36: Simulation output of the ADPLL showing feedback signal tracking reference signal
The maximum frequency lock error, defined in equation below.

\[
\text{Percentage Lock Error} = \frac{\text{Target Frequency} - \text{DCO Lock Frequency}}{\text{Target Frequency}} \times 100
\]

The worst resolution is when the DCO is oscillating from 1.98 GHz – 3.849 GHz. Hence, the maximum lock error will be obtained when the PLL is trying to lock to a REF signal corresponding to the above mentioned range.

\[
\text{Percentage Lock Error} = \frac{(123.994e6 - 123.750e6)}{123.994e6} = 0.00196783715 \%
\]

Figure 37 shows the eye-diagram of DCO output clock when locked at 5.12 GHz plotted using Cadence tools. In this eye-diagram, each and every cycle of the DCO output clock are overlapped on one clock period (after the DCO clock is locked to the reference) and the maximum deviation that can be obtained from the graph is measured as peak-to-peak jitter. Number of cycles that are taken into account are 1000. The delay is measured at 50% voltage levels and the period jitter determines how noisy and stable the oscillator output signal is.
The peak-to-peak jitter for this implementation when the feedback signal is locked at 5.12 GHz is 15 ps. The root mean square jitter is a measure of the deviation of the period of each cycle from its mean value. It is measured from Cadence simulation tools and is found to be 4 ps when the DCO signal is oscillating at the same frequency.
Figure 38 shows the output of the frequency divider phase locked to the reference signal. The top signal is the DCO feedback signal and the bottom signal is the REF signal which is oscillating at 320 MHz. It is evident that the DCO feedback signal is locked to the REF signal from the waveform.

Figure 38: The REF signal locked to the feedback signal
Table 3: Comparing the proposed design with recent architectures from literature

<table>
<thead>
<tr>
<th></th>
<th>This Work</th>
<th>[24]</th>
<th>[23]</th>
<th>[22]</th>
<th>[21]</th>
<th>[20]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process (CMOS)</td>
<td>90 nm</td>
<td>65nm</td>
<td>0.18 μm</td>
<td>0.18 μm</td>
<td>65 nm</td>
<td></td>
</tr>
<tr>
<td>DCO type</td>
<td>Ring</td>
<td>Ring</td>
<td>LC</td>
<td>Ring</td>
<td>Ring</td>
<td>Ring</td>
</tr>
<tr>
<td>power-supply (V)</td>
<td>1.2</td>
<td>1.2</td>
<td>1.2</td>
<td>1.8</td>
<td>1.8</td>
<td>1.1</td>
</tr>
<tr>
<td>Multiplication factor</td>
<td>16</td>
<td>27</td>
<td>120</td>
<td>16</td>
<td>60</td>
<td>120</td>
</tr>
<tr>
<td>Tuning range (GHz)</td>
<td>1.9-7.8</td>
<td>0.3-1.4</td>
<td>3-3.5</td>
<td>0.033-1.04</td>
<td>1.1 – 2.2</td>
<td>0.19-4.27</td>
</tr>
<tr>
<td>RMS jitter (ps)</td>
<td>4@ 5.12GHz</td>
<td>3.7@ 1.3GHz</td>
<td>0.4@ 3GHz</td>
<td>13.8@ 950MHz</td>
<td>4@ 1.5GHz</td>
<td>1.4@ 3GHz</td>
</tr>
<tr>
<td>peak-peak jitter (ps)</td>
<td>15 @ 5.12 GHz</td>
<td>32@ 1.3GHz</td>
<td>N/A</td>
<td>86.7@ 950MHz</td>
<td>28.4@ 1.5GHz</td>
<td>15@ 3 GHz</td>
</tr>
<tr>
<td>power dissipation (mW)</td>
<td>5.72 @ 5.12 GHz</td>
<td>16.5@ 1.3GHz</td>
<td>10@ 3GHz</td>
<td>15.7@ 950MHz</td>
<td>15@ 1.5GHz</td>
<td>11.8@ 3 GHz</td>
</tr>
</tbody>
</table>

When compared to other recent work in Table II, the combination of very wide tuning range of 74% centered at 4.85 GHz, very low power dissipation, and low jitter makes this design a competitor for a number of integrated wireless systems on
chip applications. A wider frequency range can be achieved by using bigger transistors in the DCO architecture and a much higher resolution can be obtained by increasing number of tri-state buffer stages.
A PLL has most of its applications in communication systems. Designing these systems to be low powered and low area is the order of the day. Since all the blocks used in a general RF transmitter and receiver are analog blocks which are more susceptible to noise, an all-digital PLL would be a good replacement for the traditional analog PLL. The ADPLL design described in this thesis makes use of only the basic digital gates and so has minimum power and area. The locking time which is an important parameter for the PLL is also comparable to the traditional PLL’s. The design and implementation of the ADPLL discussed in this thesis consumes very low power, 5mW at 5GHz and has a locking time of 2.5 us. The ability to have such a low power and less locking time and wide frequency range with high resolution allows for a convenient way of designing an ADPLL. The jitter of this design is also small and so can be used in high frequency RF communication systems replacing the traditional PLL.
6. Future work

The ADPLL designed in this thesis is aimed at achieving high and wide frequency range. There is more research going on a fractional frequency divider which can be implemented as an extension of this work. The fixed frequency divider used in this work can be replaced by a divide by ‘N’ circuit forming an integer-n or fractional-n frequency divider. The locking range can be extended by using a frequency doublers and dividers. Since this design consists of all-digital blocks, it can be extended by programming the design using a hardware description language and can be automatically synthesized. It is also necessary to verify the design’s noise performance to get more robust and accurate results.
7. References


[16] Zhao, J., and Kim, Y.: 'A Novel All-Digital Phase-Locked Loop With Ultra Fast Frequency and Phase Acquisition'


