2015

DNA-Nucleobase Guanine as Passivation/Gate Dielectric Layer for Flexible GFET-Based Sensor Applications

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DNA-NUCLEOBASE GUANINE AS PASSIVATION/GATE DIELECTRIC LAYER FOR FLEXIBLE GFET-BASED SENSOR APPLICATIONS

A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy

By

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2015

Wright State University

WRIGHT STATE UNIVERSITY

GRADUATE SCHOOL

August 20, 2015

I HEREBY RECOMMEND THAT THE DISSERTATION PREPARED UNDER MY SUPERVISION BY Adrienne D. Williams ENTITLED DNA-Nucleobase Guanine as Passivation/Gate Dielectric Layer for Flexible GFET-Based Sensor Applications BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Doctor of Philosophy.

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ABSTRACT

Williams, Adrienne D., Ph.D. Environmental Sciences Ph.D. Program, Wright State University, 2015, DNA-Nucleobase Guanine as Passivation/Gate Dielectric Layer for Flexible GFET-Based Sensor Applications.

The main goal of this dissertation was two-fold: first, to study and design a graphene-based transistor environmentally friendly by replacing a standard substrate and gate dielectric with different flexible/rigid and biodegradable films and secondly, to study their effects on graphene's charge carrier mobility. A thin film of deoxyribonucleic acid nucleobase purine guanine deposited by physical vapor deposition onto up to ten layers of graphene that were transferred onto various rigid and flexible substrates was characterized more thoroughly. Several test platforms were fabricated with guanine 1) as a standalone gate dielectric, 2) as the control and 3) as a passivation layer between the graphene and PMMA (polymethylmethacrylate). It was found that the bulk charge carrier mobility of graphene was best maintained and most stable with guanine as a passivation layer between the graphene and PMMA. The optimal transistor device suggested in this research consists of 60 nm PMMA (gate dielectric)/10 nm guanine (passivation layer)/four monolayers of graphene (semiconductor)/Willow glass (substrate). Charge carrier concentration, conductivity type, and electrical resistivity were investigated for these devices as well. In addition, the relative humidity under ambient conditions was studied to determine the effect of moisture and oxygen on graphene alone and on graphene with the gate dielectric material on the top of graphene to determine which dielectric material degrades faster. This study strongly suggests potential application of guanine in the electronics industry because of its high temperature stability.

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LIST OF ABBREVIATIONS

Deoxyribonucleic Acid (DNA)

Deoxyribonucleic Acid-Hexadecyltrimethylammonium Chloride (DNA-CTMA)

Cetyltrimethylammonium Chloride (CTMA)

Dimethyl Sulfoxide (DMSO)

Poly(methyl metacrylate) (PMMA)

Physical Vapor Deposition (PVD)

Field Effect Transistor (FET)

Graphene Field Effect Transistor (GFET)

Silicon Carbide (SiC)

Matrix-assisted Pulse Laser Evaporation (MAPLE)

Toluene: Dimethyl Sulfoxide (T:D)

X-ray Photoelectron Spectroscopy (XPS)

Atomic Force Microscopy (AFM)

Near-Edge X-ray Absorption Fine Structure (NEXAFS)

Atomic Layer Deposition (ALD)

Indium-Gallium-Zinc-Oxide (IGZO)

Willow Glass (WG)

Four Monolayers of Graphene (4-MLG)

Monolayers of Graphene (MLG)

Chemical Vapor Deposition (CVD)

Thermogravimetric Analysis (TGA)

Functionalized Graphene (FG)

Chemical/Mechanical Polished (CMP)

Transmission Electron Microscopy (TEM)

Electron Volt (eV)

Metal-Insulator-Semiconductor Field Effect Transistor (MIS-FET)

Source-Drain (SD)

Nanometers (nm)

Electron-beam (E-beam) Evaporation

Titanium-Gold-Indium (Ti-Au-In)

Positive Gate Bias Stress (PBS)

Equivalent Oxide Thickness (EOT)

Poly (ethylene terephthalate) (PET)

Gold (Au)

Threshold Voltage (ΔV_{th})

Highest Occupied Molecular Orbital (HOMO)

Lowest Unoccupied Molecular Orbital (LUMO)

Capacitor-Metal-Oxide-Semiconductor (CMOS)

Gate to Source Bias Voltage (V_{GS})

Electrode Beam Deposition (E-beam)

Organic Field Effect Transistor (OFET)

ACKNOWLEDGMENTS

I would like to thank my dissertation director and academic research advisor, Dr. Gregory Kozlowski for his guidance in relation to this project. In addition, I would like to acknowledge and thank my dissertation committee members, Dr. Steven H. Higgins, Dr. James Grote, Dr. Eva M. Campo, and Dr. Angela Campbell for sharing their expertise. I would also like to give acknowledge and thank Dr. Fahima Ouchen of Air Force Research Laboratory, Wright-Patterson Air Force Base for the technical assistance she provided to me in relation to this research project as well as serving as a mentor in the laboratory. It is with great appreciation that I thank the Wright State University Environmental Sciences Program and Air Force Research Laboratory, Wright-Patterson Air Force Base for funding this critical research. A special acknowledgment goes to both my parents Joseph and Sandra Williams and my brother Joseph Williams Jr. for their continued guidance and support for nearly a decade and beyond. I love you all. My family and friends have continuously reminded me that through my faith and perseverance all things are possible.

I. INTRODUCTION

Electronic circuits are currently based on traditional silicon technology. Organic electronics have huge potential for developing biodegradable products. An ideal pathway for such electronic devices involves fabrication with materials from nature such as silicon. Transistors with an operational voltage as low as 4–5 V, a source drain current of up to 0.5 μA and an on-off ratio of 3–5 orders of magnitude have been fabricated with such materials. This work comprises steps towards environmentally safe devices in low-cost, large volume, disposable electronic application.

Plastic waste is a huge concern in the world. Plastics consumption is expected to increase by a factor of two to three in a few years, particularly due to the growth in developing countries (Rudnik et al. 2008). As an example, household hazardous waste in the UK alone reaches 437,000 tons per year, 47.5% of which is electronic products and plastics (Slack et al. 2004). Each person in the United States produces an average of 4 pounds of household hazardous waste each year for a total of about 530,000 tons/year. The average United States household generates more than 20 pounds of household hazardous waste per year. As much as 100 pounds can accumulate in the home, often remaining there until the residents move out or do an extensive cleanout. How much electronic waste precisely do we generate? Whether trashed or recycled, what are we getting rid of each year in the USA (EPA 2011)? Electronic waste by the ton in 2010 – was it trashed or recycled according to the EPA is summarized in Table 1.1.

Table 1.1. Electronic waste facts and figures.

Products	Total Disposed*	Trashed	Recycled	Recycling Rate
	tons	tons	tons	%
Computers	423,000	255,000	168,000	40%
Monitors	595,000	401,000	401,000	33%
Hard copy devices	290,000	193,000	97,000	33%
Keyboards and Mice	67,800	61,400	6,460	10%
Televisions	1,040	864,000	181,000	17%
Mobile devices	19,500	17,200	2,240	11%
Total (in tons)	2,440,000	1,790,000	649,000	27%

*disposed means going into trash or recycling.

Computer products include CPUs, desktops and portables. Hard copy devices are printers, digital copiers, scanners, multi-functions and faxes. Mobile devices are cell phones, personal digital assistants, smartphones, and pagers. This study did not include a large category of electronic waste: TV peripherals, such as VCRs, DVD players, DVRs, cable/satellite receivers, converter boxes, game consoles. These totals do not include products that are no longer used, but which are still stored in homes and offices. With increased use of plastic electronics in low-cost, large volume, disposable or throwaway applications, plastic waste problems may increase dramatically over the already forecasted enormous increase. Therefore minimizing the negative impact of the increasing production, consumption and disposal of both polymer materials and electronic circuits is a crucial goal in reaching environmental protection and sustainability. Here we describe a first approach for such environmentally friendly electronics, based on natural materials, nature-inspired materials or materials familiar to the public. We limit our work to the demonstration of field effect transistors, which are the building blocks of more complex integrated circuits. Key to the successful demonstration of high-performance, biocompatible and biodegradable organic field effect

transistors operating at low voltages is the evaporation of ultrathin layers of natural organic dielectrics, such as adenine, guanine or glucose on inorganic oxide dielectrics. This is a viable alternative to the passivation of such oxide dielectrics with self-assembled monolayers (Miozzo et al. 2010).

An extensive amount of research has been done on graphene field effect transistor (GFET) using graphene as the channel material. As an example, the top-gate (Fig.1.1) devices can be fabricated with epitaxial graphene layers grown on Si-face 6H-SiC substrates via Si sublimation with SiO_2 serving as the top gate dielectric.

Gate dielectric (SiO_2) is a dielectric between the gate and the graphene layer (see Fig.1.1) with the following most important constraints to guarantee a perfect performance of transistor (Vaziri 2011):

- electrically clean interface between gate dielectric and graphene,
- high capacitance to increase the FET transconductance (ratio of the current variation at the output of the transistor to its voltage variation at the input,
- high thickness to avoid dielectric breakdown and leakage by quantum tunneling.

General characteristic of standard FET transistor is represented in Fig.1.2 and 1.3 if the graphene layer in the schematic plotted in Fig.1.1 is replaced by a semiconductor with a band gap. When voltage v_{DS} increases beyond the critical value to reach the saturation regime (see Fig.1.2), the current through the channel remains constant and then i_D only depends on v_{GS} (Fig.1.3). It appears that an ideal graphene sheet is gapless and its characteristic is different (see Fig.1.4) if it is compared with a band gap transistor (Fig.1.3).

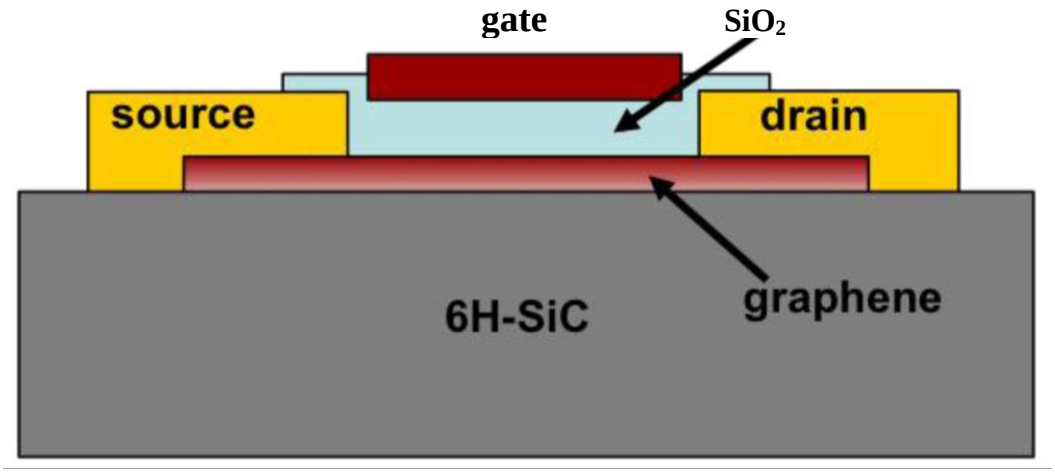


Figure 1.1. Schematic diagram of top-gated graphene FET fabricated with epitaxial graphene layers grown on Si-face 6H-SiC substrate via Si sublimation.

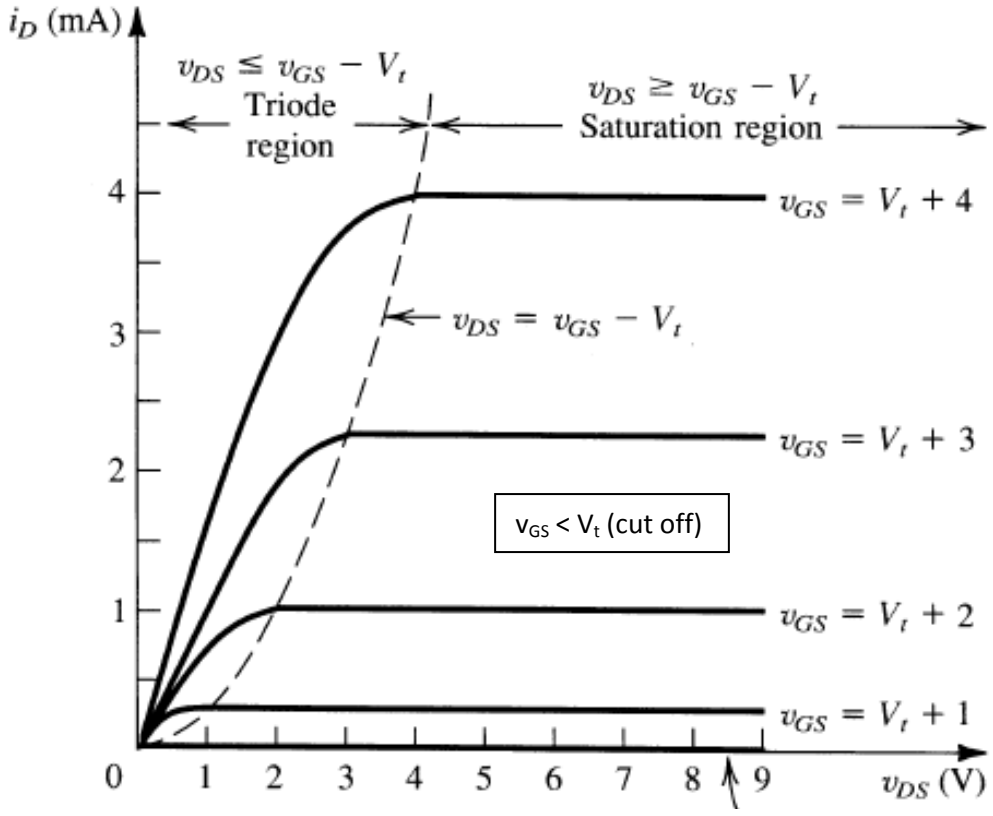


Fig.1.2. General characteristic curves of FET transistor (where v_{GS} is gate-source voltage, v_{DS} is drain-source voltage, i_D is drain current, and V_t is threshold voltage (see Fig.1.3)).

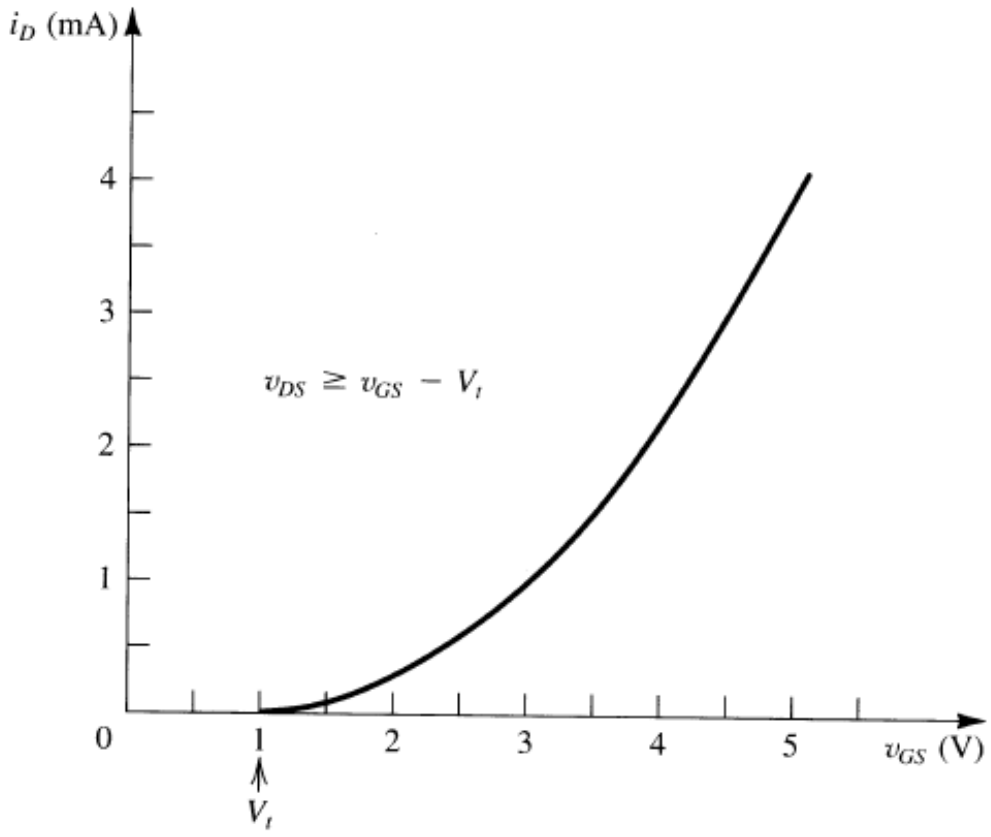


Fig.1.3. Plot of i_D versus v_{GS} in the saturation regime.

Despite the promising electronic properties, graphene field effect transistor cannot be utilized in digital logic since graphene does not have a band gap in its natural state and cannot completely block the current in the transistor's off-sate. However, many efforts have been done to overcome this problem, most notably graphene nanoribbons. In this method, limiting one dimension and making graphene nanoribbons (strips of graphene with ultra-thin width (<50 nm)) can induce a band gap leading to a larger on-off ratio (Fujita et al. 1996). There are many other ways to create a band gap in graphene. For example, a stack of graphene layers (Zhang et al. 2009) (it is utilized in this dissertation) or regular array of holes incorporated into a single graphene layer (Xie et al. 2013) are responsible for the presence of graphene's band gap.

The main goal of this dissertation was two-fold. The first goal is to create GFET such as schematically presented in Fig.1.1 by replacing the gate dielectric SiO_2 with flexible and biodegradable DNA or guanine films, and/or substrate SiC with rigid or flexible substrate such as Willow glass or others. The second goal is to study their effects and, in particular, of guanine on graphene's charge carrier (electrons or holes) mobility μ. The mobility, in general, describes how quickly a charge can move through a material when pulled by an applied electromagnetic field. For example, an average velocity of the electrons called the drift velocity, v_d in response to the electric field E, incorporates the charge carrier mobility, μ defined as (Eq.(1))

$$v_d = \mu E \tag{1}$$

where the mobility is almost always specified in units of $cm^2/(V \cdot s)$.

When graphene is applied in transistors, the mobility of charge carriers degrades

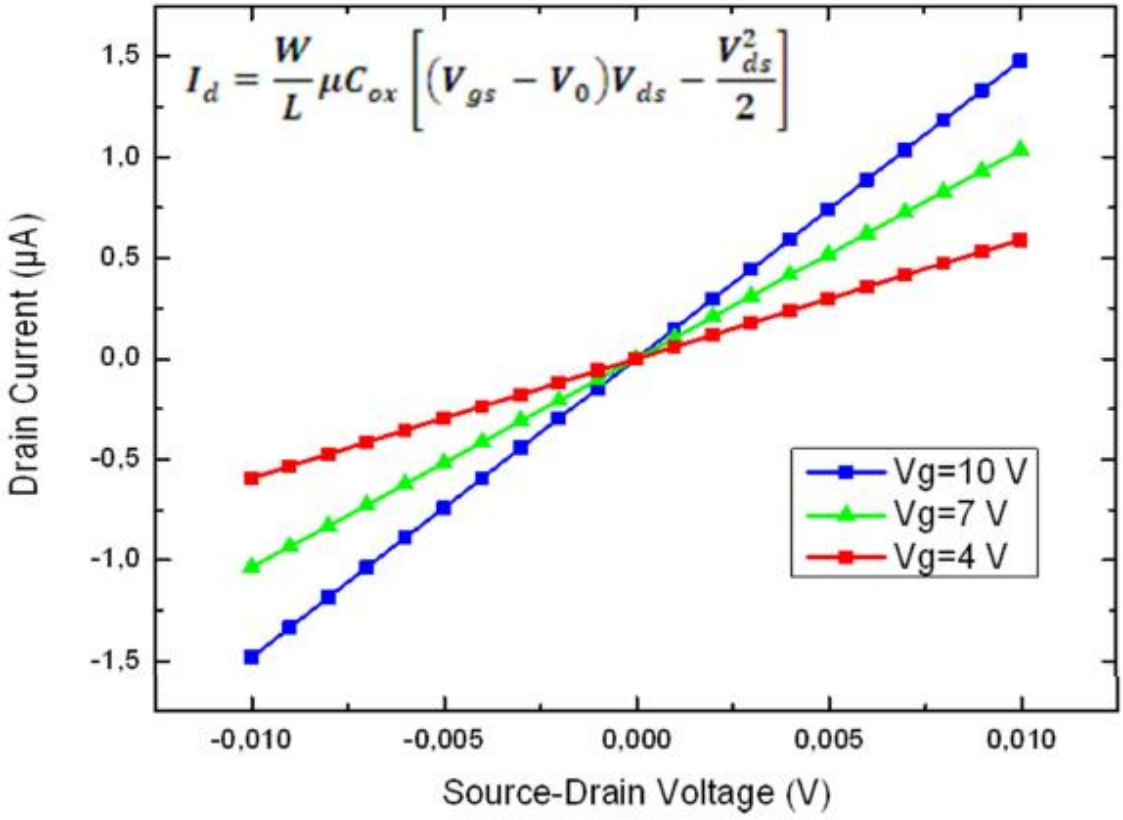


Fig.1.4. Simulated ideal drain current against source-drain voltage for different gate voltage.

significantly due to extrinsic scattering mechanisms. Scattering from charged impurities at the interface of graphene/gate dielectric and near the interface dominates among other mechanisms. These interface and near interface states can be charged and discharged via a graphene channel if their energy levels are below or above the Fermi energy level in graphene, respectively (Vaziri, 2011). Lowering the density and the effect of charged impurities is critical to improve the mobility. Thus, replacing the dielectric material for both substrate and top gate with a high-k (dielectric constant) material can be a solution. High-k materials can reduce the charged impurity scattering because of increased screening effect (Chen et al. 2008), and also improves the gate charge control on the channel due to the higher gate capacitance. Using a high-k material in GFETs is still a trade-off since it introduces more charged impurities than SiO_2. On the other hand, the deposition of high-k material may reduce the mobility of carriers in GFETs due to the defects introduced into graphene sheet. Among different deposition methods for top gate dielectric, physical layer deposition results in more defects and lower quality, while atomic layer deposition (ALD) can provide a high quality dielectric thin film with precise thickness and with less damage into the graphene layer underneath (Liao et al. 2010).

The effects of the guanine included the exploration of several test platforms fabricated with guanine as a standalone gate dielectric—as the control; and guanine can be applied also as a passivation layer between the graphene and PMMA. The two test platforms could have potential applications in biosensors and electronics. In the first test platform guanine was used as a gate insulator in a graphene field effect transistor (GFET) configuration. In the second test platform guanine was used as the “passivation layer” on

top of the graphene layer. Several factors a priori knowledge about various aspects of graphene could be considered. Below is a brief description of each of these items.

Deposition techniques and various substrates comparing bulk charge carrier mobility with device mobility were studied. This work used solvent-less deposition in order to minimize the use of environmentally unfriendly solvents. The substrate-graphene and graphene-gate dielectric interfaces were studied to determine the effects of environmental conditions such as fluctuations in temperature and oxygen levels in the atmosphere. In microfluidics, the integration of graphene as a "lab on a chip" in the fabrication of a biosensor could be utilized for human performance monitoring and/or enhancement (sweat monitor).

Water contamination, which results from metal ions and organic pollutants, has a significant negative impact on the environment. In fact, remediation plans, which seek out to address the environmental contaminations of these pollutants, involve the use of bulk porous graphene architectures. For water-treatment applications, graphene was found useful in three different forms: 1) treatment and remediation, 2) sensing and detection and 3) pollution prevention.

Graphene-based water treatments, however, have been shown to be very costly due to the difficulty of the removal of adsorbent materials after usage. These treatments are also complex due to the risk of secondary pollutants that may enter the environment. To eliminate this occurrence, researchers have assembled individual sheets into 3D macroscopic structures (Berger 2014). These 3D structures would preserve the properties of the graphene sheets and allow easy collection and recycling after water remediation. The application of graphene in water remediation must continue to focus on graphene's

surface properties and microstructure (i.e. size spacing and their orientation). In addition, the ordered and structured design of graphene must be achieved for optimum performance in water remediation.

Particularly, DNA nucleobases are environmentally friendly and have been found to be able to withstand harsh environmental conditions. Environmental conditions such as fluctuations in temperature and oxygen levels in the air can be observed and studied to determine whether or not this affects the substrate-graphene and graphene-gate dielectric interfaces of these devices.

Graphene field effect transistors exhibit several electrical characteristics. According to Freitag (2012), graphene has a zero band gap. The current in a graphene channel does not close completely; and consequently results in the gate limits at the current on/off ratio of ~104. With a high charge carrier mobility, thinness and mechanical, electrical stability of the material, graphene has been proven as an ideal candidate for a field effect transistor (FET) (Freitag, 2012).

The implications of these factors have provided the rationale for this research project in that, the possibility of maintaining the bulk charge carrier mobility of graphene after deposition of the gate dielectric layer for making transistor devices within the laboratory setting is plausible and attainable. However, it has been shown that the FET device mobility is much less than the bulk mobility due to non-optimized gate dielectrics. This is the driving force and main focus of this research.

This dissertation is arranged in the following way. After the general Introduction, Chapter II concentrates on a thorough review of up-to-date literature relevant to the main subject of Thesis, namely, how to build a biodegradable GFET transistor which is

environmentally friendly. This research for now has been restricted to the exploration of flexible and non-flexible gate and substrate dielectric with graphene layers as a semiconductor. Chapter III discusses a DNA film as a possible gate dielectric fabricated by pulsed laser deposition technique (MAPLE). Other possible choices for dielectric materials potentially used in GFET are discussed in Chapter IV followed by fabrication methods used for it (Chapter V). Characterization techniques including the most important Hall Effect are reviewed in Chapter VI and results of the measurements, including structural and chemical characterizations are discussed in Chapter VII, followed by a proposed optimal solution for a GFET transistor based on the study. Overall results of the Thesis are summarized in Chapter IX.

II. LITERATURE REVIEW

2.1 FET and DNA

The following discussion provides the theoretical foundation of this dissertation project as well as potential areas of further study. For example, Irimia-Vladu et al. developed an organic field effect transistor (OFET) with operational voltages of 4-5 V and a source drain current of 0.5 μA from biodegradable and biocompatible materials with use of nucleobases guanine and adenine (Irimia et al. 2010). Metal contacts formed the gate, source and drain electrodes. It was also concluded that such organic dielectrics were needed as the gate insulators and/or semiconductors for the gate-controlled charge transport between the electrodes. The OFETs were fabricated on a degradable substrate that was coated with a layer to reduce surface roughness. An OFET was fabricated where thin layers of nucleobases adenine and guanine were vacuum evaporated on Al_2O_3, perylene diimide as the organic semiconductor, and gold (Au) as the gate, source and drain. The OFET had an operational voltage of 5 - 6 V with a mobility of ~ 0.016 cm^2/Vs for a capacitance per unit area of 81.6 nF cm^{-2} of the gate dielectric. It was suggested that the key to the production of an OFET is to have low operation voltages with the evaporation of ultrathin gate dielectric layers to serve as passivation layers. Irimia-Vladu et al. research group demonstrated that the advantages in the use of DNA nucleobases are the minimization of hysteresis and temperature stability. Lee et al. constructed an OFET with guanine as a hydrogen getter and charge trapping layer in oxide dielectric materials. The guanine's properties of stable molecular stacking, high melting point at 360°C, and high packing density at 2.2 g/cm^3, were shown to prevent decomposition of the layers (Lee et al. 2014). Electrical properties of the guanine thin film with 3.83 eV highest

occupied molecular orbital (HOMO) and 2.48 eV lowest unoccupied molecular orbital (LUMO), and strong electron affinity, are preserved despite deposition of oxides. The schematic of the device structure is presented in Fig. 2.1.

Lee et al. (2014) found that the Indium-Gallium-Zinc-Oxide (IGZO)-FET with guanine appeared to be electrically stable compared to the IGZO-FET with no guanine when both FETs were under a positive gate bias stress (PBS). The IGZO-FET with no guanine in Al_2O_3 dielectric did show a threshold voltage shift in the positive direction due to the PBS. In contrast, the IGZO-FET with guanine did not appear to contain a bias stress induced threshold voltage (ΔV_{th}) and gate hysteresis. The electron charges were injected from the IGZO channel to the guanine layer via application of a positive voltage on the gate through a Fowler-Nordheim tunneling. This process resulted in a positive ΔV_{th}. The Al_2O_3 tunneling layer was bent to induce a triangular shaped barrier wall. In turn, the electrons at the IGZO channel were able to tunnel through the thin barrier and occupy the LUMO state of the guanine layer. Due to the barrier height, the electrons were trapped in the guanine layer. A bias voltage (-30V) could not release the trapped electrons in the guanine layer because the IGZO layer was electrically depleted by a negative pulse voltage and drop in voltage thickness. Lee et al. inserted a dielectric oxide layer during atomic layer deposition (ALD) process in which IGZO layers served as the n-channel FET and guanine as the hydrogen getter (or charge trapping layer). This device was shown to be a stable FET with guanine due to guanine's ability to endure the consecutive ALD process.

Shin et al. demonstrated that ultrathin functionalized graphene (FG) prepared by the functionalization of chemical vapor deposition (CVD) grown graphene using a low-

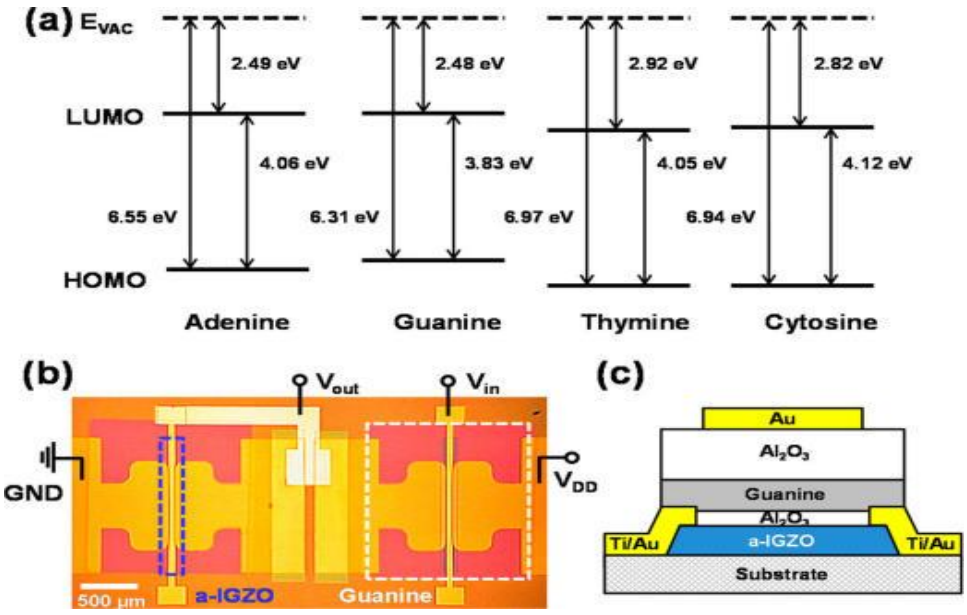


Figure 2.1. Schematic of device structure of organic field effect transistor (Lee et al. 2014).

(a)Schematic energy-level diagrams of DNA-base materials including adenine, guanine, thymine and cytosine thin films with vacuum-level (E_{vac}) alignment. The HOMO-LUMO gaps, electron affinities, and ionization energies were determined by ultraviolet photoemission spectroscopy (UPS) measurement. (b) Optical microscopy image of the top-view of our inverter comprised of two a-IGZO FETs which were connected in series. The a-IGZO channel and embedded guanine layer are indicated by blue and white dashed lines. (c) Schematic cross-section image of the a-IGZO FET with embedded guanine getter/charge trapping layer (Lee et al. 2014).

density plasma treatment could serve as an effective seed layer for the ALD of high-k dielectrics on graphene. They found that the ALD deposition appeared to produce rough dielectric while the oxygen species emanating from the FG seed layer enabled conformal and pinhole-free dielectric film deposition over the entire area of the graphene channel. The capacitors fabricated with the FG-seeded Al_2O_3 layer exhibited high scaling capabilities with low leakage currents compared to the capacitors with Al-seed layers (see Fig. 2.2) (Shin et al. 2013).

The FG-seeded Al_2O_3 had a capacitance density of 300 nF/cm^2, which was higher than the Al-seeded capacitance of 210 nF/cm^2. Both the FG-seeded Al_2O_3 and the Al-seeded had similar breakdown voltages. The FG-seeded Al_2O_3 had a low leakage current density of 7 x 10^{-9} A/cm^2 at 3 MV/cm (Fig.2.3).

FG-seeded Al_2O_3 and Al-Al_2O_3 layers were compared to the conventional seed layers typically used on graphene with respect to the equivalent oxide thickness (EOT). EOT is a method for the evaluation of the quality of various gate dielectrics in capacitor-metal-oxide-semiconductor (CMOS)-based technology. In studies by Shin et al. (2013) and Fallahazad et al. (2012), a Ti-seeded Al_2O_3 capacitance density of ~ 400 nF/cm^2 and a high k ~ 80 but TiO_2 were shown to contain more leaks than Al_2O_3 due to an extremely small band gap. They did not report the leakage current of the Ti-seeded Al_2O_3. Shin et al. reported that a lower leakage current for the same EOT must be achieved in order to have the maximum scalability for various dielectric thicknesses (Shin et al. 2013).

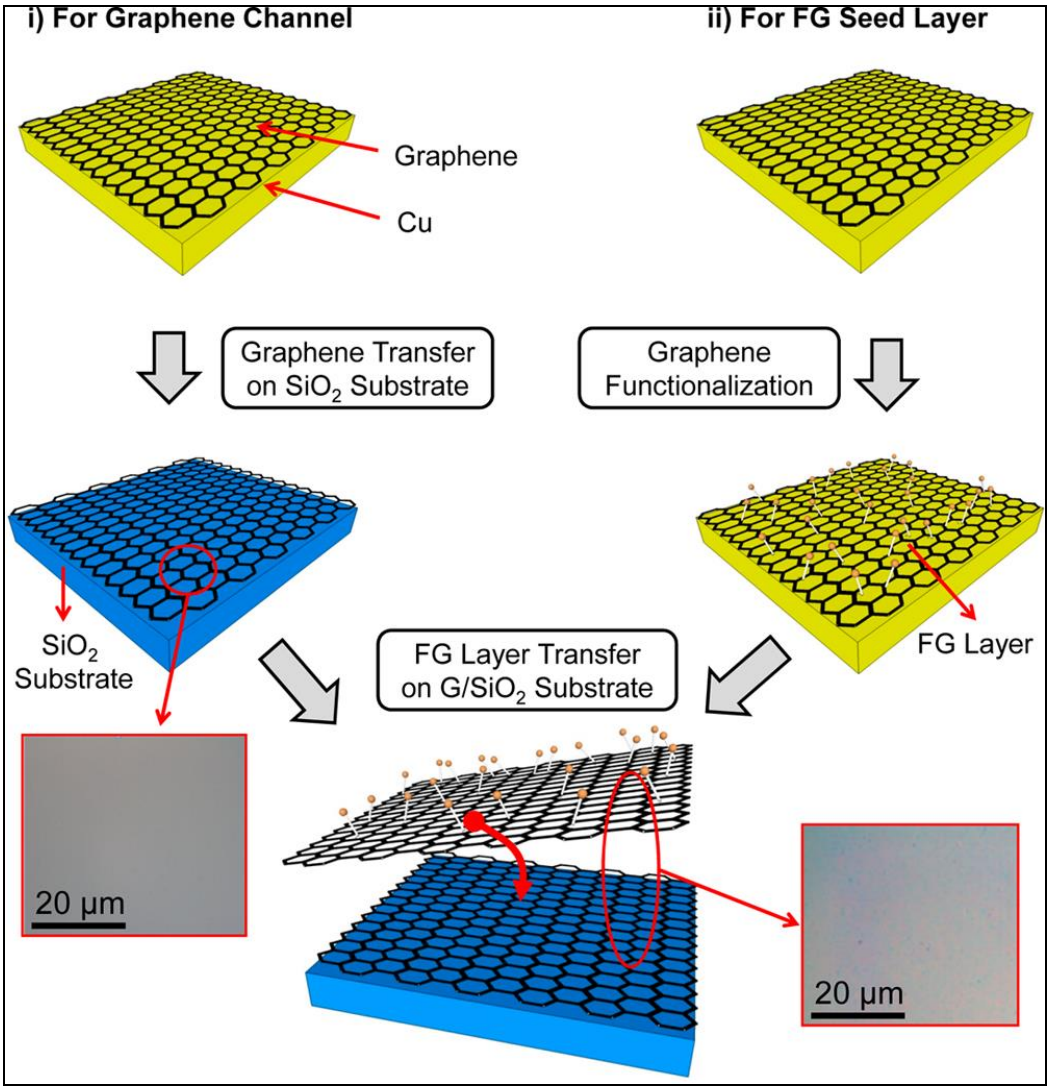


Figure 2.2. Schematic diagram of the fabrication process for the FG seed layer formation on graphene (Shin et al. 2013).

The FG seed layer was prepared using a low-density oxygen plasma treatment on CVD graphene grown on Cu which was subsequently transferred to graphene/SiO_2 substrates using a wet transfer process. The graphene channel was indirectly functionalized with another CVD graphene sheet.

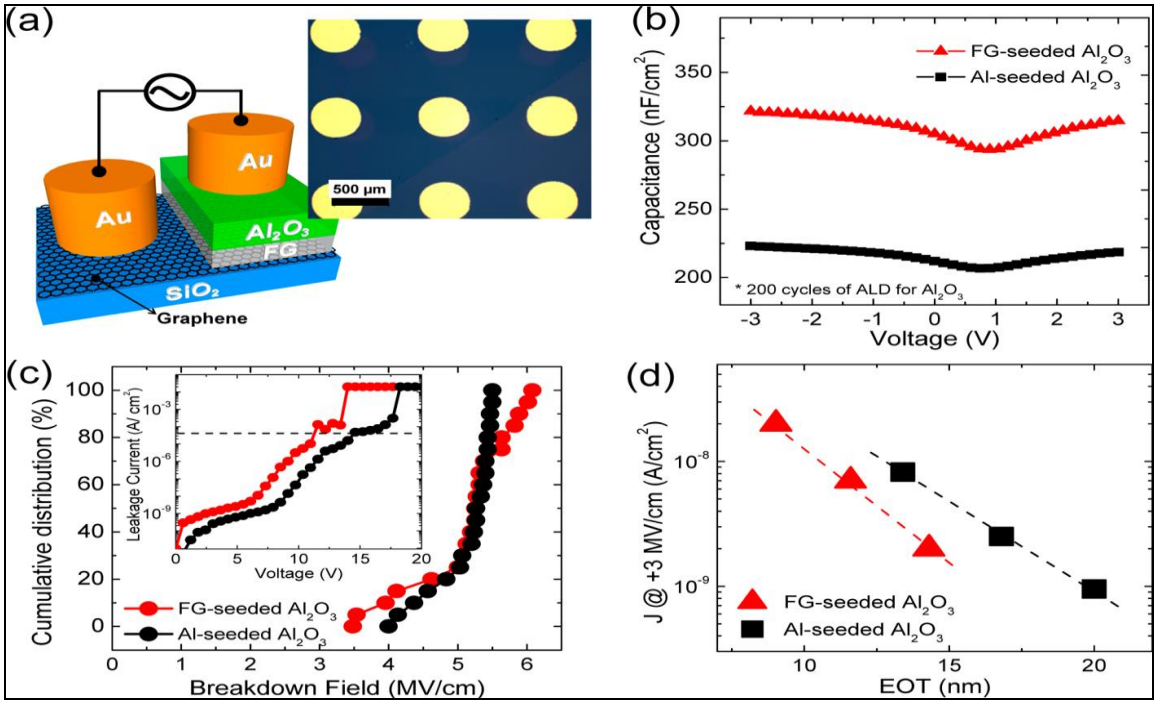


Figure 2.3. Schematic FG-seeded Al_2O_3 and Al-seeded Al_2O_3 dielectric capacitor (Shin et al. 2013).

(a) Schematic cross-sectional view of the MIG capacitors with the FG-seeded Al_2O_3 dielectric. Identical ALD conditions (200 cycles of ALD) were used for the Al_2O_3 deposition. (b) Capacitance−voltage of the different dielectric stacks (Al_2O_3/FG and Al_2O_3/oxidized Al) on graphene. (c) Cumulative failure of the breakdown field for the Au/Al_2O_3/seed layers/graphene MIG capacitors. (d) Benchmarked data on leakage current densities (at +3 MV/cm^2) versus EOT for dielectrics with different seed layers on graphene.

Specifically, in order to achieve high-performance graphene devices, the integration of gate dielectrics into graphene channels has been considered as a significant process because the formation of ultrathin, high quality dielectrics on graphene-dielectric interface, low operating voltage, scaling capability, and device reliability (Shin et al. 2013). Atomic layer deposition may be a useful technique for deposition of ultrathin dielectric films. ALD has been found to control thickness and provide excellent uniformity of the dielectric films. However, the conformal dielectric films deposited on graphene have been found to pose a challenge due to graphene's hydrophobic surface. Therefore, other deposition techniques of various dielectric materials have been adopted (i.e., spin-coat). These techniques have proven to be difficult in the control of dielectric thickness and uniformity.

Tsai et al. (2014) fabricated a flexible transparent graphene-based FET transferred onto poly (ethylene terephthalate) (PET). They used an electro polishing method in order to smooth out the surface of the Cu foil (of the CVD-grown graphene) since it appeared to affect the defect density and electronic property (i.e., mobility) of the graphene on PET. The electro polishing method is an electrochemical process which removes (i.e. polishes and passivates metal specimen) material from a metal specimen and has been confirmed to be an effective deposition technique. Cu foils with and without the use of the electro polishing method designated as up-Cu and p-Cu foils respectively were fabricated (Fig. 2.4) (Tsai et al. 2014).

Tsai et al. (2014) showed that the electro polishing method improved graphene mobility from 90 cm^2/Vs to 340 cm^2/Vs. In addition, the change in mobility when the bending

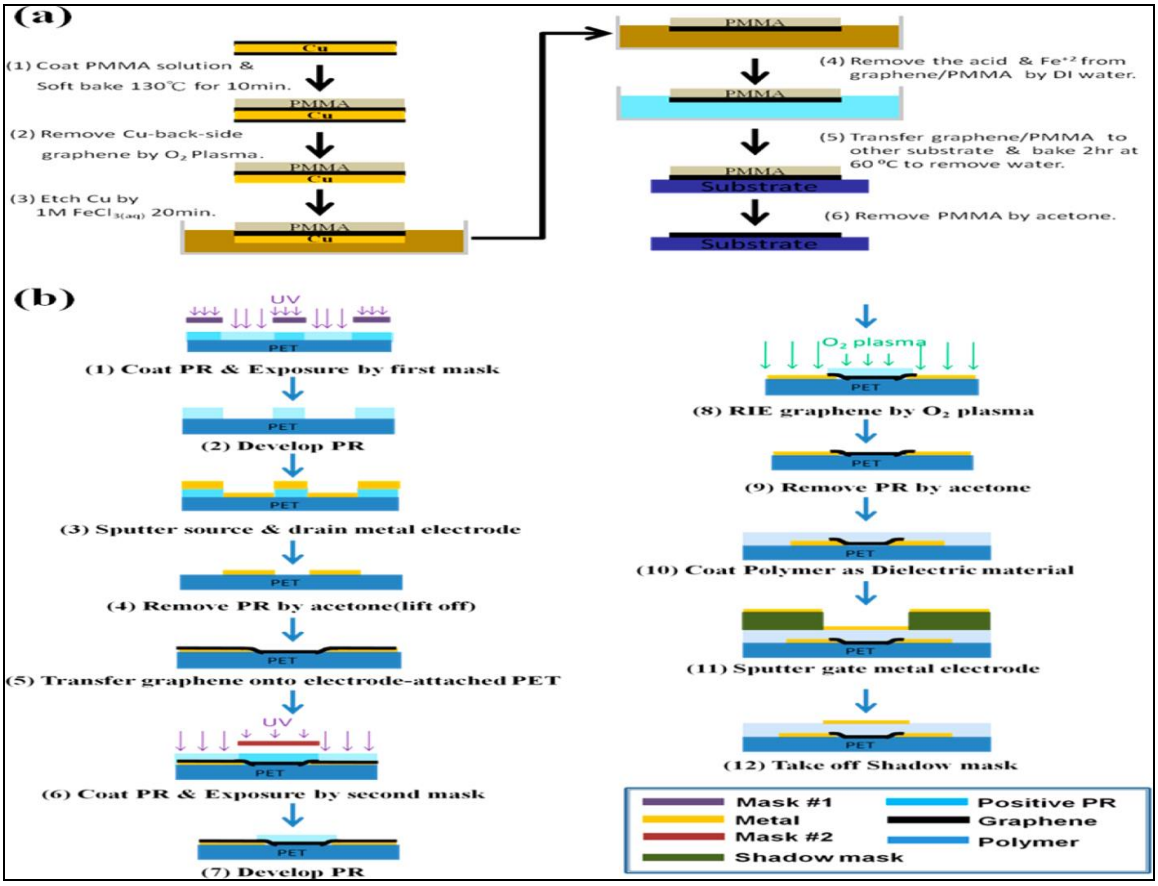


Figure 2.4. Schematic of a fabricated flexible transparent graphene-based FET transferred onto poly(ethylene terephthalate) (PET) (Tsai et al. 2014).
(a) Flowchart of the transferring process. (b) Flowchart of the preparation process for flexible transparent GFETs.

radius of flexible device was decreased from 1.0 cm to 6.0 cm was lower than 10%. It was confirmed that CVD-grown graphene on Cu foil conformed to the Cu surface. Such observations indicated that the presence of defects (i.e., wrinkles) on the uneven Cu foil generated nucleation sites. Three characteristic peaks: D-band, G-band, and 2D-band were detected in the Raman spectrum (see Fig. 2.5 a). The D-band indicates defects in the graphene structure, the G-band represents the E_{2g} vibration mode of sp^2-bonded carbon, and 2D-band refers to a second-order two-phonon process. A low D-band intensity with a ratio greater than 2 between intensities of band-2D to band-G indicates high-quality single-layer graphene. The thickness of the as-synthesized graphene was determined by using AFM to measure the height of the graphene transferred from the p-Cu foil to the SiO_2/Si substrate (Fig.2.5 b). The thickness of the transferred graphene was 0.7 nm - 1.0 nm which is more than typical spacing (0337 nm) in graphite. It was suggested that the thickness of the graphene layer is most likely due to the adsorption of extra water vapor or gas molecules on the surface of the graphene, which increases the thickness of the graphene layers. This transferred graphene thickness of 0.7 nm - 1.0 nm was slightly different when the AFM thickness measurements were conducted in air with suggested values between 0.6 nm and 1.4 nm.

In the electro polishing process, Cu foil was connected to the positive end of a power supply. AFM images of the up-Cu and p-Cu foils are shown in Fig.2.6, respectively. Substantial improvement in the roughness with an R_{max} of 36 nm was achieved after electro polishing treatment. Because of the highly uneven surface of the up-Cu foil, wrinkle-like graphene was clearly observed as shown in Figs. 2.7 a, b. After the electro

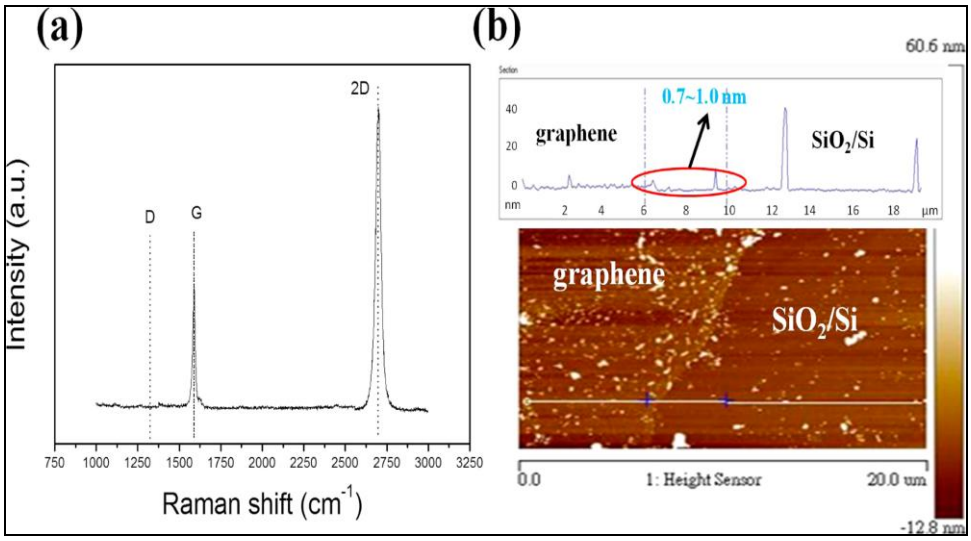


Figure 2.5. Raman spectrum and AFM image of graphene on Si p-Cu foil to the SiO_2/Si substrate (Tsai et al. 2014).

(a)Raman spectrum of graphene on p-Cu foil. (b) AFM images of graphene transferred from the p-Cu foil to the SiO_2/Si substrate.

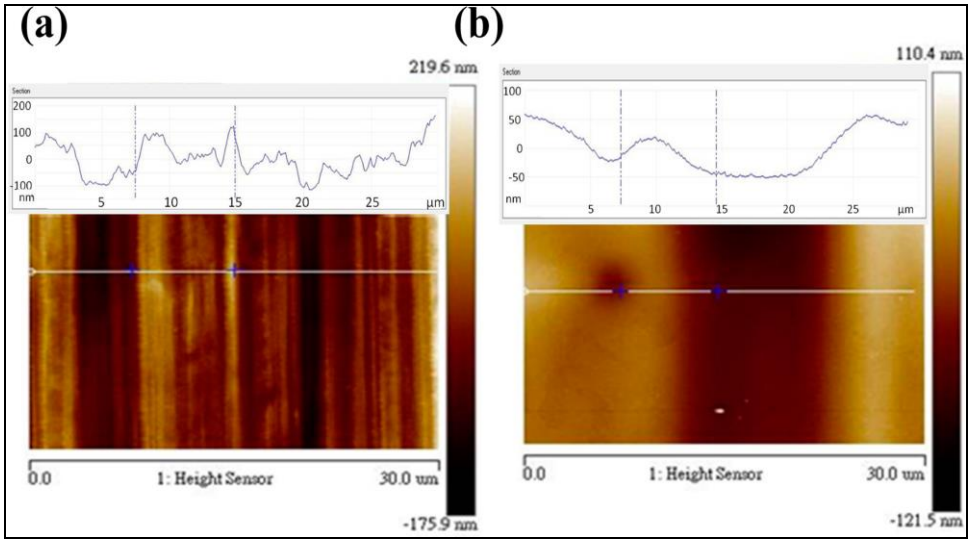


Figure 2.6. AFM images of (a) up-Cu and (b) p-Cu foils (Tsai et al. 2014).
AFM images of wrinkle-free graphene on Cu foils.

polishing, annealing processes were performed on the Cu foil leading to an increase in grain size and a decrease in roughness. This led to the wrinkle-free graphene transferred onto the Cu foils as depicted in the SEM images in Figs. 2.7 c, d.

As a result of study by Tsai et al., flexible transparent GFETs were fabricated by transferring graphene from Cu foil to PET. The characteristic curve of the device was obtained as shown in Fig. 2.8 a. The relationships between the drain current and drain-source voltage swept from − 5 to + 5 V at gate voltage of 0,− 10,− 20, …, − 60 V were measured on the GFET (see Fig. 2.8 b). The carrier mobility of the GFET using graphene synthesized from the p-Cu foil was nearly four times higher than that of graphene prepared from the up-Cu foil (Fig.2.8 c). Variations in the carrier mobility of the GFETs before and after bending were measured as shown in Fig. 2.8 d.

In the research performed by Ouchen et al. (2014), DNA nucleobases adenine, guanine, cytosine, uracil and thymine were considered for their thermal stability in potential use as a gate dielectric in a graphene-based transistor (Ouchen et al. 2014) (see Fig. 2.9).

As can be seen from Fig. 2.9, thermal stabilities (TS) were high for guanine in contrast to cytosine, adenine and DNA-CTMA in nitrogen (N_2). Thermogravimetric analysis (TGA) was also performed on cytosine, adenine and guanine in ambient air and TS were synonymous to TS in N_2. TGA of biomaterials in N_2 (Fig. 2.9) showed that guanine shows promise for incorporation into organic electronics. As a DNA bio-based material, guanine has a high degradation temperature of 460°C. In addition, it has insulator characteristics of DNA-CTMA (i.e., high k, high degradation temperatures, and great insulator with a low dielectric loss), and breakdown voltage ~3.5 MV/cm (Lantz et al. 2009).

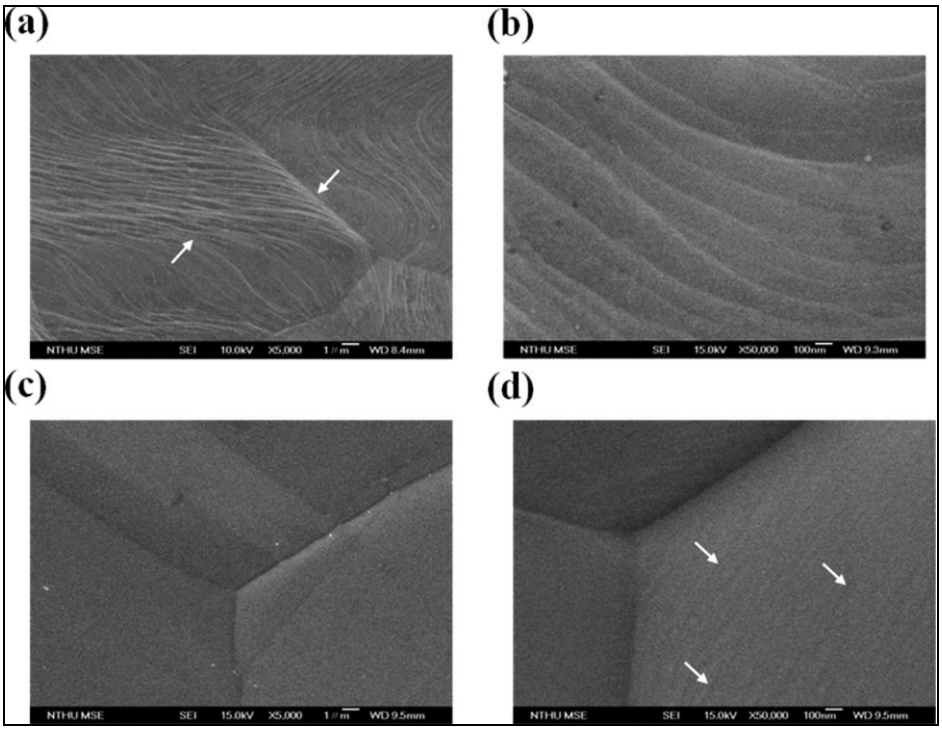


Figure 2.7. SEM images of graphene on the original Cu foil: (a) 5000×; (b) 50000×. SEM images of graphene on the p-Cu foil: (c) 5000×; (d) 50000× (Tsai et al. 2014).

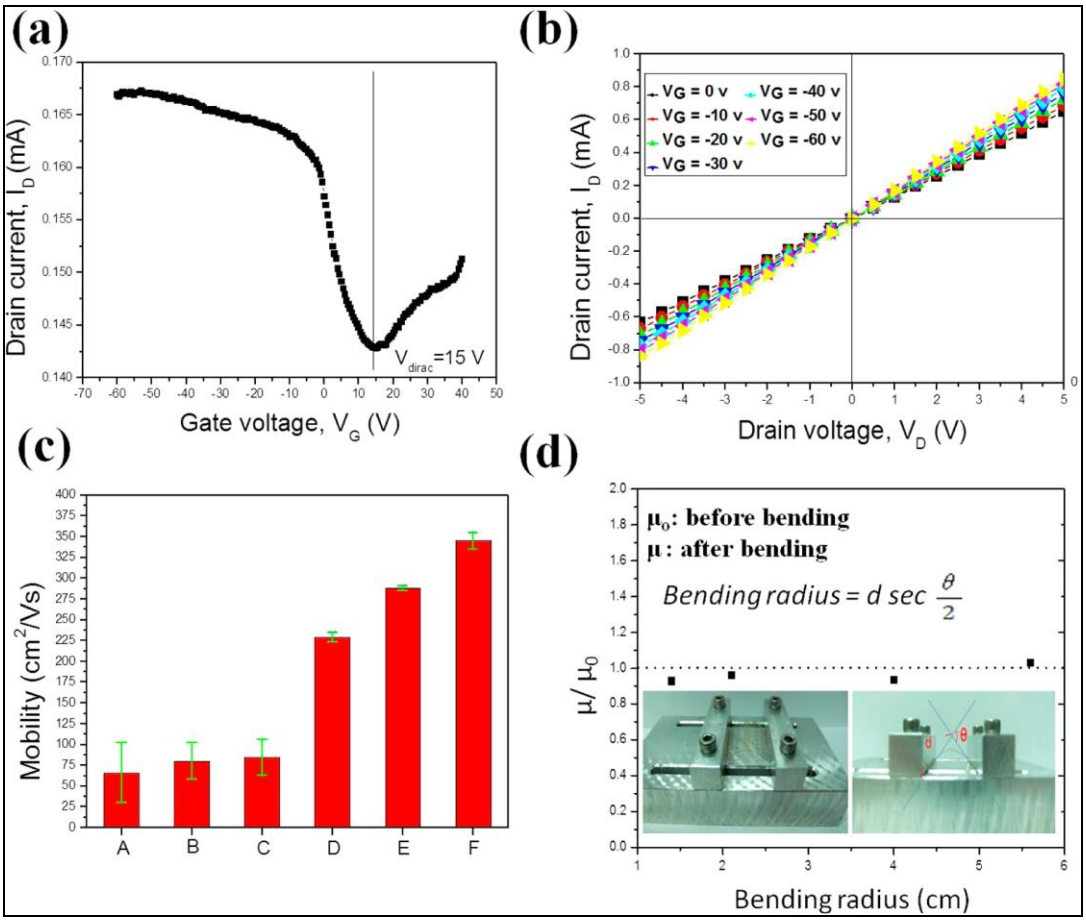


Figure 2.8. I-V curves of graphene on Cu foil and its relationship to the threshold voltages (Tsai et al. 2014).

(a) Curve of the I_G−V_G and I_D−V_G (−60 to +40 V) relationships measured at V_D = 5 V. (b) I_D−V_D (−5 to +5 V) curve (V_G = 0, −10,−20, −30, −40, −50, and −60 V). Channel length: 10 μm. (c) Carrier mobility of six devices fabricated using various types of graphene. A−F represent devices labeled A−F. The number on the left side of the slash implies the channel length (μm), and the word on the right side of the slash indicates the substrates that did (yes) or did not (no) undergo electro polishing: (A) 10/no; (B) 15/no; (C) 20/no; (D) 10/yes; (E) 15/yes; (F) 20/yes (each datum represents the average of three experimental values). (d) μ/μ_0 versus bending radius. The inset on the lower left shows the bending instrument, and that on the lower right depicts the flexible transparent GFET under bending.

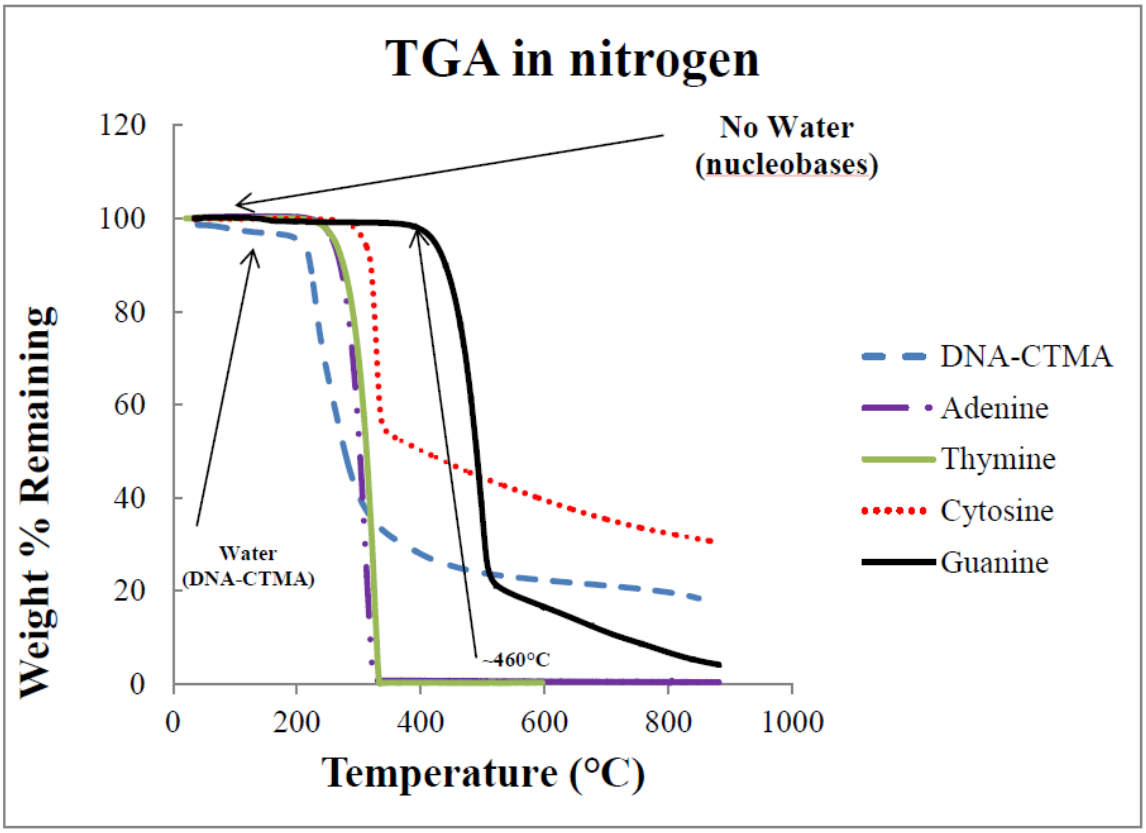


Figure 2.9. Thermogravimetric analysis of biomaterials in N_2 (Ouchen et. al 2014). Guanine had the highest degradation temperature ~ 460°C.

A 60 nm thick layer of guanine was deposited by PVD and explored (Ouchen et al. 2014). The PVD technique is a solvent-free method and minimal impurity issues occurred, unlike in MAPLE and spin-coat/spin-cast techniques. Guanine is able to be deposited due to PVD in a top and bottom gate configuration. Guanine (insulator), graphene (semiconductor), SiC as the rigid substrate with Willow glass (WG) as the flexible substrate can be incorporated into the fabrication of a bio-based GFET. As shown in the TGA plots (Fig. 2.9), the nucleobases have higher degradation temperatures than DNA-CTMA with guanine exhibiting the highest at 460 C. At temperatures below the degradation, the linear decrease of the remaining mass of DNA-CTMA as a function of temperature is an indication for its hydrophilic nature, translated by a major water loss at those temperatures (< 220°C). On the other hand, the insignificant mass loss for the nucleobases at temperatures below their degradation suggests their strong hydrophobicity as no change of initial mass is noted at those temperatures (< 300 C for adenine, < 350 C for cytosine and < 460 C for guanine).The high degradation temperature, the hydrophobic nature and the ease of processing into thin films (solvent-less) are the reasons to why guanine was chosen as the dielectric/passivation material for this research.

2.2 Biopolymers and Deposition Techniques of "Transferred Graphene"

It was observed in previous studies that solution-processed polymer thin film deposition techniques are dependent upon solvent choice, which greatly impacts chain conformation and aggregation in polymers (Hsu 2008). Conformation defects such as twisting and bending of polymer chains influences Van der Waals forces amongst polymer chains and modifies the interchain optoelectronic properties of conjugated polymers.

In the case of intrachain species, the presence of a local conformational defect in a polymer chain disrupts the π-electrons, which reduces both the conjugation length and intrachain mobility. The ability to control the internal morphology of a conjugated polymer thin film is of great interest because it allows control over the extent to which interchain and intrachain species occur (Lantz et al. 2009). The interchain interactions are important for enhancing transport through the film and improve internal quantum efficiency. This process influences optoelectronic properties of organic films in electronic and photonic applications (Hsu 2008).

Solution-based polymer deposition methods, such as "spin-coating" have proven to be a successful route in the fabrication of organic optoelectronic devices. The spin-coating deposition technique requires the solution of a material in a solvent to physically wet the surface of the substrate. Specifically, in spin-coating, interchain recombination is evident due to the high density packing of polymer chains. But, this technique was shown to yield solvent-induced conformational defects that cannot be controlled. This deposition technique results in organic thin film properties that are extremely sensitive to the solvent used and the way in which the solvent evaporates from the substrate. In turn, the morphology of the thin film deposited is uncertain. Thus, an alternative deposition technique needs to be determined to successfully deposit a biomaterial onto graphene without changing graphene's electronic properties (e.g., a decrease in charge carrier mobility) (Hsu 2008). Several biopolymers in various deposition techniques were used to determine the best alternative for graphene-based applications. Specifically, PMMA as a referenced gate dielectric was deposited by spin-coating and it was compared to guanine deposited by PVD. Guanine was shown to have consistent and reproducible results

without altering the bulk charge carrier mobility of the graphene. In contrast to guanine, PMMA decreased the bulk charge carrier mobility of the graphene about 200 cm^2/Vs, specifically in both the Si- and C-face and WG samples. It appeared that the graphene structure was damaged after PMMA deposition due to the changes in structural and electrical properties of the graphene.

2.3 Review of Graphene

In the field of electronics, graphene-based devices have been found to be dependent upon electron transport which is subjected to different types of scattering. Scattering effects are correlated with the quality of the graphene grown. For example, in phonon scattering, all defects of the graphene produced are eliminated. In Coulomb scattering, charged impurities dominate at low temperatures as graphene that come into contact with a substrate acts as an insulator. The carrier mobility, its dependence on temperature, and carrier density determined the type of scattering mechanisms that will occur in the graphene (Steckl 2007). Graphene is considered to exhibit one of the highest charge carrier mobility of all materials. Typical GFETs exhibit ambipolar behavior in which charge carriers change from electrons to holes and vice versa at a minimum conductivity point called Dirac neutrality point (Hsu 2008). Modulating the source-drain current using the gate voltage in a GFET simply shifts the Fermi energy from changing hole conduction to electron conduction and vice versa, with no band gap in between. Graphene transistors thus have very low on/off current ratios - in effect the transistor is unable to turn “off". It was observed that GFETs do not turn off completely unlike other semiconductors with a bandgap, since graphene has a zero-bandgap (Freitag et al. 2012).

Graphene-based electronic devices were operated when carriers are injected into a graphene channel and then collected through metal-indium contacts. These contacts create energy barriers known as Schottky barriers (Yuan et al. 1998). The carriers can overcome the barrier at the metal-graphene interface by the charge-transfer process. The carrier then moved through a barrier at the doped graphene is known as Klein tunneling. This is similar to a p-n junction. This type of carrier passage created a large resistance for holes (Steckl 2007).

Graphene contains some of the best physical properties that make it an excellent candidate for electronic applications: a) extremely high charge carrier mobility, b) saturation velocity, c) insensitivity of electron transport behavior to temperature variation, d) thinness, e) mechanical strength, f) flexibility, g) high current carrying capacity, and f) high thermal conductivity. As a result, graphene can be used as a field effect transistor (FET) for wireless communications and sensing applications (Freitag et al. 2012).

In this dissertation, graphene as the semiconductor layer was examined in two test platforms. A bio-based test platform, similar to a metal-insulator-semiconductor-field effect transistor (MIS-FET) configuration consisted of a semiconductor, source, drain, gate and gate dielectric. It was similar to a conventional FET which relies in part on the control of channel conductivity, drain current, and voltage (V_{GS}).

Use of the bio-based platform was identified based on the evidence reviewed and in reference to high speed applications. FETs have been concluded to successfully respond to variations in voltages but they require a short gate and fast charge carriers within the channel (Lantz et al. 2009 and Hsu 2008). Consequently, FETs are known to

degrade under these conditions (i.e., threshold voltages, barrier, and drain-current saturation) (Hsu 2008). In turn, if an FET is fabricated with a thin barrier then gate control region should counteract short-channel effects to shorten gate lengths. This was found feasible with use of one atomic layer thick graphene used as the channel.

For a high performance GFET, the interface between the gate dielectric and the conduction channel must be minimized to the extent possible to eliminate interface trap density and minimal carrier scattering to maximize, optimize, as well as maintain consistent, reproducible graphene charge carrier mobility (Steckl 2007). Based on previous research, deposited dielectric creating interfacial layer is the driving force behind a transistor. Charge trapping affects carrier mobility and shifts the transistor threshold voltages. The choice of a dielectric material and deposition technique can greatly affect the performance of a GFET (Dong et al. 2011).

2.4 Theory of Transport Properties in Graphene

Graphene is a "massless and gapless Dirac quasi-particle system with a rough linear dispersion." Graphene-based devices have shown to have high mobility at room temperature, low on-off current ratio, and a long mean free path. It has been shown that in air and at room temperature the carrier density, resistivity and conductivity type of graphene can be controlled by applying a gate voltage (Dong et al. 2011).

Due to graphene consisting of optical and acoustic phonon and electron interactions with impurities, the momentum and energy balance equations derived from the Boltzmann's equation consistently determines the drift velocity and temperature of graphene in the linear and non-linear response regimes. Dong et al. (2011) suggested that current-voltage relations appeared to have non-linear behavior. Moreover, they proved

that the source-drain (SD) current and electron temperature in graphene are sensitive to electron density and lattice temperature in a graphene-based device. At room temperature a gated graphene device has a very high carrier density and SD current density.

In particular, the I-V_{SD} relation exhibits non-linearity and non-ohmic behaviors when $V_{SD} > 0.1$ V. In addition, the SD current and electron temperature largely depends on the applied gate voltages with decreasing graphene lattice temperatures. The current density increases with increasing electron density and/or decreasing lattice temperature. When the $V_{SD} > 0.1$V, the heating of electrons in graphene occurs so that the electron temperature is higher than the graphene lattice temperature. Thus, the electron temperature increases as V_{SD} increases. Lastly, it was determined the SD voltage and electron temperature in graphene were $V_{SD} < 3$ V and $T \leq 300$ K, respectively. These findings were based on the scattering mechanism in graphene due to electron-acoustic phonon interaction via deformation potential coupling. It suggests that graphene can be used as an FET in high-speed electronics and nanoelectronics in the fields of nanotechnology and environmental science (Dong et al. 2011).

III. INVESTIGATION OF MAPLE-DEPOSITED DNA FILMS

In our research at AFRL Materials and Manufacturing Directorate, deoxyribonucleic acid-hexadecyltrimethylammonium chloride (DNA-CTMA) was investigated as a gate dielectric in a GFET (Ouchen et al. 2013). DNA-CTMA has a relatively low dielectric constant k = 6 and low leakage current.

Hall transport measurements as a function of temperature of epitaxial graphene grown by SiC decomposition and DNA-CTMA/graphene (Williams et al. 2013) were performed. This study revealed that as temperature decreases graphene's mobility decreases. Several graphs based on a temperature-dependent study before (graphene only) and after (DNA-CTMA spin-cast onto graphene) were plotted (Fig. 3.1). The plot below includes charge carrier mobility, charge carrier concentration, electrical resistivity, and R_1/R_2.

DNA is water-soluble which is incompatible with Matrix-Assisted Pulse Laser Evaporation Deposition (MAPLE). Cetyltrimethylammonium-chloride (CTMA) serves as a cationic surfactant. The CTMA produces a DNA-lipid complex that is insoluble in water but soluble in alcohols. In turn, the DNA-CTMA thin films properties can be tuned by changing the DNA molecular weight and concentration of solvent system used. An organic solvent based solution of DNA is required for MAPLE deposition. To address this issue, 5 mg/mL concentration of DNA-CTMA was dissolved in a mixture of Toluene:DMSO (T:D). Different solvent systems may affect uniformity, coverage, and morphology of the film. The solvent system that was found to achieve optimum thin film uniformity, coverage and morphology at 70:30 T:D. A krypton-fluorine excimer laser (KrF)

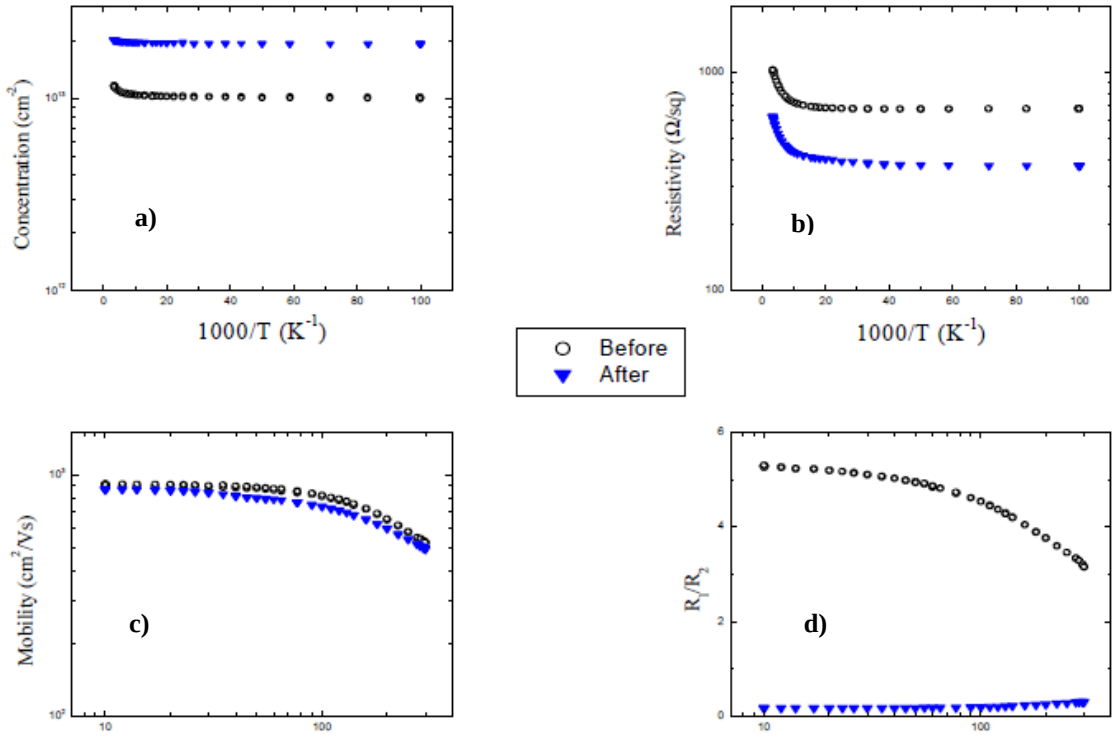
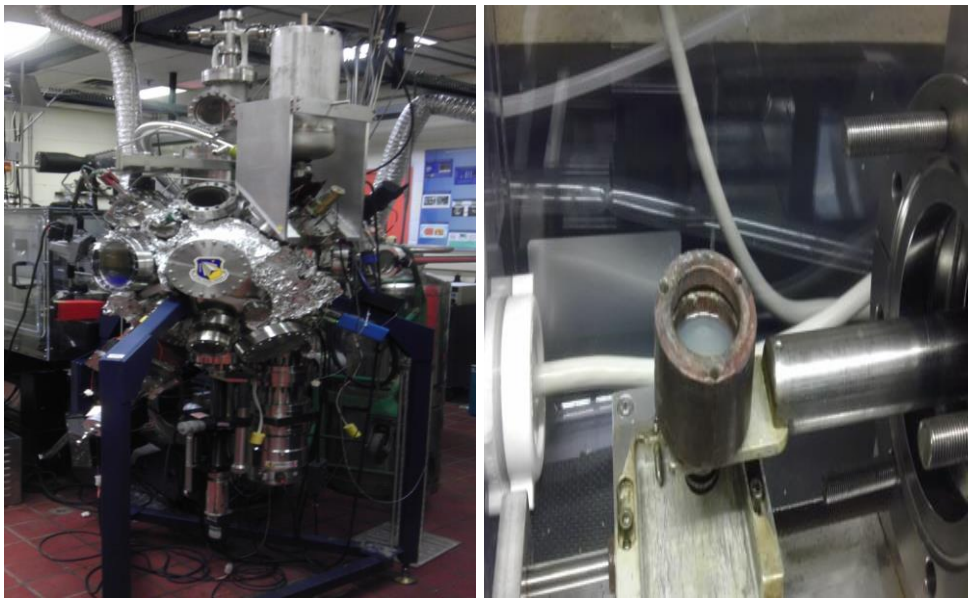


Figure 3.1. Temperature dependent studies of graphene and DNA-CTMA/graphene; a) charge carrier concentration; b) electrical resistivity; c) charge carrier mobility; and d) R_1/R_2 (Williams et al. 2013).

The above graphs are based on a temperature-dependent study before (graphene only) and after DNA-CTMA spin cast onto graphene.

with a wavelength of 248 nm was used to excite the frozen target which led to the evaporation of the solvent system carrying the DNA-CTMA molecules to the substrate (see Fig.3.2). Argon gas was introduced into the chamber to carry the carbonaceous molecules away from the deposition chamber. The organic molecules arrived at the substrate, mostly free of solvent molecules, which significantly reduced the wettability issue. Therefore, homogeneous film coverage of high molecular weight organic materials and enhanced adhesion to the substrates was achieved (Williams et al. 2013).

Initial studies were focused on graphene epitaxially grown on a lattice matched silicon carbide (SiC) substrate, with use of an Oxy-Gon vacuum furnace at 1700°C for 5 minutes at 760 Torr in the presence of argon. DNA-CTMA films were MAPLE deposited onto graphene. Hall measurements gave inconsistent results that showed both p- and n-type graphene samples produced before and after spin deposition of DNA-CTMA onto graphene. Therefore, the graphene conductivity type was independent of the DNA-CTMA films. In addition, the oxygen in the atmosphere created defects, which decreased the bulk mobility of the graphene. Tab.2.1 shows low mobility for both p- and n-types. Charge carrier mobility and conductivity types did not change before and after MAPLE deposition. Mobility of p-type samples were ~ 470 cm^2/Vs and n-type were ~ 347 cm^2/Vs (see Tab.3.1).



a) **b)**

Figure 3.2. a) MAPLE-deposition technique of DNA-CTMA b) in solvent system 70:30 T:D.
A DNA-CTMA solution that was poured into a target cup and cooled to liquid nitrogen temperature for MAPLE-grown DNA-CTMA films (Williams et al. 2013).

Table 3.1. DNA-CTMA spin-coat and MAPLE-deposited onto graphene (Williams et. al. 2013).

	Charge Carrier Mobility (cm^2/Vs)	Charge Carrier Concentration ($10^{13}cm^{-2}$)	Resistivity (Ω/sq)	Type
Graphene	**470±23.5**	**2.02**	**643**	**p**
Graphene/DC(MAPLE)	**400±20.0**	**1.97**	**790**	**p**

a)

	Charge Carrier Mobility (cm^2/Vs)	Charge Carrier Concentration ($10^{13}cm^{-2}$)	Resistivity (Ω/sq)	Type
Graphene	**196±9.8**	**2.48**	**1285**	**n**
Graphene/DC(MAPLE)	**164±8.2**	**2.13**	**1788**	**n**
Graphene/DC(Spin-coat)	**851±42.6**	**1.94**	**379**	**n**

b)

After MAPLE deposition of DNA-CTMA, contact profilometry and X-ray photoelectron spectroscopy (XPS) were performed on the DNA/graphene based samples. DNA-CTMA film thickness measured ~ 111.7 - 243.0 nm with use of contact profilometry. XPS was used to identify the atoms of particular interest-phosphorus, carbon (also present in graphene), nitrogen, and oxygen groups (see Fig.3.3). XPS showed carbon atoms originated from the graphene layers in the samples (Williams et al. 2013).

Phosphorus, nitrogen, and oxygen groups present in the thin films confirmed that the DNA-CTMA fragments were successfully deposited onto the graphene layer. Carbon atoms had the strongest peak intensity due to the graphene layer. A peak at a binding energy of 167.8 eV was identified to be sulfur. Since neither DNA-CTMA nor graphene had sulfur in their molecular structure, the presence of a sulfur atom can be attributed to residual dimethyl sulfoxide (DMSO) that resulted from the MAPLE deposition. Spin

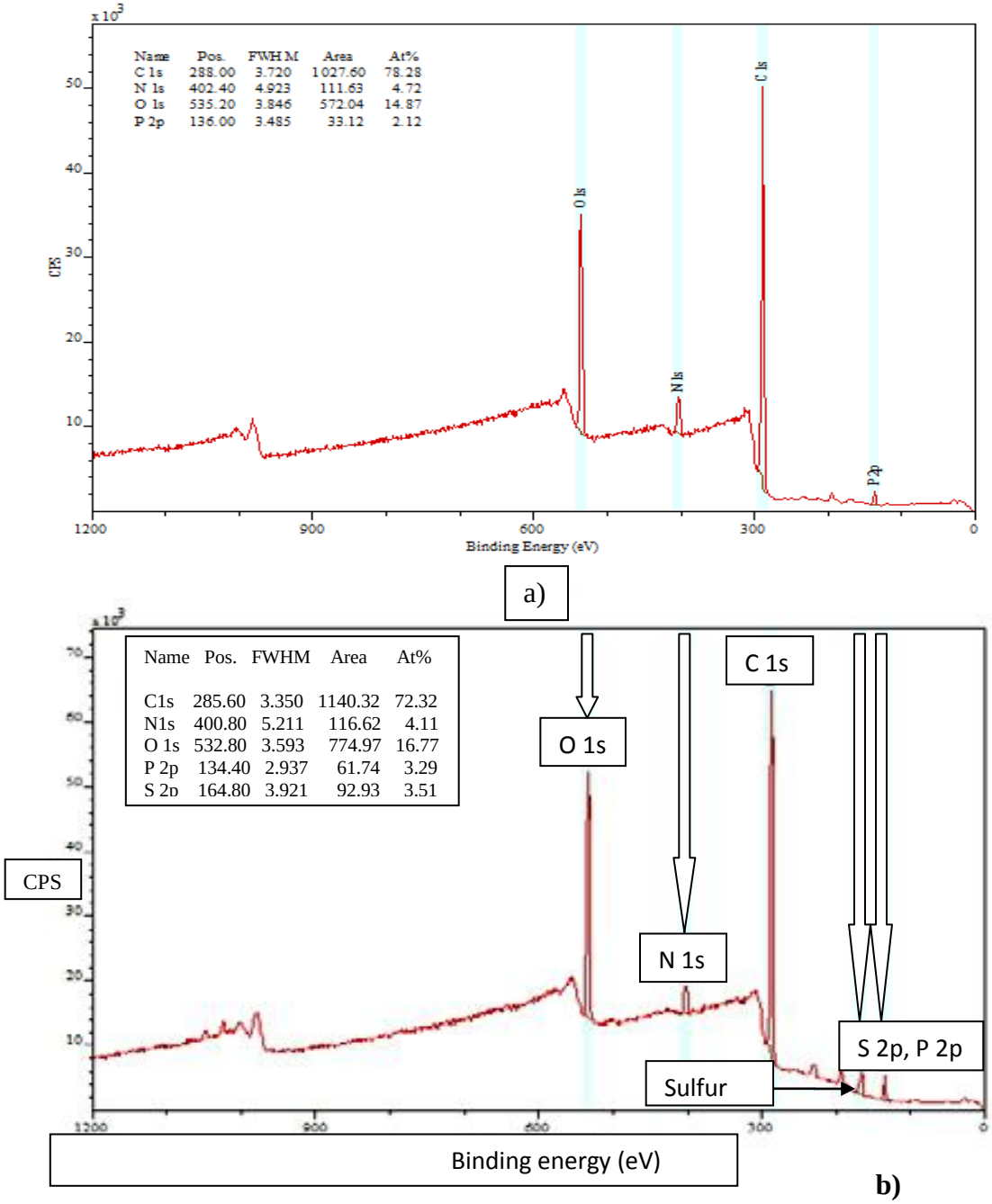


Figure 3.3. a) XPS of MAPLE-deposited of DNA-CTMA thin film without residual DMSO; b) with residual DMSO (Williams et al. 2013).
MAPLE-deposited DNA-CTMA onto epitaxial graphene without residual DMSO due to lack of sulfur being present in the XPS spectrum. Fig. 3.3b depicts the presence of DMSO due to presence of the sulfur peak.

coated DNA-CTMA films showed no evidence of the presence of the sulfur peak in MAPLE deposited DNA-CTMA which was due to lack of DMSO. Raman spectroscopy of graphene revealed a G band at 1582 cm^{-1} and a 2D band at 2755 cm^{-1} (G-band represents the E_{2g} vibration mode of sp^2-bonded carbon, and 2D-band refers to a second-order two-phonon process) as shown in Fig. 3.4. Raman spectra were taken at a laser wavelength of 532 nm. Atomic Force Microscopy (AFM) showed graphene was grown at high quality due to the appearance of terraces (see Fig.3.5).

Problems of contamination arose with DNA-CTMA solvent system of 70:30 T:D which created non-uniform films and inconsistent bulk charge carrier mobility of the epitaxially grown graphene. The MAPLE technique was found not to be a viable alternative in the production of a thin film as a gate dielectric in a GFET. Thus, exploration into other biomaterials was investigated for use in a GFET.

DNA nucleobases such as adenine, guanine, uracil, thymine and cytosine possess promising physical and chemical properties similar to those of DNA. These properties included a high k and high thermal stability with lower molecular weights. Previous findings suggest DNA nucleobases can be used in electronic applications such as gate dielectrics for organic field effect transistors (Irimia-Vladu et al. 2010) (see Tab. 3.2).

Table 3.2. Dielectric constant, breakdown field, and dielectric loss tangent of adenine, guanine (Irimia-Vladu et al. 2010) and silicon.

Nucleobases	Adenine	Guanine	Silicon
Dielectric Constant (at l kHz)	~3.85	~4.35	~12.3
Breakdown Field (MV cm^{-1})	~1.5	~3.5	~0.3
Loss Tangent (at 100 mHz)	~4 x 10^{-3}	~7 x 10^{-3}	~5 x 10^{-3}

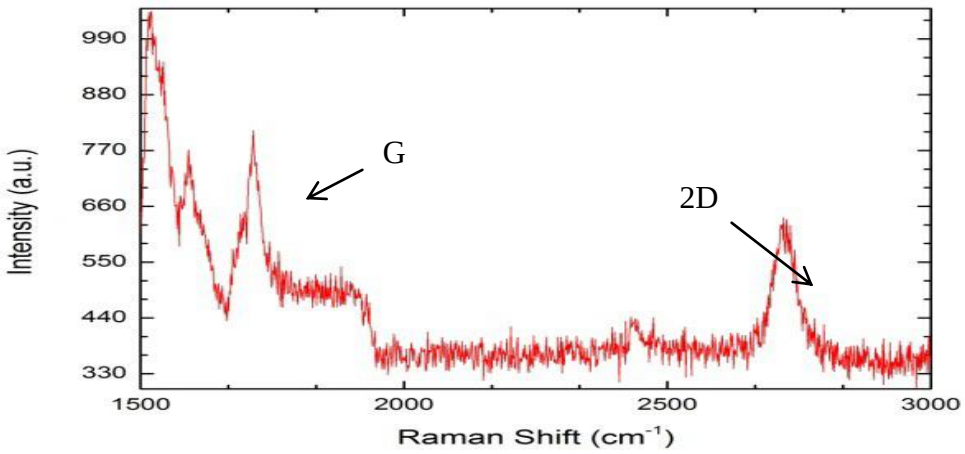


Figure 3.4. Raman spectrum of graphene with G band and 2D bands as the most notable peaks indicative of graphene (Williams et al. 2013).
Graphene is present as shown by the G and 2D peaks.

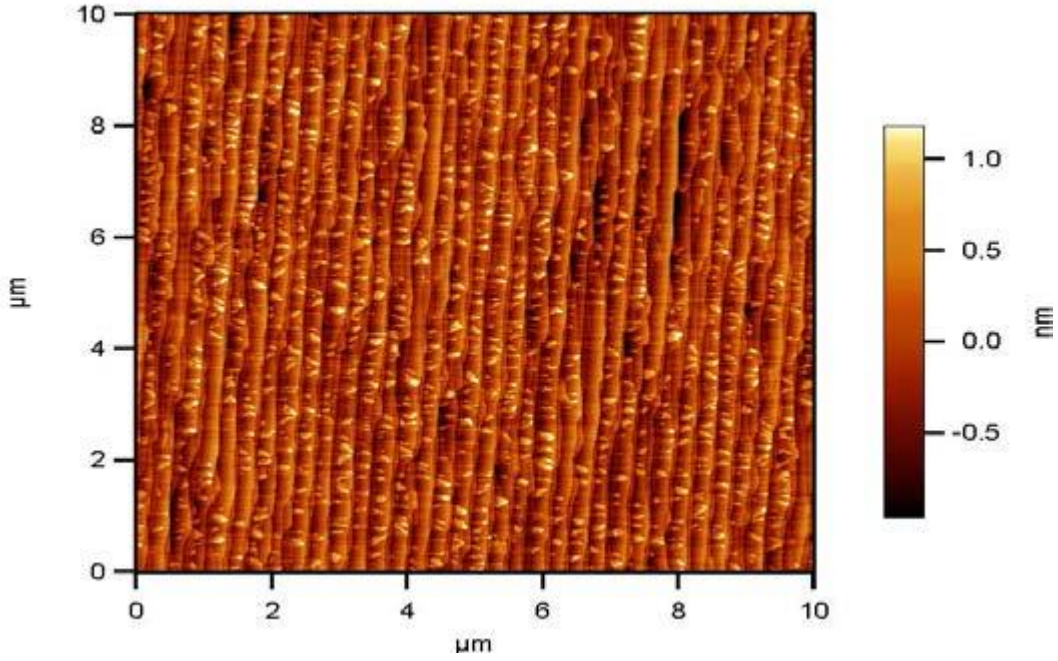


Figure 3.5. AFM of epitaxially grown graphene on SiC (Williams et al. 2013). Graphene is seen as steps or terraces.

IV. MATERIALS (SUBSTRATES/FILMS)

4.1 Rigid Substrates

Silicon Carbide as Non-Flexible Substrate

In this research, SiC was investigated as a non-flexible substrate. In a graphene-based *metal-insulator-semiconductor field effect transistor*, also known as a MIS-FET, graphene has been commonly deposited and epitaxially grown on rigid semi-insulating substrate such as SiC with a band gap ~ 3eV (10^{10} Ohm-cm) (Randhawa et al. 2007). SiC, commonly used for graphene epitaxial growth is composed of Si- and C-faces. As reported in my Master's thesis entitled "Dimensional Changes of Graphene through SiC Decomposition", graphene grown on C-face show visible patches of brighter/darker regions that correspond to thicker and/or thinner regions of graphene monolayers. In contrast, epitaxially grown graphene on Si-face appeared to be much more uniform in thickness. Atomic Force Microscopy (AFM) has provided visible images of SiC (Si- and C-face). Graphene on Si-face was smooth, but on C-face it appeared rough with many scratches. This was concluded to be a result of the Si-face subjected to the chemical and mechanical polishing (CMP). Due to these findings, the exploration of SiC (Si- and C-face) was the non-flexible substrate of choice. Other rigid substrates - silicon and glass slide were investigated to determine if their suitability in a GFET. It was found not to be a non-flexible alternative substrate.

Given the aforementioned research-based evidence, this study also utilized and performed the transfer process in a clean room environment. The transfer process allowed for monolayers of graphene to be stacked one at a time up to the desired thickness. After each graphene monolayer was deposited onto SiC it was rinsed thoroughly in toluene to

remove residual material from the thermal release tape (TR tape) and air dried under a fume hood. Reproducible, consistent and high bulk charge carrier mobility in the SiC, specifically, on the Si-face was observed. Dielectric films of guanine and PMMA were deposited on top of the graphene layers with titanium-gold-indium (Ti-Au-In) ohmic contacts used as the source and drain.

4.2 Flexible Substrates

Willow Glass flexible substrate

Flexible substrates were also explored in this study. Willow glass had a surface roughness of 0.295 nm, which is much lower than that of glass slide (SiO_x) with an RMS roughness = 3.03 nm. Atomic Force Microscopy was used to determine if Willow glass would be the flexible substrate of choice in comparison to glass slides. Guanine and PMMA were deposited onto Willow glass and glass slides to compare. In addition, guanine and PMMA films were deposited onto graphene layers. Other flexible substrates such as kapton, poly(dimethylsiloxane) (PDMS), and photo-print paper (laminate side) were investigated but determined not to be useful in the fabrication of a bio-based test platform.

Cleaning of Non-Flexible and Flexible Substrates

Substrates were cleaned and sonicated in 10 mL each of the following for 15 minutes:

- acetone
- methanol
- isopropanol

4.3 Guanine

It was postulated that we could use Physical Vapor Deposition (PVD) to deposit guanine film 60 nm thick onto graphene (Steckl 2007). The dielectric constant of guanine at 1kHz is 4.35, which is on the order of DNA dielectric constant k ~ 6, DNA-CTMA k ~ 7.8, and PMMA k ~ 3.5 (Hsu 2008). The breakdown voltage of guanine is ~ 3.5 MV/cm with a loss tangent of ~ 7 x 10^{-3} at 100 mHz (Irimia et al. 2010 and Li et al. 2009), unlike in DNA with a breakdown voltage of 46 MV/cm and a loss tangent less than 100 up to 30, 000 MHz and PMMA with breakdown voltage 3.5 MV/cm and a loss tangent of 2.8 at 0.01MHz. A few grams of guanine powder distributed by Sigma-Aldrich are seen on the Kimwipe (Fig.4.1).

Figure 4.1. Guanine powder prior to physical vapor deposition onto substrates.

V. FABRICATION METHODS

5.1 Deposition Techniques and CVD Graphene Transfer Process

Based on the abundance of the deposition techniques, CVD method was chosen together with graphene transfer process. Monolayers of graphene were grown on Cu foil by CVD and then transferred onto TR tape. These monolayers were transferred (i.e., rolled) onto different non-flexible and flexible substrates to determine which substrate can be used in the bio-based GFET test platform. Layers of 1, 2, 4 and 10 graphene monolayers were transferred onto these non-flexible and flexible substrates.

AFM was performed to determine the surface roughness of the graphene on non-flexible and flexible substrates - specifically, on glass slides and Willow glass. Hall transport measurements were conducted to determine the bulk charge carrier mobility of the graphene and assessed the changes prior and after PMMA and guanine depositions. Contact profilometry was a technique to verify that PMMA and guanine was successfully deposited at the desired thickness in nm.

5.2 Chemical Vapor Deposition of Graphene

One layer graphene was grown by CVD on Cu foil (see Fig.5.1). The CVD and transfer methods for graphene used in this study were slightly modified from the work detailed elsewhere (Bae 2010). A tube furnace (OTF-1200x-S ^{TM}, MTI Corp., CA) equipped with a scroll vacuum pump was used for CVD. A 4 x 4 in^2 Cu foil was placed in the furnace and heated up to 1000°C while hydrogen gas was injected at a pressure of 125 mTorr (Williams et al. 2014). The hydrogen-only reduction step continued for 30 min. at 1000°C. Then, a methane gas was injected at a pressure of 1.25 Torr for 30 min.

at 1000°C. The furnace was powered off and cooled down to RT while the flow of methane and hydrogen remained. The TR tape was carefully placed over the graphene coated Cu film to prevent any air bubbles from being entrapped followed by a 5 min. oxygen plasma treatment on the Cu side at 35 mW (Nitto Americas Inc., CA).

In this study, the TR tape that had been placed over the graphene coated Cu film was etched in $(NH_4)_2S_2O_8$ solution (100 mg/ml in DI water) for 2 hours, rinsed with deionized (DI) water, and dried with N_2 (Williams et al. 2014). The graphene layer was successfully transferred onto rigid and flexible 1x1 cm^2 substrates. One monolayer was transferred at a time with a toluene "rinse" between each transferred monolayer onto the substrate to remove residual material from the TR tape. The transfer process was achieved by heating up the substrate/graphene/TR tape at 125°C which resulted in the peeling of the graphene off the TR tape from the substrates. This process was completed in a clean room and continued until the desired numbers of layers (thickness) were transferred onto the wafers.

5.3 Spin-Coat of PMMA - a Reference Gate Dielectric

PMMA was deposited at desired thickness onto non-flexible and flexible substrates. The following parameters were used in this research:

Poly(methyl methacrylate):

- 3 wt.% Anisole in PMMA
- 100 µL @ 1000RPM
- 30 seconds

5.4 Physical Vapor Deposition of Guanine

Guanine was deposited onto graphene-based rigid and flexible substrates by Physical vapor deposition (PVD). PVD is a vacuum-based technique used to deposit thin films

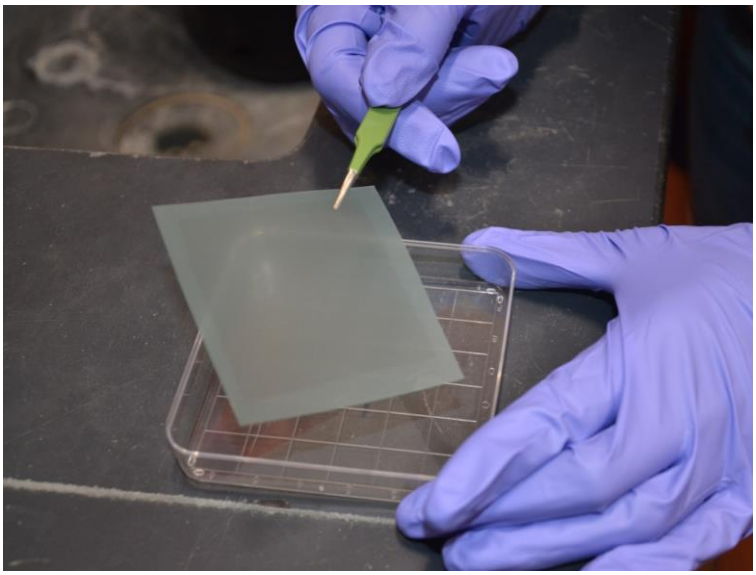


Figure 5.1. 1-MLG of graphene on thermal release tape.
Graphene on TR tape after transfer from Cu foil substrate.

by condensation of a vaporized form of a desired material onto substrates. Physical vapor deposition is a vapor coating technique that allows for the transfer of a material on an atomic level. PVD is similar to CVD, but in the former the material being deposited starts out in solid form, unlike in CVD where the materials are introduced into a reaction chamber in gaseous forms (Mattox 2010).

In PVD (see Fig.5.2), a material is deposited and transformed into a vapor which is transported across a region of low pressure from the source to the substrate as a thin film. During the evaporation process in PVD the target material - guanine is deposited by a high energy ion bombardment. In turn, the deposition process occurs when the actual thin film material is coated onto the substrate.

PVD results in improved efficiency and greater device performance compared to solvent-based deposition techniques. It is also a technique that is viewed as an environmentally friendly deposition technique (Mattox 2010). PVD was a solvent-less based process technique that occurred in a controlled vacuum chamber.

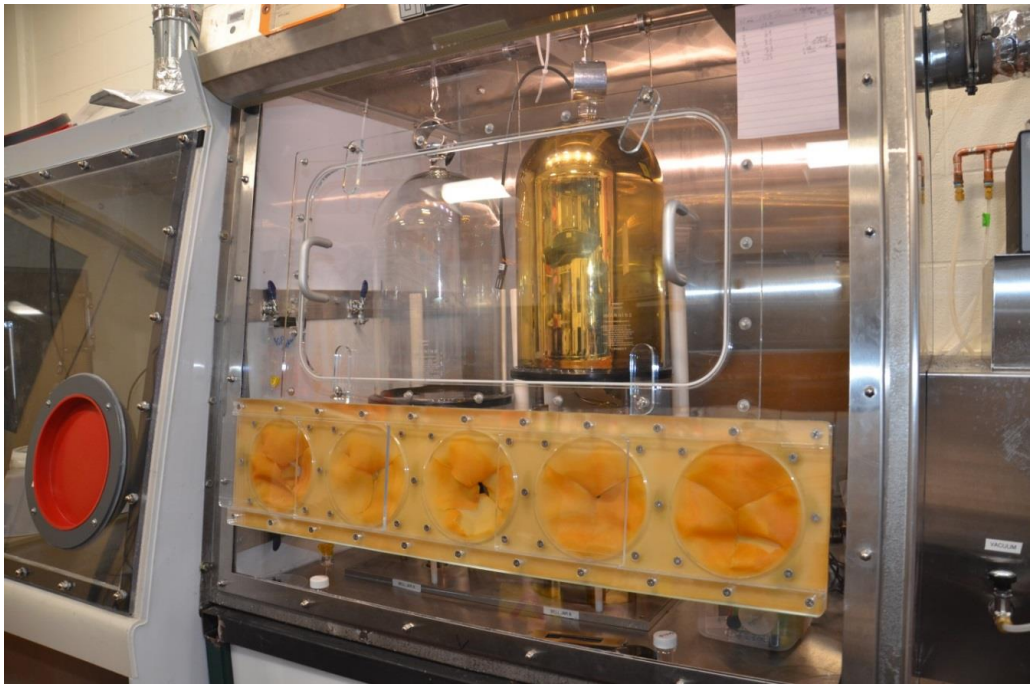


Figure 5.2. Glove box and physical vapor deposition (PVD) system.
PVD of guanine.

VI. CHARACTERIZATION TECHNIQUES

6.1 Raman Spectroscopy

Raman spectroscopy is a light scattering technique used to diagnose internal structures of molecules and crystals. In this research, Raman spectroscopy was used to determine the presence of graphene on each sample substrate. A light of known frequency and polarization was scattered from a sample and analyzed. The frequency scale represented the Raman shift (energy of a free vibration of a molecule). The peaks occurred at the frequencies of Raman active modes. In graphene, the D, G, and 2D band were seen in the Raman spectrum of all samples. A Raman spectrum occurred as a series of discrete frequencies shifted symmetrically above and below the frequency of the exciting radiation and in a pattern characteristic of the sample molecule. Stokes lines were given as the low-frequency side of the incident radiation and the anti-stokes lines were on the high frequency side of incident radiation. In a quantum mechanical representation of the origin of Raman lines, the incident photon elevates the scattering molecule to a quasi-excited state whose height above the initial energy level equals the energy of the exciting radiation (Willard et al. 2012) (see Tab. 6.1 for the parameters of Raman spectrometer used here).

6.2 Atomic Force Microscopy

AFM requires neither a vacuum environment nor any sample preparation and it can be used in ambient and/or liquid environments. AFM is a method used to image the morphology of a variety of surfaces. Compared to other conventional microscopic techniques, AFM probes a sample and produces measurements in three dimensions (x, y, and z).

Figure 6.1. Raman spectrometer.
Samples analyzed for graphene-based peaks.

Table 6.1. Raman spectroscopy parameters for graphene.

Laser Wavelength	532 nm
Laser	On
Laser Power	10.0 W
Aperture	25 μm
Grating	900 lines/mm
Estimated Resolution	5.8-8.8 cm^{-1}
Estimated Spot Size	0.5 μm
Allowed Range	3549 to 26 cm^{-1}
Minimum range limit (cm^{-1})	50
Maximum range limit (cm^{-1})	3500
Accessory	Microscope
Objective	50x

This allows for three-dimensional images of a sample surface. Atomic resolutions of 0.1 nm - 1.0 nm in the x-y direction and 0.01 nm in the z direction can be observed (Blanchard 1996).

Atomic Force Microscopy (see Fig.6.2) key components are as follows:

- Sample
- Split Photodiode detector
- Cantilever
- Tip
- Piezoelectric Scanner
- Controller
- Laser

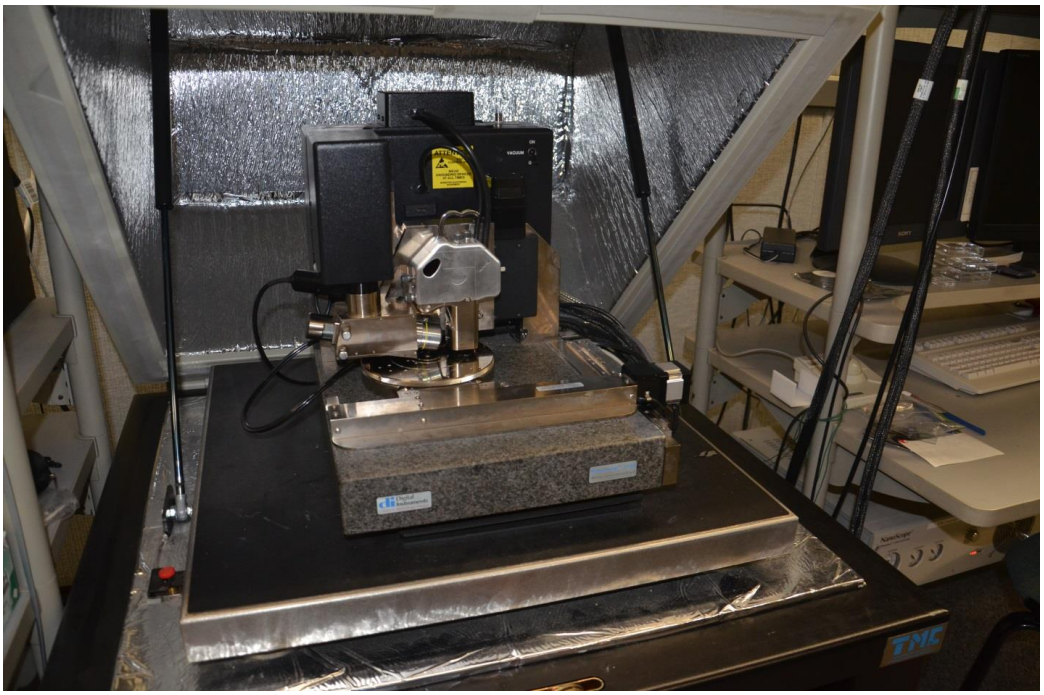


Figure 6.2. Atomic Force Microscopy system.
In this research, the tapping mode was used on each sample.

AFM was used to determine the surface roughness of the rigid and flexible substrates with graphene standalone and gate dielectric/graphene layers to assist in the determination of the ideal substrate to be used in the bio-based test platforms. Images were assessed for their roughness and compared (see Fig. 7.7) by using the Nanoscope IIIA software. Each sample was placed onto a metal circular plate that was placed onto an XYZ piezo scanner. The surface of the sample was analyzed with use of an optical microscope. An AFM head was placed onto the scanner and the optical microscope was focused. With use of the coarse adjustments, the tip was lowered and the AFM leveled. The photo detector was adjusted as well as the switch into dynamic mode. The dynamic mode deals with the oscillations and frequency of the cantilever (Blanchard 1996).

An image was captured with use of several parameters:

- Scan size: 5.00 µm
- Scan rate: 0.500 Hz

Surface roughness values observed by AFM were taken for the glass slides and Willow glass, 4-MLG transferred on a glass slide and on Willow glass, PMMA/4-MLG/glass slide, and guanine/4-MLG/WG (Blanchard 1996). These images are depicted in this dissertation (see Results and Discussion section).

6.3 Hall Effect Measurements

Hall Effect measurements are used in the field of electronics as well as device manufacturing. Important parameters that can be determined by Hall Effect measurements are carrier mobility (µ), carrier concentration (n), Hall coefficient (R_H), magnetoresistance (R), n or p type conductivity, and resistivity. The Hall voltage (V_H) was measured by the placement of a magnetic field perpendicular to the sample.

The graphene and/or gate dielectric/graphene samples were placed in a uniform magnetic field. A current was passed through the graphene-based samples. The transverse current occurred due to the current (I) and magnetic field (B). The potential (V_H) was then able to be measured across the sample in which resistivity and thickness were determined. After these parameters were obtained - magnetic field (B), current (I), potential (V_H), thickness (t), and resistivity (ρ), the Hall mobility (μ_H) can be calculated by the following equation (Green 2011) (Eq.(2)).

$$\mu_H = | V_H t|/BI\rho \quad (2)$$

Generally, the Hall measurement system can actually be used to determine: Hall voltage (V_H), carrier mobility (μ), Hall coefficient (R_H), resistivity (ρ) (four-point probe or Van der Pauw), magnetoresistance (R), and the conductivity (n or p type). This research focused on charge carrier mobility of the graphene only and gate dielectric/graphene/ substrates. The above parameters were obtained via a four point probe measurement. Both the Van der Pauw and Hall effects method use four point contacts that force a current and measure voltage. In particular, the Hall Effect measurement contains a current that is forced on nodes of a sample and the voltage is measured on the opposite nodes. Moreover, in the Hall Effect measurement, a transverse magnetic field is applied in contrast to Van der Pauw method where there is no magnetic field is applied (Green 2011).

The Hall Effect is derived from the Lorentz which is the force on a point charge due to electromagnetic fields (Green 2011). Essentially, the Hall Effect can be observed when the combination of a magnetic field through a sample and a current along the length of the sample creates an electrical current perpendicular to both the magnetic field and

the current (Green 2011). This, in turn, creates a transverse voltage that is perpendicular to both the magnetic field and the current. In Fig. 6.3, an illustration of the Hall Effect is presented from which the bulk charge carrier mobility was determined in the graphene-based samples.

Hall Effect measurements were taken prior and post dielectric deposition. A Hall measurement setup for a non-flexible 1x1 cm^2 4-MLG/SiC (Si-face) is depicted in Fig. 6.4.

6.4 Contact Profilometry

Contact profilometry measurements were performed to measure film thicknesses of dielectric materials (see Fig.6.5).

6.5 X-ray Photoelectron Spectroscopy

XPS is defined as a surface characterization technique that uses photo-ionization and energy-dispersive analyses of emitted photoelectrons from a material in order to determine the composition and electronic state of the surface region of a sample. A photon is absorbed by an atom in a molecule of a material which causes ionization and emission of an inner shell electron. A material is analyzed in a high vacuum chamber

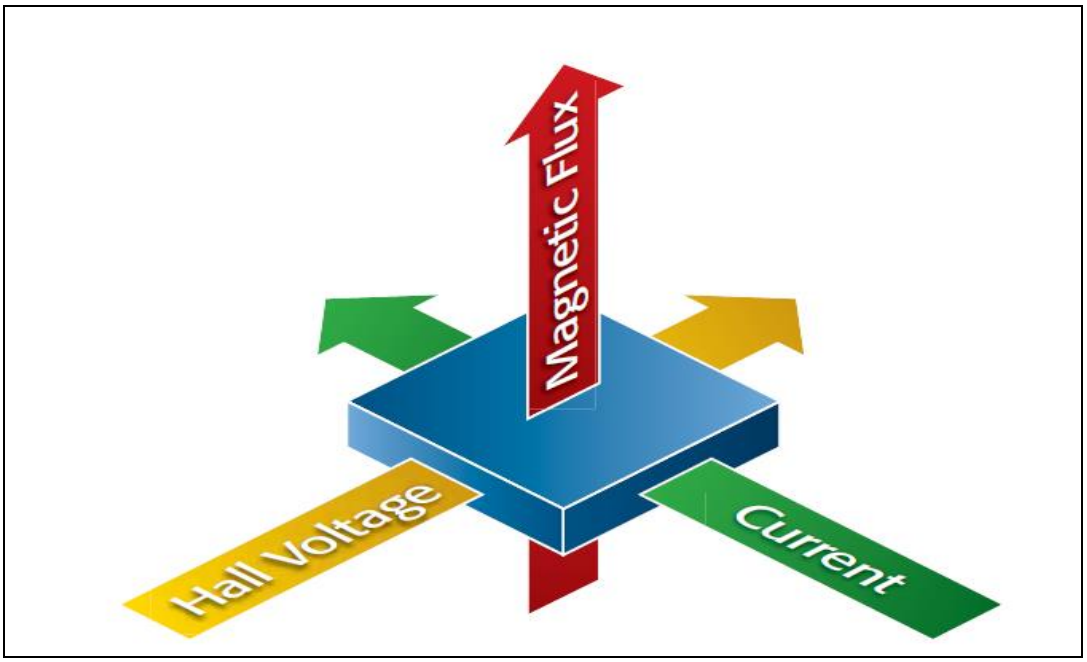


Figure 6.3. Illustration of the Hall Effect measurement (Green 2011).
Four point probe measurements or commonly known as the Van der Pauw method were used for each sample.

Figure 6.4. Four point probe Hall measurement setup.
Hall measurement sample setup of 1x1 cm^2 4-MLG/SiC (Si-face).

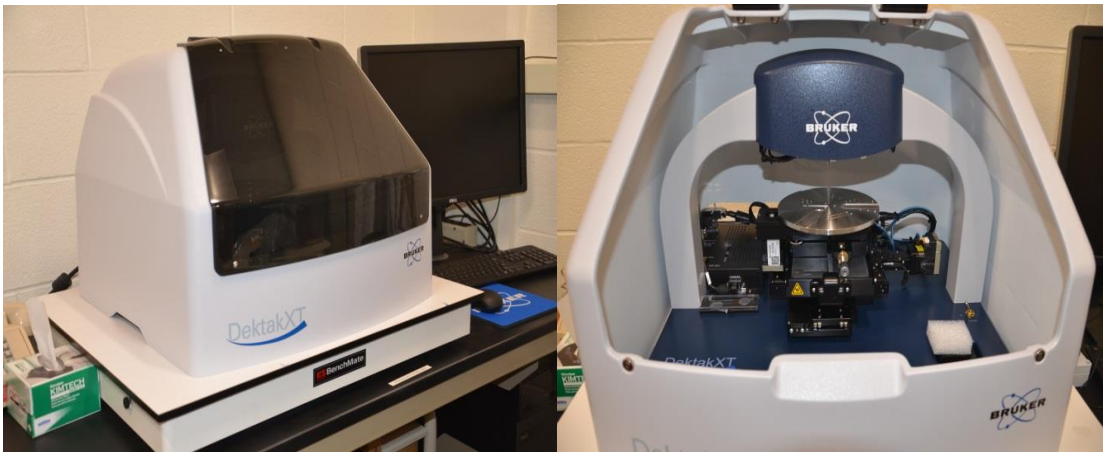


Figure 6.5. Contact profilometry measurement setup used to determine thickness of thin films.
Guanine and PMMA were measured for their thicknesses after deposition onto graphene.

~ 10^{-10} Torr. It also reduces re-contamination of a cleaned sample (Grant 2003).

XPS is an analytical surface technique that is capable of measuring the composition to only ~ 10 nm depth. The limited depth is due to inelastic scattering of electrons. X-ray intensity decreases slowly with an increase in depth, although X-ray intensity can go up to thousands of atomic layers into a sample. Photoelectrons that are produced near the surface of a sample have a higher probability of ejection from the surface without the loss of energy. These are the photoelectrons that produce a peak in a spectrum. Photoelectrons that lose energy appear in the bulk (background) of a spectrum at a much lower kinetic energy than photoelectrons that have escaped near the surface of a sample. The analysis depth is determined by the electron mean free path (i.e. how far an electron can travel without losing energy). Energy ($h\nu$) ejects an electron from the K shell as a photoelectron. The XPS system used in this research is presented in Fig.6.6. The binding energy is specific to an electron subshell of a particular atom - this allows for all elements, except hydrogen and helium to be identified. XPS is useful for studying chemical shifts allowing information to be obtained about the chemical environment of surface atoms. One must focus on the chemical shifts once the sample has reached the detector after emission. Prior to electron emission of a material, the total energy of a system is the energy of an X-ray photon $h\nu$ plus the energy of the target atom in its initial state E_i. After an emission of an electron, the total energy of the system becomes the kinetic energy of the emitted electron E_k plus the ionized atom in its final state E_f. The number of electrons detected is measured as a function of kinetic energy. The electron's kinetic energy (KE) is then converted to binding energy (BE). Thus, the following equation is used (Grant 2003) (Eq.(3)).

Figure 6.6. X-ray photoelectron spectroscopy image of sample measurement setup. Graphene-based samples were analyzed for impurities.

$$KE = \text{X-ray energy} - BE \quad (3)$$

The X-ray energies used in this research are from an aluminum source: 1486.6 eV.

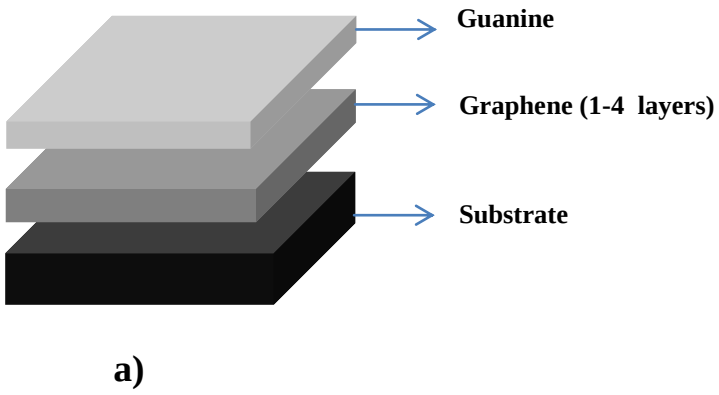
Any change in the oxidation state and/or the chemical and physical environment of atoms of a sample, will cause chemical shifts in peak positions in the XPS spectra. Consequently, the atoms of a higher positive oxidation state were postulated to exhibit a higher binding energy due to Coulomb interaction between the photo-emitted electron and the ion core of the material. Particularly, the atoms of a higher positive oxidation state were oxygen and carbon. The line width of a peak can help in the determination of the atom present in the sample. The peak intensity in the spectrum is determined by the number of photoelectrons from a specific element that are emitted at an angle θ with respect to the material surface, then enters the spectrometer and appears in spectra (Grant 2003).

Preliminary XPS analyses determined that Cu was present in the graphene samples. XPS was performed on TR tape only and etched CVD 1-MLG graphene on TR tape to determine the presence and/or source of Cu atoms in the graphene during the transfer process. This method helped determines how to optimize the graphene transfer process to remove all Cu atoms (if any) which may have been present on the graphene-based samples after the transfer process onto the substrates. XPS spectra did not depict any Cu atoms present on the graphene samples. However, carbon was at a high percentage due to the one monolayer of graphene.

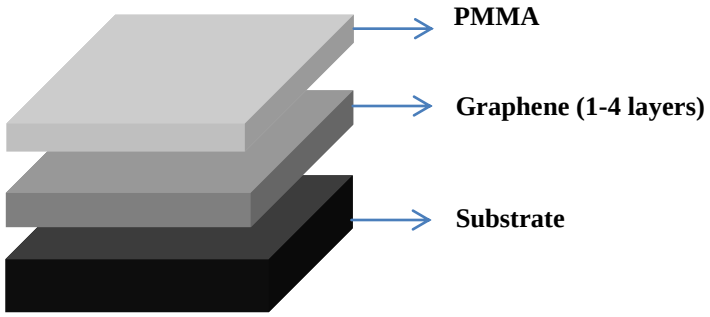
VII. RESULTS AND DISCUSSION

7.1 Schematic of Metal/Insulator/Metal (MIM) Test Platforms

Two test platforms were fabricated for comparison of the dielectric properties of guanine and PMMA at thicknesses of 60 nm, 300 nm, and 1 μm thick. The first test platform had guanine only or PMMA only on top of 4-MLG/Willow glass substrate (see Fig.7.1). Dielectric thicknesses below 60 nm were too thin and produced non-uniform thin films. In turn, 60 nm, 300 nm and 1 μm were chosen and studied for uniformity. Graphene was the back electrode in both configurations.



a)



b)

Figure 7.1. Schematic of graphene test platform A: a) with guanine as gate dielectric layer and b) PMMA as gate dielectric layer (Williams et al. 2015).
Guanine or PMMA *only* were the gate dielectric layers.

In Fig. 7.1a, guanine was used as the gate dielectric material deposited onto graphene monolayers (Williams et al. 2014). In Fig. 7.2, guanine was the passivation layer (e.g., a hermetic seal) to preserve graphene's transport properties. Monolayers of graphene (MLG) were stacked on top of each other on the surface of the SiC (Si- and C-face) substrate.

SiC was used as a rigid substrate due to its lattice match to the graphitic structure. Glass slides were used due to availability and low cost. High resistivity silicon as a substrate was used because of availability and use in graphene growth.

Results showed that the graphene used by the transfer method prior to and after PMMA and guanine depositions were all p type. Charge carrier concentrations values were on the same order of magnitude of 10^{12}-10^{13} cm^{-2} and resistivity values of 10^{2}-10^{3} Ω/sq. Charge carrier mobility of 1- and 2-MLG was measured on glass, SiC (Si- and C-face). We observed irreproducible charge carrier mobility in samples with 2-MLG in contrast to 4-MLG. Glass slides had reproducibility in bulk mobility which showed 270 cm^2/Vs at the first monolayer but a decrease in bulk mobility between the 2^{nd} monolayer, 660 cm^2/Vs and the 4^{th} monolayer, 453 cm^2/Vs. A similar trend was observed in C-face samples, with mobility decreasing between the 1^{st} monolayer, 920 cm^2/Vs and 2^{nd} monolayer, 690 cm^2/Vs. Samples of Si-face had an increase in mobility as the stacking of graphene monolayers increased (see, Fig.7.3).

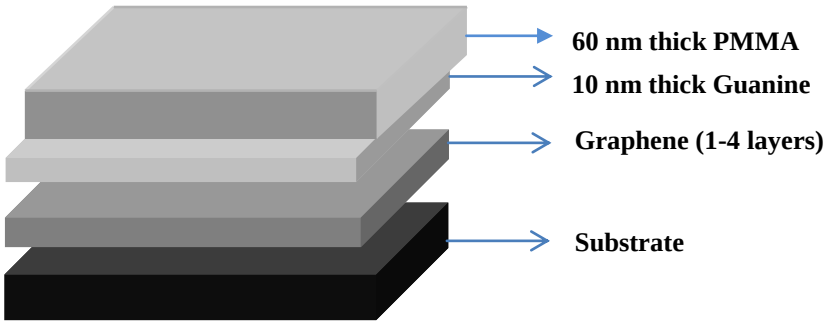


Figure 7.2. Schematic of graphene test platform B.
Guanine was the passivation layer and PMMA was the gate dielectric layer.

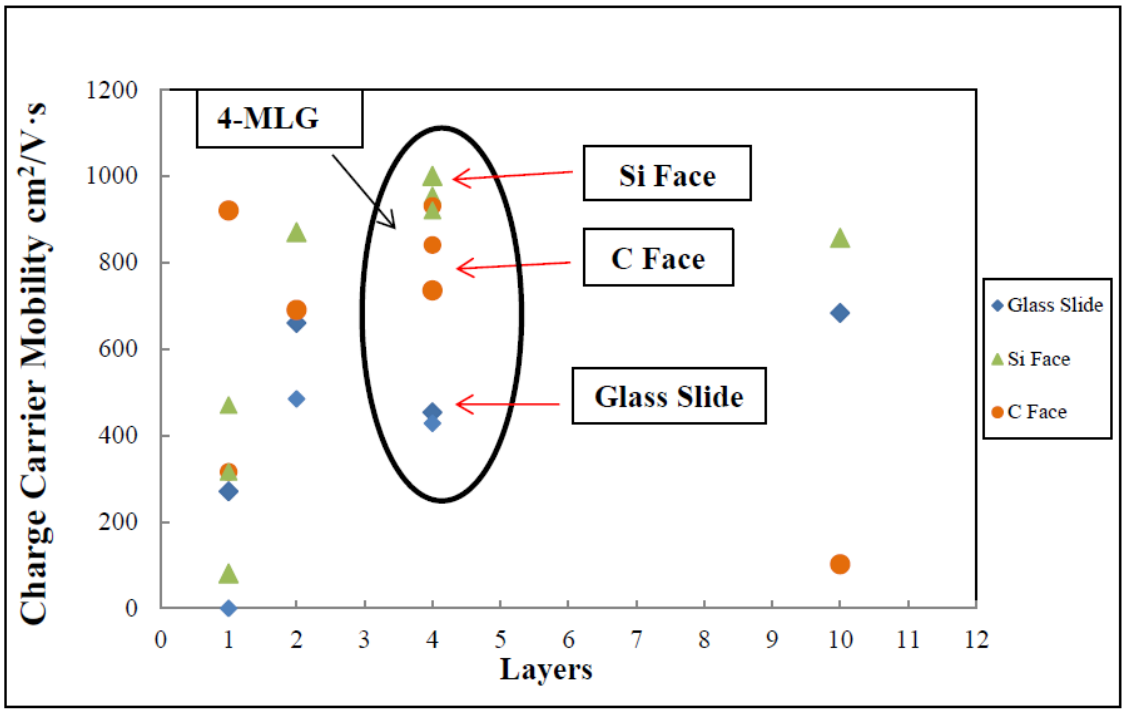


Figure 7.3. Plot of 1, 2, 4, 10-MLG on SiC (Si- and C-face), glass slide and silicon vs. bulk mobility cm^2/Vs.
SiC (Si- and C-face) had the most consistent and reproducible charge carrier mobility at 4-MLG (Williams et al. 2015).

Graphene was transferred at 1, 2, 4 and 10-MLG (Si-face, C-face and glass slides) to determine whether there was an increase in bulk mobility with an increase in graphene monolayers. At 10-MLG graphene bulk mobility was inconsistent for Si-face, C-face and glass slides. This data is plotted in Fig. 7.3. Charge carrier mobility of 1-, 2-, and 4-MLG were measured on Si-face, C-face and glass slide. An increase of graphene mobility in average for the graphene films on SiC (Si- and C-face) substrates have been observed as the stacking of graphene monolayers was increased up to 4-MLG. In contrast, the glass slides had a maximum graphene mobility of 572 cm^2/Vs at 2-MLG (see Fig. 7.4). Four monolayers of graphene were transferred onto silicon. Silicon 4-MLG bulk mobility of 268 cm^2/Vs, 581 cm^2/Vs, and 734 cm^2/Vs were inconsistent and irreproducible. Graphene with PMMA had a decrease in bulk mobility of ~ 42 % at RT after 3 days evidenced in Fig. 7.5. Graphene bulk charge carrier mobility decreased ~ 10% from its initial value from day 1 with guanine (Williams et al. 2015) (see Fig. 7.5). This may suggest that guanine can act as a passivation layer for the 4-MLG in response to environmental conditions (e.g., temperature, pollutants, water vapor, oxygen, carbon dioxide, nitrogen, and so on). Relative humidity studies under ambient conditions were investigated to determine the effect of moisture and oxygen on graphene *only* stability and graphene with the gate dielectric material on top to determine which dielectric material degrades faster - guanine or PMMA. The samples were left in an open box in air where a humidity meter and thermometer probe was placed to monitor the relative humidity up to six days. Since the measured graphene mobility was more reproducible at 4-MLG, this configuration was selected. The next section will focus on the studies of the 4-MLG layers in terms of stability under ambient conditions.

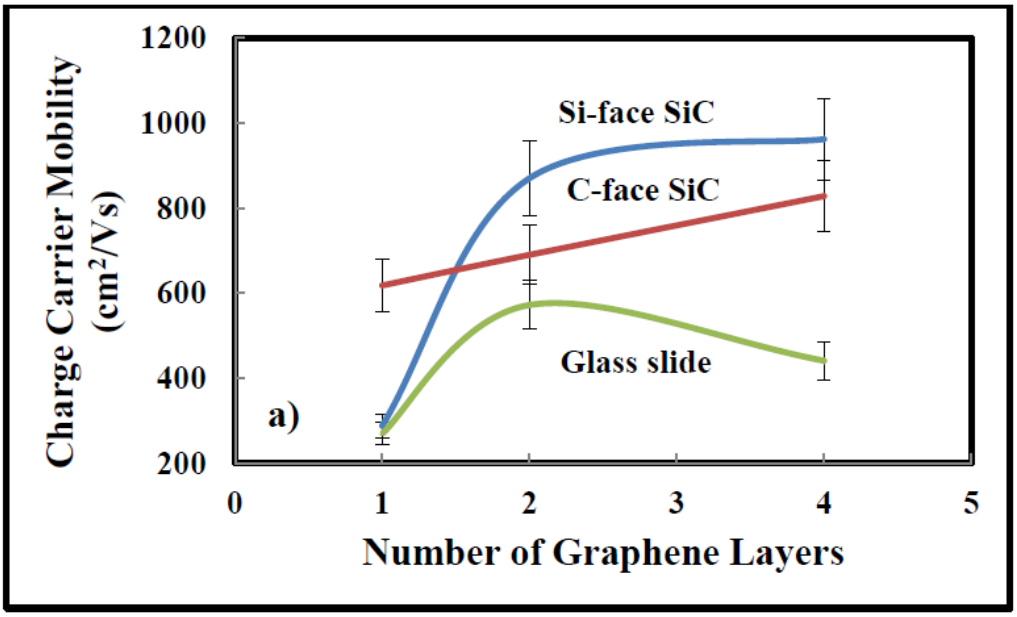


Figure 7.4. Charge carrier mobility as a function of 1, 2, and 4-MLG on Si - and C-face (SiC) and glass slide substrates (Williams et al. 2015).
Highest bulk mobility of graphene on Si- and C-faces are at 4-MLG whereas with the glass slide substrates with a maximum graphene bulk mobility at 2-MLG.

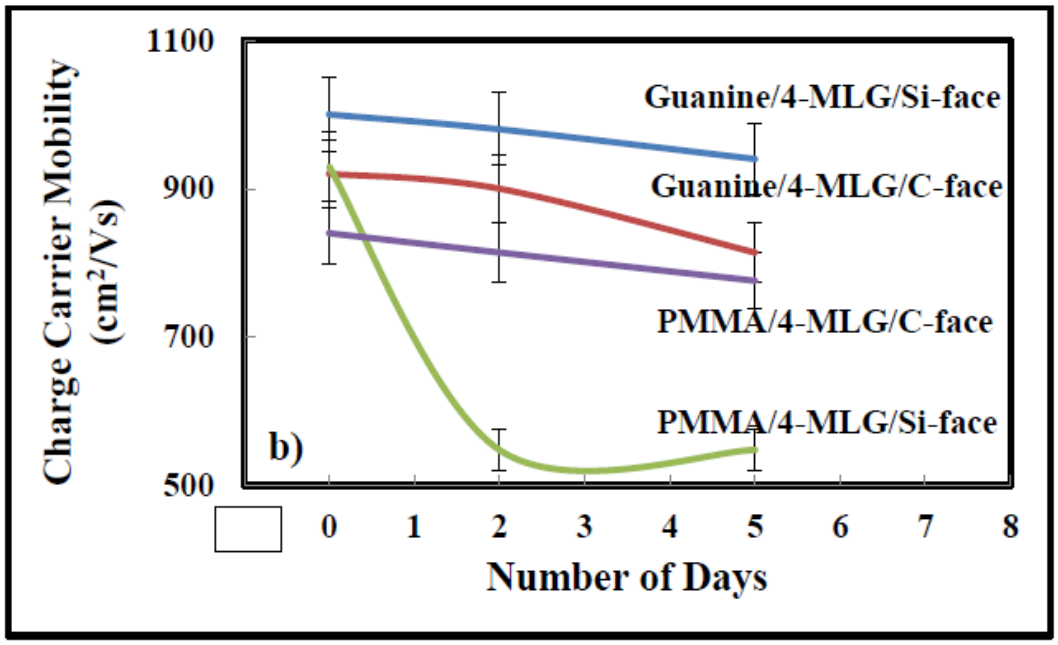


Figure 7.5. Plot of rigid film stability study of PMMA and guanine deposited onto graphene on Si- and C-face (Williams et al. 2015).
Guanine/4-MLG/Si- and C-face appeared to be most stable at RT in air over several days compared to Si- and C-face PMMA/4-MLG Si- and C-face.

7.1.1 Graphene Transfer on Rigid Substrates

Initial transport measurements on transferred graphene were performed on non-flexible substrates-SiC (Si- and C-face), glass slides, and silicon to determine the ideal rigid substrate in a test platform of a bio-based GFET. This initial study indicated that 4-MLG on the Si-face, C-face, and glass slides had the most consistent and reproducible Hall transport measurements. All samples were p type. These data are presented in Tab. 7.1 (Williams et al. 2015).

7.1.2 Graphene Transfer on Flexible Substrates

An investigation into flexible substrates: kapton, PDMS, photo-print paper, and

Table 7.1. Four monolayers of graphene on rigid substrates.

Substrate	Charge Carrier Mobility (cm^2/Vs)			Average Charge Carrier Concentration ($10^{13}cm^{-2}$)	Average Resistivity (Ω/sq)
	0^{th} Day	2^{nd} Day	5^{th} Day		
Si-face SiC	**870 ± 44**	**682 ± 34**	**652 ± 33**	**1.40 ± 0.07**	**684 ± 34**
C-face SiC	**690 ± 35**	**614 ± 31**	**621 ± 31**	**1.18 ± 0.06**	**849 ± 42**
Glass Slide	**441 ± 25**	**479 ± 79**	**462 ± 66**	**3.96 ± 0.20**	**195 ± 10**

Willow glass was performed to determine whether the graphene-substrate interface could impact graphene electrical properties (i.e. charge carrier mobility, resistivity, and charge carrier concentration) (Williams et al. 2013). Here, 4-MLG was transferred onto flexible substrates: kapton, PDMS, photo-print paper, and Willow glass. Kapton, PDMS, and photo-print paper were chosen as flexible substrates due to their availability and low cost. On the other hand, Willow glass was chosen for its availability *only*. Table 7.2 summarizes the results (Williams et al. 2015).

Table 7.2. Initial studies of four monolayers of graphene flexible substrates (Williams et al. 2015)

Substrate	Charge Carrier Mobility (cm^2/Vs)	Yield of Usable Sample (%)
Kapton	**273 ± 235**	**50**
Photo-Print Paper	**38**	**16**
PDMS	**0**	**0**
Willow Glass	**530 ± 342**	**100**

Studies of 4-MLG on kapton and PDMS appeared to have inconsistent charge carrier mobility and open circuits on the graphene-based samples. Photo-print paper had surface adhesion issues between the graphene-laminate surfaces (Williams et al. 2014). The most suitable flexible substrate appeared to be Willow glass with consistent and reproducible graphene charge carrier mobility (Williams et al. 2015).

7.1.3 Transferred Graphene: Willow Glass Electrical Properties under Ambient Conditions and Lifetime-degradation Studies

Hall transport measurements on 4-MLG on Willow glass at room temperature in over a period of several days were studied (Williams et al. 2015). Average initial values of Hall transport measurements performed on the 0^{th}, 2^{nd} and 5^{th} days of 4-MLG on Willow glass is depicted in Fig.7.6. Relative humidity for all samples on the first day averaged ~26.6 ±5.4 % at room temperature in air. Humidity values did not fluctuate significantly between the 0^{th}, 2^{nd} and 5^{th} day. PVD guanine onto 4-MLG/Willow glass and spin-coat PMMA onto 4-MLG/Willow glass were examined (see Tab. 7.3).

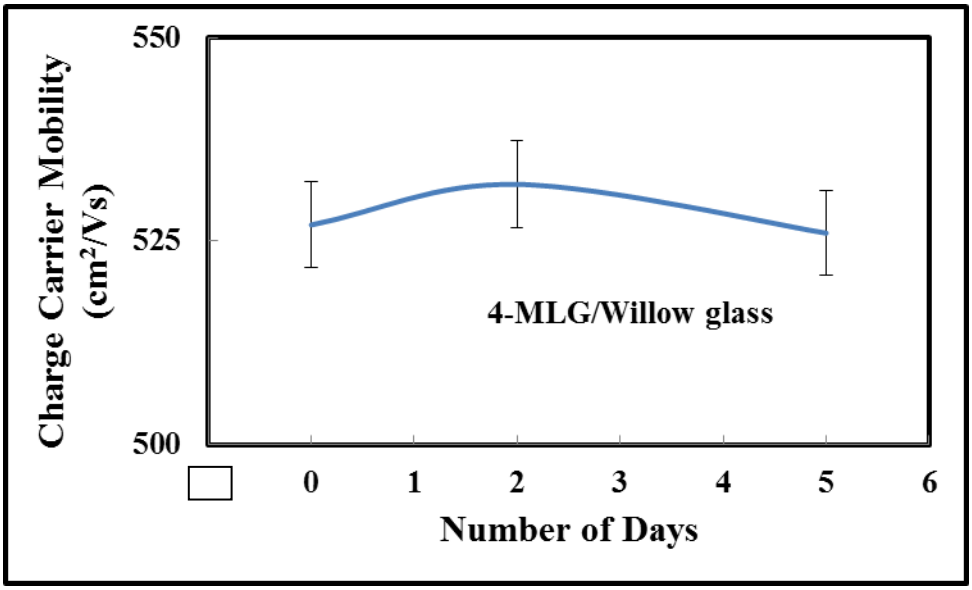


Figure 7.6. Average graphene stability Hall transport measurements on Willow glass over a period of several days (Williams et al. 2015).
Willow glass bulk charge carrier mobility appeared to be electrically stable over a number of days at room temperature in air.

Table 7.3. Electric characterization of 4-MLG transferred on Willow glass substrate (Williams et al. 2014).

Substrate	Charge Carrier Mobility (cm^2/Vs)			Average Charge Carrier Concentration ($10^{13}cm^{-2}$)	Average Resistivity (Ω/sq)
	0^{th} Day	2^{nd} Day	5^{th} Day		
PMMA/4-MLG/WG	346 ± 74	325 ± 82	327 ± 86	2.83 ± 0.91	649 ± 0.71
Guanine/4-MLG/WG	440 ± 58	436 ± 70	437 ± 69	5.39 ± 1.82	281 ± 0.81

With guanine on top, the graphene charge carrier mobility appeared to be more stable than with PMMA. Charge carrier concentration and resistivity of graphene (with guanine on top) remained relatively constant over several days as opposed to graphene with PMMA.

7.2 Atomic Force Microscopy Results

AFM (scan size = 5 μm, scan rate = 1.489 Hz, data scale 15 nm, samples/line = 512) surface roughness measurements (see Fig.7.7) of glass slides and Willow glass showed a higher surface roughness in the glass (standalone) at RMS = 3.030 nm compared to WG with an RMS = 0.295 nm. PMMA/4-MLG/WG had an RMS = 0.870 nm with guanine/4-MLG/WG RMS = 1.670 nm. It appeared that the surface roughness values are dependent on the type of deposition methods of the guanine and PMMA. In spin-coating, an even distribution of PMMA was spread onto the 4-MLG unlike in PVD where guanine was vaporized onto the 4-MLG. Implications of AFM results indicate the

need to further examine these samples with near-edge X-ray absorption fluorescence spectroscopy (NEXAFS) as evidenced of WG being the most suitable substrate of choice. Surface roughness values are depicted in Tab. 7.4.

Table 7.4. Willow glass vs. glass slide (SiO_x) *itself* and 4-MLG/substrate surface roughness measurements.

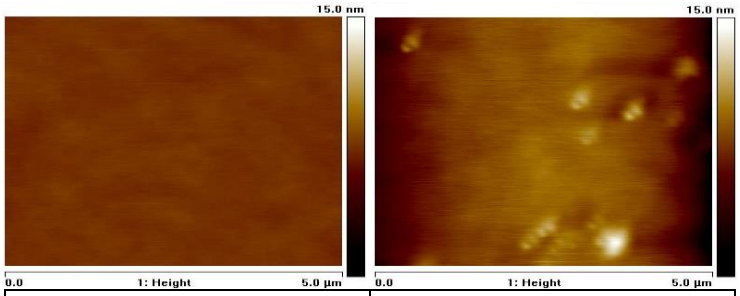
	Willow Glass (nm)	Glass Slide (nm)
Substrate Only	**0.295**	**3.030**
4-MLG/Substrate	**4.850**	**5.940**

Table 7.5. Surface roughness of graphene *itself* and gate dielectric/graphene on Willow glass (Williams et al. 2014).

Sample/Willow Glass Substrate	Surface Roughness (nm)
Substrate *Only*	**0.295**
4-MLG	**4.850**
PMMA	**0.420**
Guanine	**0.578**
PMMA/4-MLG	**0.870**
Guanine/4-MLG	**1.670**

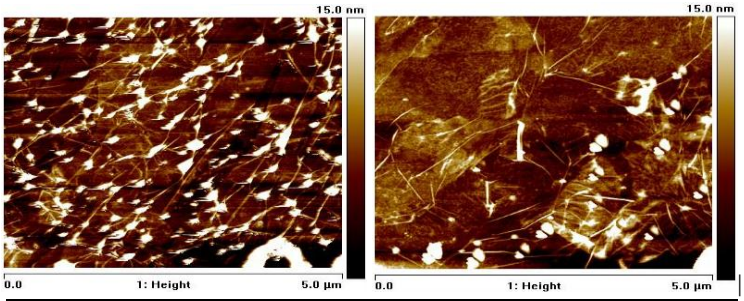
In Tab.7.5, the surface roughness values of the PMMA/4-MLG/WG were found to be less than that of guanine/4-MLG/WG samples which may be due to the deposition technique of the gate dielectric layer.

7.3 MIM Results of Test Platform A and B



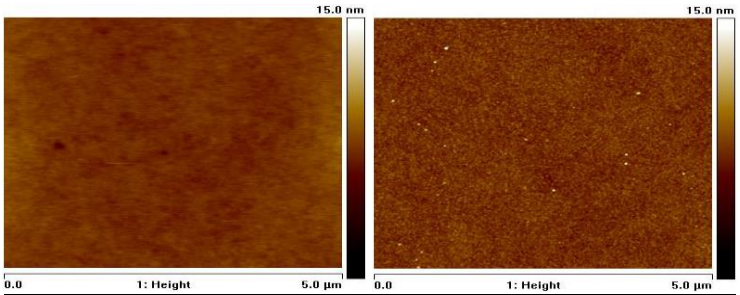
Willow Glass RMS=0.295 nm	Glass Slide RMS=3.030 nm

a)



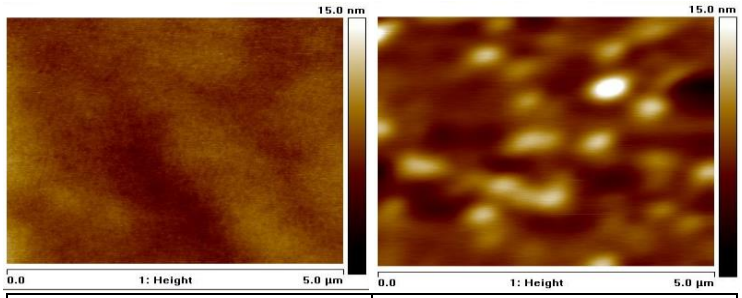
4-MLG/Willow Glass RMS=4.850 nm	4-MLG/Glass RMS=5.940 nm

b)



PMMA/Willow Glass RMS=0.420 nm	Guanine/Willow Glass RMS=0.578 nm

c)



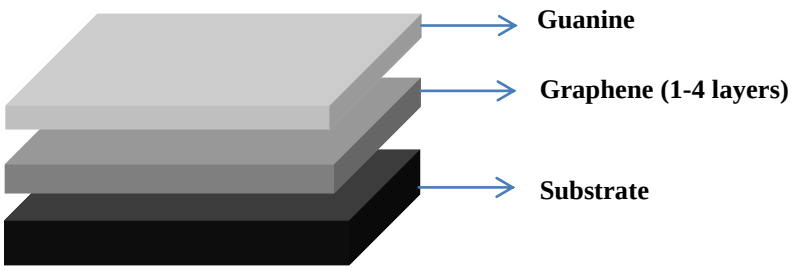
PMMA/4-MLG/Willow Glass RMS=0.870 nm	Guanine/4-MLG/Willow Glass RMS=1.670 nm

d)

Figure 7.7. AFM images of a) WG and glass; b) 4-MLG of graphene/WG and 4-MLG/glass; c) PMMA/WG and guanine/WG; d) PMMA/4-MLG/WG and guanine/4-MLG/WG.

7.3.1 Test Platform A

Test platform A (see Fig.7.1a):



Microscopic images of guanine/4-MLG/WG and PMMA/4-MLG/WG were taken to observe any overshadowing after completion of Ti-Au electrode deposition in the fabrication of these test platforms. Transmission electron microscopy (TEM) grids were used for electron-beam (E-beam) deposition of Au as the top electrode onto the dielectric layers in these test platforms. Transmission electron microscopy grids were carbon on 200 Mesh (lines/inch) Cu, 94x94 μm bar width, and bar width + hole width = pitch . The pitch was 125 mm bar dimension and hole dimension. Test platform measurements were determined via the probe station as seen in Fig.7.8.

Figure 7.8. Probe station.
Measurement of all graphene-based samples was conducted at this probe station.

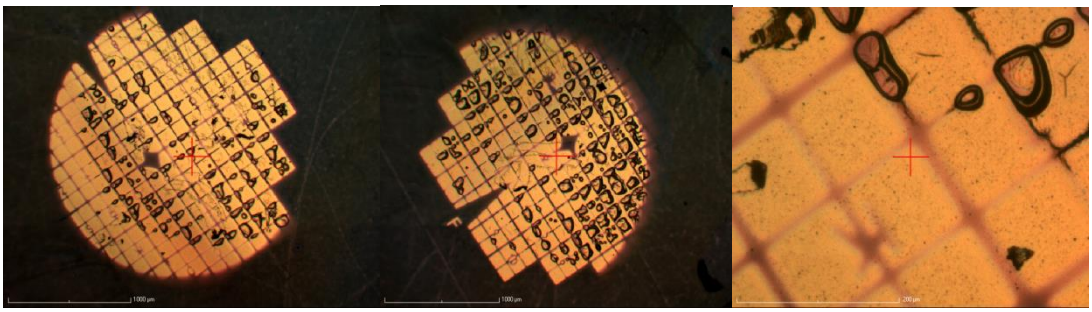


Figure 7.9. Optical microscope images of 1 μm thick/PMMA/4-MLG/WG after-electrode deposition.

PMMA appeared not to adhere to the surface of the graphene due to “defects” present on the Au film (Fig.7.9).

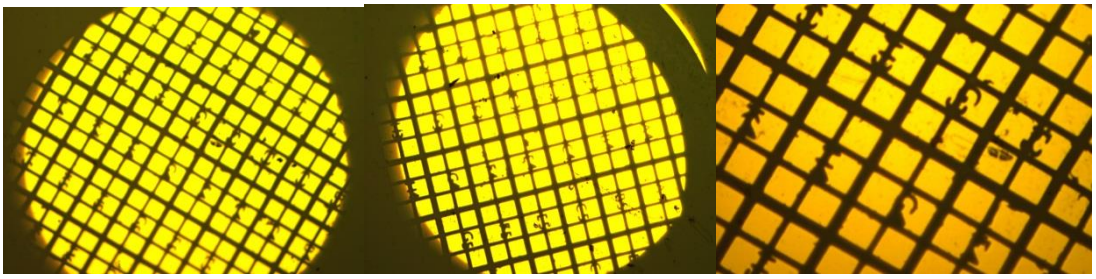
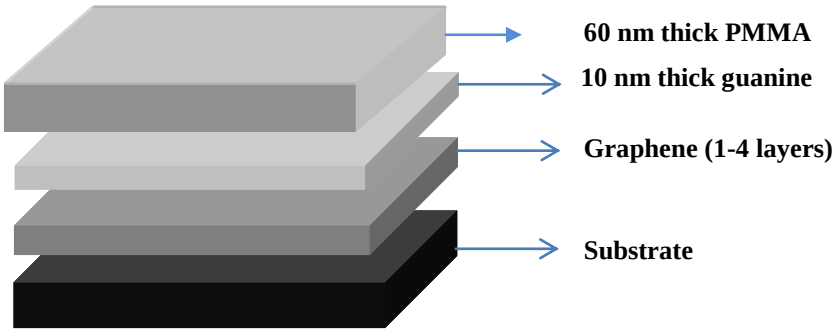


Figure 7.10. Optical microscope images of 1 μm thick/guanine/4-MLG/WG post-electrode deposition.
A successful electrode deposition with guanine as the gate dielectric layer.

7.3.2 Test Platform B

Test platform B (see Fig. 7.2):



Optical microscope images and I-V measurements of 60 nm guanine/4-MLG/WG and 300 nm guanine/4-MLG/WG could not be taken due to the high leakage current (Fig.7.11).

7.3.3 Current-Voltage Characteristics

In Fig. 7.12, I-V measurements for test platform A (1 μm guanine/4-MLG/WG) and test platform B (60 nm PMMA/10 nm guanine/4-MLG/WG) were performed to measure leakage currents under typical DC voltage used for gating OFETs. In this configuration, graphene was used as the bottom electrode and Au as the top electrode.

Degradation studies were undertaken to determine graphene mobility degradation on TR tape with and without a toluene rinse. This study was completed to observe any changes in graphene's electrical properties between each transferred graphene layer.

Studies on graphene *only* transferred the same day and 5 days after graphene was transferred onto TR tape were performed to determine if graphene degrades on TR tape (if not transferred immediately). The same batch of graphene in Tabs. 7.6 and 7.7 were used, respectively. One sample of 4-MLG/WG received a toluene rinse between each consecutive transferred graphene layer while the other sample did not. Measurements were at RT in air up to 5 days. These data are listed in Tab. 7.6. Average measurement values of PMMA/guanine/4-MLG/WG test platform B were graphed in Fig. 7.6 to observe the change in bulk mobility over a period of 5 days at room temperature in air.

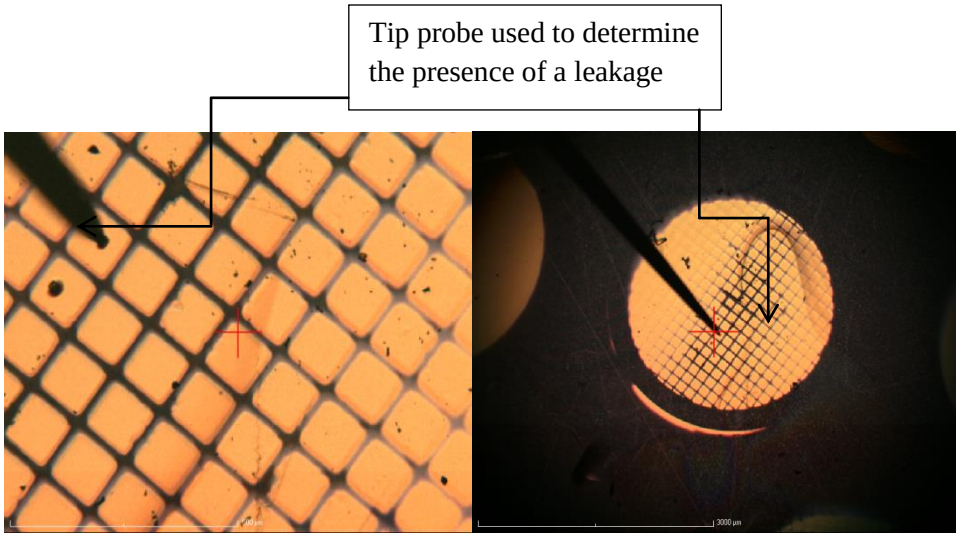


Figure 7.11. Optical microscope images of 60 nm thick PMMA/10 nm thick guanine/4-MLG/WG after electrode deposition.
Successful deposition of PMMA gate dielectric layer and guanine as the passivation layer.

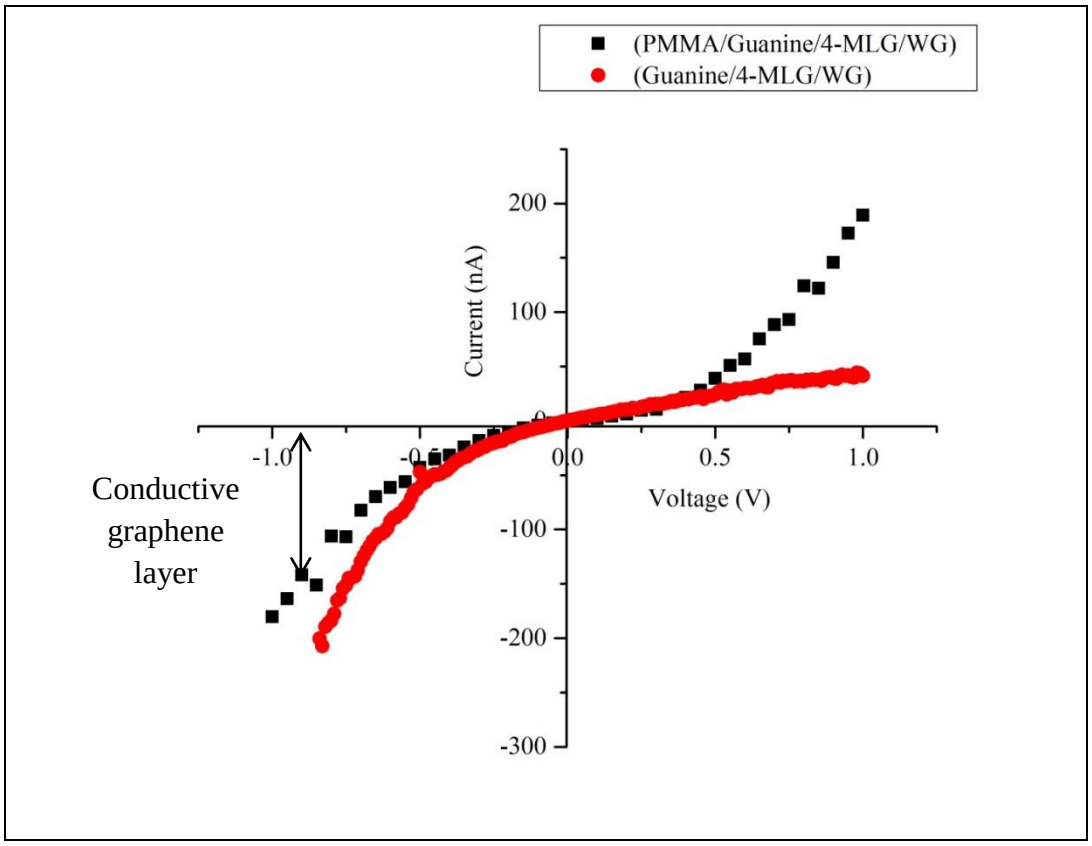


Figure 7.12. I-V curves for guanine as a gate dielectric material vs. guanine as a passivation layer.
The PMMA/guanine/4-MLG/WG (black line) appeared to be less conductive than the guanine/4-MLG/WG (red line).

7.4 Degradation Studies on Comparison of 4-MLG/WG Toluene Rinse vs. No Toluene Rinse

Table 7.6. Comparison of 4-MLG/WG toluene rinse vs. no toluene rinse.

Willow Glass Substrate	Charge Carrier Mobility (cm^2/Vs)	Charge Carrier Concentration ($10^{13}cm^{-2}$)	Resistivity (Ω/sq)
4-MLG/WG Toluene Rinse	812±41	2.29	335
4-MLG/WG No Toluene Rinse	677±34	2.62	351

Tab. 7.6 indicated that 4-MLG/WG with a toluene rinse had a higher bulk charge carrier mobility than 4-MLG/WG with no toluene rinse in between each transferred graphene layer. This study proved that the toluene rinse between each graphene layer does remove the residual material from the TR tape during the transfer process. Furthermore, ambient condition degradation studies of 4-MLG/WG with a toluene rinse and 4-MLG/WG with no toluene rinse were performed 5 days after graphene transfer (using the same batch of graphene used in Tab. 7.7). These results shown in Tab. 7.7 proved that graphene does degrade on TR tape at room temperature in air up to 6 days.

Table 7.7. Degradation study at RT in air after 5 days.

Willow Glass Substrate	Charge Carrier Mobility (cm^2/Vs)	Charge Carrier Concentration ($10^{13}cm^{-2}$)	Resistivity (Ω/sq)
4-MLG/WG Toluene Rinse	7.3±0.4	4.6	27644
4-MLG/WG No Toluene Rinse	34±1.7	2.60	7017

Four monolayers of graphene were transferred onto Willow glass. Polymethylmethacrylate and guanine were transferred onto 4-MLG/WG and graphene bulk mobilities were compared. This study examined the stability of PMMA/4-MLG and guanine/4-MLG at room temperature in air (Fig.7.13). After deposition of PMMA onto 4-MLG decreased graphene bulk mobility 29.2% and 15.6%. Guanine depostion onto 4-MLG decreased graphene bulk mobility 2.55% and 0.75%. These results indicated in Tab. 7.8 suggests that guanine layer maintained the graphene layers bulk mobilities.

Charge carrier mobilities were studied of test platform B-60 nm PMMA/10 nm guanine/4-MLG/WG to determine if this test platform was stable at room temperature in air for up to 5 days. The "control" mobility of this batch had a charge carrier mobility of 812 cm^2/Vs. All three samples were derived from the same batch of graphene. Results are listed in Tab. 7.8 and Fig. 7.14.

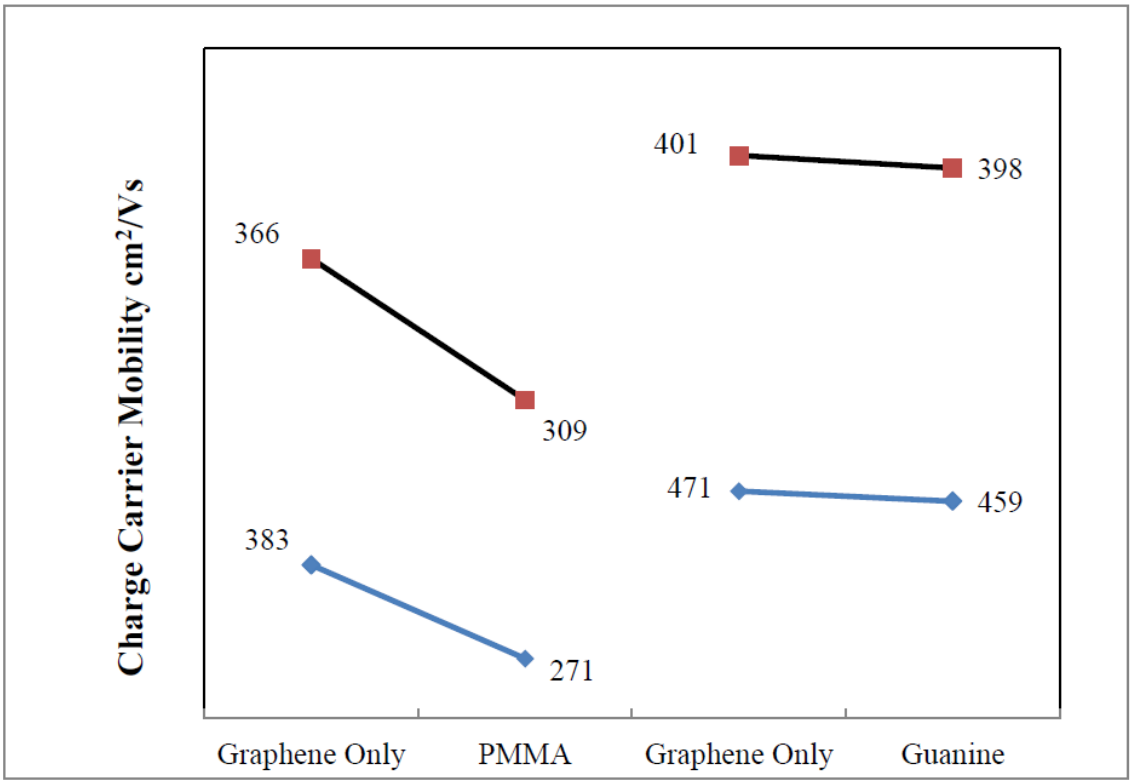


Figure 7.13. Electrical characterization of graphene only and with PMMA on graphene vs. graphene only and with guanine on graphene.
PMMA decreased whereas guanine maintained graphene bulk mobility.

Table 7.8. Electrical characterization of test platform B-60 nm PMMA/10 nm guanine/4-MLG/WG.

Sample	Charge Carrier Mobility (cm^2/Vs)			Charge Carrier Concentration ($10^{13}cm^{-2}$)	Resistivity (Ω/sq)
	0^{th} Day	2^{nd} Day	5^{th} Day		
PMMA/guanine/4-MLG/WG (Sample 1)	857±42	847±42	858±43	3.12	704
PMMA/guanine/4-MLG/WG (Sample 2)	706±35	697±35	719±36	3.51	251
PMMA/guanine/4-MLG/WG (Sample 3)	548±27	590±30	582±29	4.06	268

In test platform A and B, the electrical properties of graphene remained constant over a period of 5 days as seen previously in non-flexible (SiC) and flexible (WG) substrates with guanine *standalone*. In particular, in test platform B, electrical properties (i.e., bulk charge carrier mobility, resisitivity, and charge carrier concentration) remained constant as well. In test platform A, however, there was a greater decrease in graphene's electrical properties. It may be assumed that in test platform B, guanine acts as the passivation layer while PMMA is the dielectric material. This finding concurs with the findings of test platform B, where from I-V curve measurement the graphene is seen as a less conductive layer in comparison to the guanine *standalone* gate dielectric layer in test platform A.

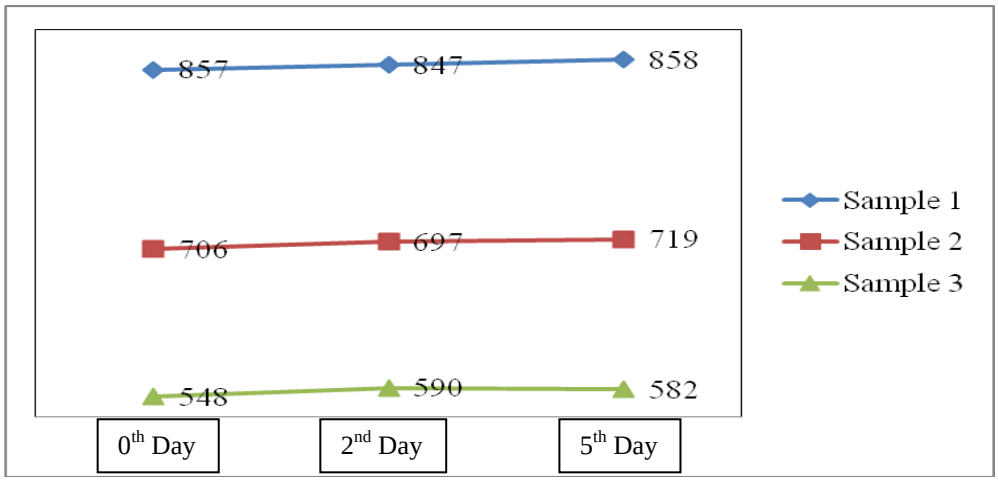
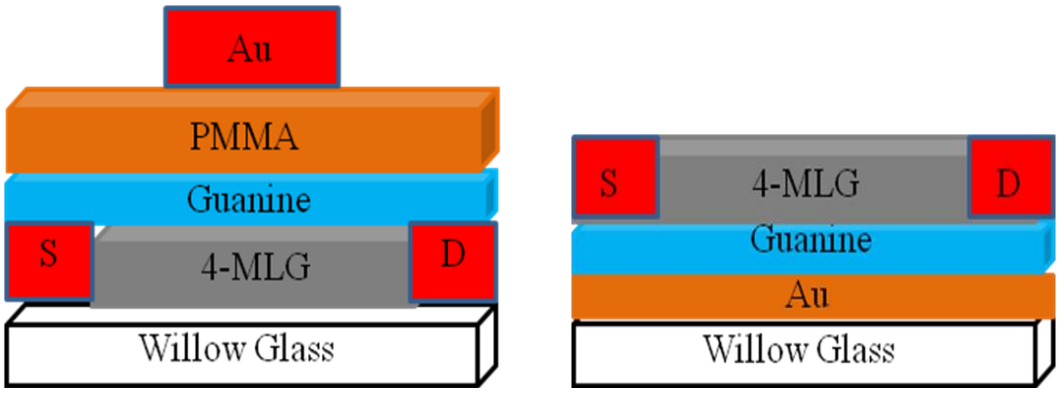


Figure. 7.14. Bulk charge carrier mobility for up to 5 days at RT in air of test platform B-60 nm PMMA/10 nm guanine/4-MLG/WG.
Plotted test platform with PMMA as the dielectric layer and guanine as the passivation layer maintains graphene bulk mobility over a period of 6 days at room temperature in air.

VIII. SUGGESTED CONFIGURATION OF METAL-INSULATOR SEMICONDUCTOR (MIS-FET)

In Fig. 8.1, PMMA is the dielectric layer and guanine is the passivation layer. 50 nm of Au would be needed to be E-beam deposited onto a GFET as the source and drain electrodes. This feature allows for deposition of a high volume of devices onto the GFET. One and 4-MLG would be needed to be deposited and I-V curve measurements for comparison have to be done. The suggested configuration of the devices are presented in Fig.8.1 a and b.



a) **b)**

Figure 8.1. Field effect transistor with a) PMMA as gate dielectric layer and guanine as the passivation layer and b) guanine as gate dielectric layer.

IX. SUMMARY

The goal of this research was to maintain the charge carrier mobility of graphene after deposition of the gate dielectric. It was achieved by use of a thin layer of guanine as a passivation layer between the graphene and gate dielectric. Bulk mobilities were maintained at RT in air up to 5 days. The I-V curves with guanine as the passivation layer had the lowest leakage current at high voltage and prevented shorting through the PMMA. The good performance of guanine as the passivation layer was achieved for thickness ~ 10 nm. As a consequence, PMMA films as thin as 60 nm could potentially be used as an organic gate dielectric in low-voltage (low-power) GFETs.

The transfer process produced impurities (defects) in the graphene structure transferred onto TR tape and then onto rigid and flexible substrates, respectively. Ironically, this did not alter nor decrease the electrical properties of the graphene at room temperature in air over a period of several days.

DNA was complexed with CTMA in water to be MAPLE-deposited as a dielectric material onto epitaxially grown graphene on SiC. These bulk charge carrier mobility were inconsistent and irreproducible. It appeared that the MAPLE-deposition technique increased chances of contamination of DNA-CTMA due to it being a solvent-based process: 70:30 T:D and produced non-uniform thin film < 250 nm in thickness. An alternative route in the use of organic materials as gate dielectrics was studied. DNA-nucleobase guanine was investigated due to its similarity in structural properties to that of DNA: high dielectric constant and high thermal stability with low molecular weight.

One, two, four, and ten layers of graphene were transferred onto rigid and flexible substrates to determine the optimum layers to be used in graphene-based test platforms. Four monolayers of graphene were chosen as the most suitable graphene layers due to the reproducibility and consistency in electrical properties. SiC, in particular, its Si-face was the optimum choice of rigid substrate not only due to the lattice matched to the graphene structure, but as well as consistent and reproducible charge carrier mobility of the graphene *standalone*. Electrical properties such as charge carrier mobility, resistivity, and charge carrier concentration were determined for these samples after several days at room temperature in air.

Willow glass was the flexible substrate chosen in this study due to its flexibility, low cost, and reproducible, consistent electrical properties at room temperature in air. These samples were all p type due to the transfer process as mentioned earlier with the rigid substrate Si-face (SiC). As seen in Si-face, these p type samples of 4-MLG/WG did not alter nor decrease the electrical properties of the graphene layers.

Graphene mobility did fluctuate but were on the same order of magnitude for both rigid and flexible substrates alike suggesting several possibilities: 1) each consecutive graphene layer may have impurities at the interfaces, 2) the transfer process was performed in a clean room at room temperature in air which contained impurities such as nitrogen and oxygen that could have affected graphene mobility, 3) one layer of graphene may have not been successfully deposited between each transferred graphene layer, and 4) the force applied to each graphene layer during the transfer process may differ between each consecutive transferred layer that may have caused variations in mobility. It is

suggested that the graphene transfer process be conducted in a glove box to minimize impurities and also measure the force applied to each graphene layer.

Guanine thicknesses used in these test platforms of 60 nm, 1 μm, and 2 μm were analyzed. It is observed that dielectric thickness layer of 60 nm allows measurement of the leakage current. 1 and 2 μm thick guanine layers were too thick to perform these measurements. Two test platforms were constructed and compared: 1) test platform A - 1 μm guanine/4-MLG/WG and 2) test platform B - 60 nm PMMA/10 nm guanine/4-MLG/WG in which PMMA is the dielectric layer. In test platform A, guanine was the gate dielectric material.

The graphene in this platform appeared to show no band gap from the I-V measurements. In test platform B, guanine was the passivation layer. Guanine appeared to passivate and/or create an hermetic seal on top of the 4-MLG. Specifically, in test platform B, graphene's electrical properties were consistent and reproducible at room temperature in air over several days when compared to test platform A. In test platform A, guanine was the *standalone* gate dielectric layer with a higher decrease in graphene electrical properties. These findings agree with I-V measurements (Fig. 7.12) that test platform B, where guanine was the passivation layer, allowed for the graphene layer to be less conductive. Guanine's electrical resistivity is unknown. Due to the fact that guanine can only be deposited at less than 1 μm thick, the electrical resistivity of guanine has not been directly measured. However, DNA is made up of various nucleobases. In turn, this infers that the electrical resistivity of guanine as well as the other nucleobases, can be no higher than DNA-CTMA with an electrical resistivity of ~ $2x10^{14}$ Ω-cm (Yaney et al. 2014) Therefore, it is fair to imply that the electrical resistivity of guanine is at least ten

times lower than PMMA with a resistivity of ~ $2x10^{13}$ Ω-cm. This is a reason why PMMA as the gate dielectric layer and guanine as the passivation layer (test platform B) is the best suited to build a device. This has potential for significant improvement of the GFET performance starting with high bulk charge carrier mobility of the gate dielectric which has to be deposited prior to device fabrication. The use of a thin film of guanine between the gate dielectric and graphene, has led to the first proof-of-concept demonstration of its highly efficient passivation effect on the graphene leading to its stable static intrinsic electronic behavior (no drop in the charge carrier mobility). The presence of guanine between PMMA and the graphene significantly enhanced the dielectric effect of the gate by allowing relatively thin films of PMMA to be used. This opens up the door for use of many other gate dielectric materials that can potentially fully optimize GFET performance, as well as for other semiconductor devices where drops in charge carrier mobility are reported after deposition of the gate dielectric. Using PMMA as a gate dielectric, without the guanine passivation layer, the charge carrier mobility of graphene decreased. With the dielectric constants of guanine and PMMA very similar, one would expect similar behavior, with a decrease in the charge carrier mobility like PMMA. However, use of guanine, as either the gate dielectric layer or a passivation layer between the PMMA gate dielectric and graphene, resulted in maintaining the charge carrier mobility of graphene. No decrease in mobility was recorded. A possible explanation for why the guanine is maintaining the mobility of the graphene could be that it is acting to minimize the impact of the impurities present at the surface of the graphene, thus decreasing the Coulomb interactions at the surface between the impurities and

carriers. This possible decrease in Coulomb interactions could then conceivably result, at least, in maintaining the mobility of the graphene layer.

In the future work, it will be useful to incorporate other nucleobases and organic gate dielectrics to determine if further improvements can be achieved in device performance. In addition, an interfacial technique such as near-edge X-ray absorption fluorescence spectroscopy (NEXAFS) can be used to determine the type of bonds that occur between the graphene/passivation/gate dielectric layers and how this may be used to improve the device performance.

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