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High Frequency VCO and Frequency Divider in VLSI 90nm Technology

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High-Frequency VCO and Frequency Divider in 90-nm Technology

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Engineering

by

Paesol Veerakitti
B.S.E.E., Wright State University 2008

2010
Wright State University
WRIGHT STATE UNIVERSITY
SCHOOL OF GRADUATE STUDIES

June 15, 2010

I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Paesol Veerakitti ENTITLED High-Frequency VCO and Frequency Divider in 90-nm Technology BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENT FOR THE DEGREE OF Master of Science in Engineering

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ABSTRACT

Paesol, Veerakitti M.S.Egr., Department of Electrical Engineering, Wright State University, 2010. High Frequency VCO and Frequency Divider in 90nm Technology.

A Voltage Controlled Oscillator (VCO) is essentially a tunable frequency generator. A VCO is used as a part in PLL system which is a system that generates a stable oscillating signal. As the digital electronic industry demands an ever increasing performance in speed, VCO’s are required to create higher frequency signals. However, the phase noise performance of a VCO decreases as the operating frequency gets higher. A ring VCO structure and an LC tank VCO structure are analyzed. The LC VCO is developed in this thesis to be used in with a tunable frequency divider as a part of a PLL system. The LC VCO structure design takes the advantage of a current source in the LC tank to provide an operational condition while lowering the overall tank size for a higher oscillation. The variable frequency divider structure uses the low voltage swing current mode and two CML latch configurations. The dividing constant of the frequency divider is varied by adjusting the load resistance of the CML latches. The resulting combined circuit structure yields a maximum operating frequency of 43.23GHz with the divided frequency of 296MHz. The phase noise of the VCO at maximum operating frequency is -80dBc/Hz at 1MHz offset.
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DEDICATED TO YAOWAMALN and PAEMISA
1 Introduction

1.1 Overview

The speed of operation in digital electronics industry, in both military and commercial products is ever increasing. Pulse generators are the heartbeat of all digital communications and digital logic. The frequency of the pulse generator determines the speed of which the digital circuitry operates. The higher the frequency, the faster the digital circuitry can operate. The phase noise of a pulse generator will determine the reliability of the operation of the circuit. A system called Phase Lock Loop (PLL) helps improve the phase noise by comparing the phase of the pulse generated by the VCO with a stable referencing, more stable phase, with the difference filtered and fed back to the input of the VCO [1]. There are four major modules for a PLL system; a phase frequency detector (PFD), a loop filter, a voltage controlled oscillator (VCO), and a frequency divider. Figure 1.1.1 illustrates the block diagram of a typical PLL system. The VCO generates the oscillation, which then reduces the frequency into a new, lower frequency by the divider. The phase of the divided frequency is then sensed by the PFD where it is compared to a referencing phase. The loop filter then filters out other carrier frequency components and harmonics, then produces a control voltage that is being fed back to the VCO to regulate the output frequency.
The heart of a PLL system is its VCO. The VCO not only determines the operating frequency, but also its reliability and performance. The frequency divider together with the oscillator is the most difficult blocks to implement in the PLL system due to its high operating frequency. This thesis focuses on developing an LC tank VCO structure in conjunction with a frequency divider to produce the highest possible oscillation, and lowest possible phase noise in order to be used in a PLL system.

1.2 Basics

This chapter discusses the theories and basic operation of the structure of a Voltage Controlled Oscillator (VCO) and frequency divider used in PLL systems. The goal of this research is to develop and improve VCO and adjustable frequency divider structures to be used in a phase lock loop high frequency synthesizer.
1.2.1 Ring VCO

In today’s industry, ring VCO structure is preferred in more cost effective applications due to its simplicity and low cost of construction. The ring oscillator is popular in the use of generating an on-chip signal and it is also often used as a test structure for the fabrication process evaluation [1]. A basic ring oscillator structure is a cascade of an odd number of CMOS inverters, with the output of the last inverter connected to the input of the first inverter [1]. The operation of ring oscillators depends on the gate delay of the CMOS inverters. Gate delay of CMOS inverters is the time it takes to charge and discharge the capacitance of the MOSFETs due to its physical properties. When placing an odd number of inverter circuits, the gate delay of each inverter adds up to a total delay of which the reciprocal is the operating frequency of the oscillator. More details on the principal of operation of the ring VCO is discussed in chapter 2.
1.2.2 LC Tank VCO

The LC tank VCO structure is popular in applications that require low phase noise such as in high speed microprocessors which rely on precise arrival time of a clock signal. The main determining factor of the output frequency of the LC VCO is the size of its LC tank. Comparing the oscillation of the LC tank to a marble in a bowl, the smaller the bowl, the faster the marble will roll back and forth in the bowl, where the period is the time it takes to complete one cycle. For the LC tank, the smaller the inductance and capacitance, the less time it takes for the electrical energy to transfer from magnetic energy (in the inductor coil), to electro-potential energy (in the capacitor plates). Thus, the smaller the LC tank, the faster the output frequency will be. The LC tank voltage controlled oscillator can be compared to a tank containing a certain amount of energy that powers the oscillation. The word “tank” refers to the combination of capacitors and inductors that store the electrical potential energy in the oscillator circuit. In an ideal situation, there is no “leak in the tank” where the capacitors and inductors have no impedance and no energy loss during oscillation. This is not likely in a real world situation, since real capacitors and inductors have impedances in reaction to frequencies. The governing relationship of the LC tank oscillation is observed to be

\[ f = \frac{1}{2\pi \sqrt{LC}} \]  

(1.2.2.1)
Equation 1.2.2.1 explains the relationship of oscillation frequency \( f \) as a function of inductance \( L \) and capacitance \( C \). In the real world situation, inductors and capacitors have impedance as a function of frequency. For inductors;

\[
Z_L = 2\pi f L
\]  
\[1.2.2.2\]

And for capacitors;

\[
Z_C = \frac{1}{2\pi f C}
\]  
\[1.2.2.3\]

In order to counter the impedances of the inductors and capacitors, a form of negative resistance is required. Figure 1.2.2.1 illustrates the LC tank with negative resistance.

**Fig 1.2.2.1 LC tank with negative resistance**

The negative resistance can be a form of an amplifier using CMOS transistors.
1.2.3 Frequency Divider

The performance and functionality of a frequency divider is a vital attribute to the overall performance of PLL systems. The noise produced from the frequency divider will be added to the overall noise of the PLL system. Most of the frequency divider structures are comprised of logic gates and flip-flops. Frequency dividers that operate in a high frequency range are categorized in two groups: fixed-N or tunable [8]. A fixed-N frequency divider is simply defined by the divider having a fixed dividing constant (i.e. divided by 4 frequency divider). One example of a basic fixed-N frequency divider is a half divider (N=2). The principal of a half-frequency divider relies on a D-flip flop circuitry, or also known as delay flip-flop [5].

![Fig 1.2.3.1 D-Flip-Flop](image)

When the clock input of the D-flip flop sees a positive edge trigger, the output Q becomes the state of the input D [5] as illustrated in Figure 1.2.3.1 and Figure 1.2.3.2.
When biasing the output Q’ to D, the D-flip flop behaves as a half divider for the incoming clock signal as shown in Figure 1.2.3.3.

As we can see that for a relatively lower frequency PLL such as 200MHz, a half frequency divider circuit is sufficient to sync the phase of the output frequency to a
crystal oscillator, which operates in the Mega Hertz range [7]. However, for a much higher frequency signal, in order to carry out the same objective, many half-divider circuits would be required. There are many different types of frequency dividers used in a PLL system in today’s industry. These types of frequency divider are categorized by either synchronous or asynchronous frequency dividers [8]. Synchronous frequency dividers operate by input signal triggering each of the flip-flops individually. Asynchronous dividers however, use the output signal of the previous flip-flop to trigger the next, like the domino effect. An example of a three-stage asynchronous divider is illustrated in Figure 1.2.3.4. Each D-flip flop divides the incoming frequency by half, and then passes on the divided signal to the next flip-flop stage, thus causing the final signal to be asynchronous with respect with the input signal.

![Fig 1.2.3.4 three-stage asynchronous frequency divider [8]](image)

Figure 1.2.3.5 is an example of a synchronous frequency divider using JK-flip flop. The final divided frequency signal can be synchronized with the clock signal by
combining the outputs of each flip flop with an AND gate.

![Three stage synchronous frequency divider](image)

**Fig 1.2.3.5 Three stage synchronous frequency divider [8]**

This structure however will accumulate the jitter of each stage of the flip flop. One way to reduce the jitter produced by this strategy is to place a synchronization flip-flop at the end of the chain, thus, only the synchronizer will be the only source of jitter [8]. As we can see from examples provided, fixed-N frequency dividers are simple and effective to implement in a PLL system. However, fixed-N frequency dividers have its limitations for many applications that would require the implementation of a channel selector.
1.2.4 Tunable Frequency Divider

There are many different types of tunable frequency dividers. The most commonly used structure today is called pulse-swallow frequency divider configuration. Pulse-swallow offers more flexibility in dealing with multiple channel widths [8]. This configuration however, involves complex circuitry. This complex circuitry has three modules in itself. These modules are called pre-scaler, program counter, and swallow counter modules. The alternative to this structure, as proposed in this thesis, is called adjustable CML master-slave latch. This proposed circuit is based upon current mode logic (CML) structure as a master-slave latch divider. The main operating principle is similar to a Johnson counter, which is a divide-by-two high-frequency divider structure.

Fig 1.2.4.1 Johnson counter as divide-by-two block diagram [8]
1.3 Thesis Organization

Chapter 2 covers the operation of an inverter ring VCO structure and its performance. Chapter 3 entails the design aspects, the principal of operation, and the performance analysis of an LC tank VCO structure. Chapter 4 describes the structure of a current mode logic frequency divider circuit and its modification as a variable frequency divider. Chapter 4 also entails the performance analysis of the variable frequency divider. Chapter 5 discusses the performance of the LC VCO and the variable frequency divider circuit combination. Chapter 6 is the conclusion of the findings and analysis of the circuit simulation results. Chapter 6 also discusses the future work of the research.
2.1 Design Aspects

Operating frequency of an inverter ring VCO is the reciprocal of the total delay of the circuit. The total delay of an inverter ring VCO is the sum of each individual inverter. The inverter delay is caused by the charge time of the capacitances of the transistors. Equation 2.1.1 can be used to estimate the inverter delay $\tau$ as a function of equivalent resistance $R_{eq}$ of the inverter, and the loading capacitance $C_L$ seen by the inverter.

$$\tau = R_{eq}C_L \quad (2.1.1)$$

Figure 2.1.1 illustrates the equivalent loading capacitance of an inverter in a ring oscillator.
The total loading capacitance \( C_L \) referencing from the output of an inverter is the sum of the drain to bulk capacitance \( C_{db} \), and the gate to source capacitance \( C_{gs} \) of the transistors.

\[
C_L = C_{db} + C_{gs}
\]  

(2.1.2)

2.2 Ring VCO Design

Referring to equation 2.1.1, the delay of the inverter is a function of \( R_{eq} \) and \( C_L \). The operating frequency of the inverter ring VCO can be varied by adjusting either \( R_{eq} \) or \( C_L \). The capacitance \( C_L \) can be varied by adjusting the width of PMOS and NMOS transistors, which cannot be done in real time. The equivalent resistance \( R_{eq} \) of the inverter, however, can be varied by controlling the current that passes through the inverter. The transistors in an inverter circuit operate in the linear region, which the drain current that passes through can be characterized by equation 2.2.1 [16].

\[
I_D = \frac{\mu n C_{ox} W}{L} \left( (V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2} \right)
\]  

(2.2.1)

The resistance of the transistor is inversely proportional to the drain current; therefore, the equivalent resistance of the inverter can be approximated by equation 2.2.2 [16].

\[
R_{eq} \approx \frac{1}{\mu C_{ox}} \frac{L}{W} \frac{1}{(V_{GS} - V_{th})}
\]  

(2.2.2)
The equivalent resistance is essentially the reciprocal of the drain current equation in the linear region of the transistor. From equation 2.2.2, the only variable that can be varied in real time is the gate to source voltage $V_{GS}$ of the transistor. Therefore, equivalent resistance can strictly be a function of $V_{GS}$.

![Inverter circuit with biasing NMOS transistor](image1)

**Fig 2.2.1** inverter circuit with biasing NMOS transistor

![Inverter circuit symbol](image2)

**Fig 2.2.2** symbol of inverter circuit with biasing NMOS

From Figure 2.2.1, the equivalent resistance of the inverter circuit can be controlled by adding an NMOS transistor. This makes $V_{GS}$ becomes $V_{bias}$ in equation 2.2.2.
Therefore, the current that passes through each inverter stage can be adjusted by $V_{bias}$. Figure 2.2.3 is the inverter ring VCO circuit utilizing this concept.

**Fig 2.2.3 five-stage mixed ring VCO**

The transistors T9, T0, T1, T2, and T3 function as current mirror. They make the current for each stage of the inverters to be in equal amounts as the tuning voltage varies. The time response of the ring VCO circuit is shown in Figure 2.2.4.
Fig 2.2.4 inverter ring VCO transient response

As we can see from time response, the oscillation doesn’t start until after 3ns. The circuit produces an oscillation of 5GHz at the tuning voltage of 1.2V. Figure 2.2.5 is the time domain response of the ring VCO at maximum operating frequency.
The maximum operating frequency of the ring VCO circuit is 12.5GHz at the tuning voltage of 0V. Table 2.2.1 summarizes the Ring VCO performance.

<table>
<thead>
<tr>
<th>Tuning Voltage (V)</th>
<th>Output Frequency (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>12.5</td>
</tr>
<tr>
<td>0.2</td>
<td>9.80</td>
</tr>
<tr>
<td>0.4</td>
<td>9.02</td>
</tr>
<tr>
<td>0.6</td>
<td>7.92</td>
</tr>
<tr>
<td>0.8</td>
<td>7.32</td>
</tr>
<tr>
<td>1</td>
<td>5.95</td>
</tr>
<tr>
<td>1.2</td>
<td>5.00</td>
</tr>
</tbody>
</table>

Table 2.2.1 Ring VCO output frequency and tuning voltage
Graph in Figure 2.2.6 illustrates the tuning curve of the Ring VCO.

![Graph](image)

**Fig 2.2.6 inverter ring VCO output frequency versus tuning voltage**

The output frequency of the ring VCO ranges from 5GHz to 12.5GHz, which is 7.5GHz of tuning range. The phase noise of the circuit is at -82dBc/Hz at 1MHz offset with 12GHz center frequency. The phase noise simulation result of the circuit is shown in Figure 2.2.7. The power consumption of the ring VCO circuit is at 3.12mW at 12.5GHz.
The simulation results indicate that the ring VCO yields relatively good tuning range, and considerably good power consumption. However, the output frequency and tuning range of the inverter ring VCO can still be improved by optimizing the transistor sizes. The LC tank VCO is preferred VCO structure in higher range operating frequency (above 20GHz).

**Fig 2.2.7 phase noise measurement of the inverter ring VCO**
3.1 Design Aspects

3.1.1 Oscillation

As mentioned earlier, for the oscillation to occur in an LC circuit, there must be an exchange of energy between a capacitor and an inductor. A compensation for the loss of energy is also necessary. Referring to Figure 1.2.1 and from Kirchhoff’s voltage and current law, we can derive the relationship:

\[ \frac{d^2 i(t)}{dt^2} + \frac{1}{LC} i(t) = 0, \tag{3.1.1.1} \]

Which is the second order differential equation describing the current in the LC tank as a function of time. Where \( i(t) \) represents an electrical current as a function of time measured in Amps, \( L \) stands for inductance measured in Henry, and \( C \) represents capacitance measured in Farad. From equation 1.2.2.1, we can derive the equation for LC tank frequency \( \omega_o \) to be:

\[ \omega_o = \frac{1}{\sqrt{LC}} \sqrt{1 - \frac{R^2C}{L}} \tag{3.1.1.2} \]
where \( R \) is the resistance of the circuit. The lower limit of the transconductance \( g_m \) of each MOSFETs must be:

\[
g_m \geq \frac{RC}{L}
\]  

(3.1.3)

The coefficient \( g_m \) is the measurement of how much the drain current changes with an incremental change of the voltage between the gate and source terminal of the MOSFET. \( g_m \) is determined by the size of the MOSFET due to its internal capacitances. Equation 3.1.4 illustrates the relationship of the transconductance.

\[
g_m = \frac{dI_D}{dV_{GS}}
\]  

(3.1.4)

\( I_D \) is the drain current, and \( V_{GS} \) is the gate voltage.

### 3.1.2 Waveform and Duty Cycle

The purpose of designing a good LC VCO is mainly to satisfy the need for a reliable and efficient clock signal. This also applies for function generators, or for any digital logic or wireless communication applications. Therefore, a time-domain analysis is broken into three sub categories. These sub categories are output frequency, duty cycle, and the shape of the waveform. The output frequency of the design will
determine whether the circuit can be utilized according to the application of the LC VCO. The duty cycle of the output waveform is important to be considered, since the falling or rising edge of the signal will be the trigger for most digital logic applications (i.e. D-Flip-Flops). It will also be important in most analog applications because the duty cycle of the clock signal will determine an ON or OFF time of the transistor. The desired duty cycle is to be as close to 50% as possible. The shape of the output waveform is important for analog applications, since bizarre waveforms can cause errors and misbehavior of the active components such as capacitors or transistors. Bizarre waveforms will also cause noise in analog circuits, and some possible errors in digital computations. For above reasons, the waveform analysis is very important to consider in designing a voltage-controlled oscillator.

3.1.3 Phase Noise

According to Gardner, in Phase lock Techniques [7], the phase noise of an oscillation can be characterized by a mathematical model. Consider a typical oscillator, where \( v_o(t) \) is the output voltage, and \( f_o \) is the oscillation frequency:

\[
v_o(t) = [A + a(t)]\cos[2\pi f_o t + \Phi(t)]. \tag{3.1.3.1}
\]

Where \( a(t) \) is the zero-mean amplitude noise, and \( \Phi(t) \) contains all of the phase and frequency that departure from the nominal oscillation frequency \( f_o \) and phase of
2\pi f_0 t. A is the mean amplitude of the oscillator output. Phase disturbance \( \Phi(t) \) includes random zero-mean phase noise, initial phase, and integrated effects of frequency offset and drift. The amplitude noise \( a(t) \) is disregarded in a standard analysis of the phase noise because the effects of phase noise overshadows the effect of amplitude noise. The variance of oscillator output \( v_o(t) \) is \( A^2/2 \) since the amplitude noise is not considered [7]. Considering the complex envelope of the equation 3.1.3.1:

\[
Z_0(t) = Ar[j(2\pi f_0 t + \Phi(t))]
\]  

(3.1.3.2)

Where \( z_0(t) \) is the complex of \( v_o(t) \). The autocorrelation equation is shown in equation 3.1.3.3.

\[
E[Z_0(t_1)Z_0^*(t_2)] = A^2[j2\pi f_0(t_1 - t_2)]E[j(\Phi(t_1) - \Phi(t_12))]
\]  

(3.1.3.3)

If increment \( \Phi(t_1) - \Phi(t_2) \) of the phase \( \Phi(t) \) is stationary, the process is wide-sense stationary. This means that the autocorrelation is a function of \( (t_1 - t_2) \) only. Therefore, the autocorrelation of an oscillator is non-stationary with frequency drift. Autocorrelation is the fundamental frequency in which it is buried in its harmonic frequencies. The main determining factor of the phase noise is the “Q” factor of the LC tank. The “Q” factor of the LC tank is the quality factor of which indicates how
well the energy is stored in the LC network in terms of the rate of energy loss. In an ideal situation, the “Q” factor is assumed to be very low or zero, which we know that it is not so in reality. Therefore, the main concern of the phase noise will be the “Q” factor which contributes to the $\Phi(t)$ of the equation [7].

Phase noise is measured by taking the power density in one sideband per Hz bandwidth at an offset frequency away from the carrier, divided by the Total power of the signal.

![Fig 3.1.3.1 phase noise measurement](image)

Phase noise can be obtained by equation 3.1.3.4.

$$S_c(f) = \frac{P_{\text{carrier}}}{P_{\text{sideband}}}$$  \hspace{1cm} (3.1.3.4)

$P_{\text{carrier}}$ repress the carrier power, $P_{\text{sideband}}$ represents the sideband power in one Hz
bandwidth at an offset frequency $f$. The sideband phase noise is calculated by:

$$S_c(f) = 10 \log[S_c(f)]$$

(3.1.3.5)

The unit is in dBc/Hz at a given offset frequency (i.e. -100dBc/Hz at 1MHz offset frequency).

3.1.4 Tuning Range and Linearity

Tuning range of an LC VCO is desired to be as wide and as linear as possible for the versatility of the oscillator circuit. Wide tuning range in a VCO allows the circuit to be used in many different applications. Therefore, wide tuning range could save production cost and manufacturing time since the output frequency can match the demand by simply adjusting the tuning voltage. The output frequency of an LC VCO can be altered by either its inductance, or its capacitance. Since the inductance of an inductor is harder to control, the capacitance of the oscillator is instead varied in order to change the output frequency. This is done by using a device called the variable capacitor (varactor). A varactor operates like a reversed biased diode where the reversed voltage determines the capacitance. However, since the tuning range of an LC VCO is determined by its capacitance of the capacitors in the LC tank, it will affect its phase noise. Linearity of tuning in an LC VCO is determined by the
physical properties of the varactor. In order to achieve a good tuning linearity in an LC VCO, a good selection of a varactor structure is crucial.
3.2 LC Oscillator Models

3.2.1 LC Oscillator Circuit

Fig 3.2.1.1 LC oscillator circuit
The circuit in Figure 3.2.1.1 was the first LC Oscillator circuit to be tested. The circuit contains four stages; LC tank with two inductors and one capacitor, a current mirror, a sense amplifier, and an inverter. The current mirror is connected to both of the source terminals of the two transistors to provide a current source for the oscillation. The sense amplifier is connected to both output terminals of the LC tank to amplify the oscillation signal from the tank. An inverter is connected to the output of the sense amplifier to bring the output signal to be the full swing range from ground to $V_{dd}$. The circuit produces an operating frequency of 200MHz (period of 5ns) using an ideal capacitor and inductor model with capacitance of 1pf, and inductance of 100nH. The circuit was then tested with different values of capacitance and inductance to vary the output frequency. To test the steady state response of the oscillation, a relatively long simulation of over 125ns was conducted. The result is illustrated in Figure 3.2.1.2. The amplitude of the oscillation does not decay nor intensify indicating that the output response is stable.
3.2.2 LC Voltage Controlled Oscillator Circuit

The tuning voltage controls the capacitance of the varactor in order to vary the output frequency. The circuit shown in Figure 3.2.2.1 is an improvement of the LC Oscillator Circuit in the previous section. It uses an inverter circuit as an amplifier for the output voltage. This is possible due to an appropriate ratio between the NMOS and PMOS transistor width of the inverter circuit. This circuit has the ratio between PMOS and NMOS (P/N) of 50. The LC network of the circuit determines the operating output frequency. The amplitude and the waveform of the oscillation are
determined by the ratio of PMOS and NMOS transistor size of the inverter at the output of the LC tank. The circuit shown in Figure 3.2.2.1 produces a frequency ranging from 12GHz to 23.1GHz.

![Fig 3.2.2.1 LC Voltage Controlled Oscillator Circuit](image)

3.2.3 LC Voltage Controlled Oscillator Circuit Output

As illustrated in Figure 3.2.2.2, the shape of the waveform of the output oscillation at frequency of 12GHz appears to be lopsided. This is because the inverter PMOS transistor size is too large compared to the NMOS. After testing and fine-tuning the LC VCO circuit, a PMOS to NMOS ratio of 8 to 1 appears to give the best response for
the oscillating frequency of 12GHz as shown in Figure 3.2.2.3. The NMOS transistors of the LC tank provide the negative resistance to compensate the loss of the LC network. The larger the tank size (i.e. larger capacitance and inductance), the larger the NMOS transistor size needs to be in order to keep the oscillating condition.

Fig 3.2.2.2 LC Voltage Controlled Oscillator Output Waveform
Thus far, ideal inductors and capacitors were used in the experiments to verify the oscillation of the LC tank in simulation software. However, real inductors and capacitors models used in CMOS technology have internal resistance as well as other physical properties that would contribute to the overall performance of the circuit. In order to fully design and simulate the LC tank VCO, a real capacitor and inductor model with all of the physical properties are necessary to be used in the simulation.
The inductor model used in the simulation contains wire length, width, number of coil turns, and the permittivity of the material. The capacitor model used in the simulation contains the plate geometry, dimension, the distance between the plates, and the permittivity of the material. This is extremely important to the design methodology because the response of the circuit can be entirely different when manufactured if the design uses ideal component models. For the case of LC VCO circuit in Figure 3.2.2.1, the oscillation of the circuit will not occur unless the transistor size of the NMOS transistor that is providing the negative resistance is large enough. Also, designing the LC VCO circuit with real component models adds quite a few extra variables in the design, as well as some limitation. One limitation is that the structure types of varactor and inductor models in a 90nm technology are pre-design for fabrication process by the foundry. Therefore, there are limited options for the types of varactor and inductor models that can be selected for the use of the LC VCO design. For example, there are PCAP and NCAP varactors, as well as symmetrical and asymmetrical inductors that can be used for the design of the LC network. PCAP refers to PFET in p-well variable capacitor. NCAP refers to NFET in the n-well variable capacitor. The details on the two components will be discussed in the next section. In order to find the best possible varactor and inductor model to be used in an LC VCO, many experiments as well as many modifications must to be conducted.
3.3.1 PCAP and NCAP Varactors in VLSI process

As mentioned in earlier sections, the choice between NCAP and PCAP varactors is a consideration to be used in the design of an LC VCO circuit. This section will briefly describe the structure and operating principle of PCAP and NCAP varactors. PCAP and NCAP varactors are MOS varactors. Their principal of operation relies on the parasitic capacitance in a MOS transistor. The structure of both of these types of varactor is simply a structural modification of an ordinary MOS transistor to enhance the parasitic capacitance. The voltage between the Drain/Source terminal and the gate terminal causes the change in the parasitic capacitance. The relationship in equation 3.3.1.1 represents the ratio in which the tuning range of the operating frequency can be determined by the maximum and the minimum capacitance of the varactor.

\[
\frac{f_{\text{max}}}{f_{\text{min}}} = \sqrt{\frac{C_{\text{max}}}{C_{\text{min}}}} \tag{3.3.1.1}
\]

The ratio between the maximum and minimum frequency is proportional to the square root of the ratio between the maximum and minimum capacitance of the capacitor.
Fig 3.3.1.1 Structure of a MOS varactor [11]

Keep in mind that there are many structures and designs for both PCAP and NCAP varactors. The structure selected for this study is purposed to illustrate the basic operating concept of the varactors. Figure 3.3.1.1 is an example of a generic MOS varactor.

Fig 3.3.1.2 Cross-section of P-to-N-well junction varactor [10]
The P-to-N-well junction varactor utilizes the capacitance \( C_j \) in the depletion area between the P-diffusion and the n-well. Therefore, \( C_j \) is determined by the reversed voltage between point A (Anode) and point C (Cathode). The depletion area increases as a function of the reversed voltage between A and C. Thus, the capacitance \( C_j \) decreases as the reversed voltage increases [10]. The circuit equivalent representation of the PCAP device is illustrated in Figure 3.3.1.2. The total equivalent capacitance of the PCAP is formed between point A and the ground. When there is no reversed voltage applied between point A and point C, the equivalent circuit is represented by an ideal AC short (as illustrated).

For NCAP varactors, two commonly used structures are; the standard NMOS varactor and the accumulation mode NMOS varactor. The operation of the standard mode NMOS varactor is a slight modification to the n-channel MOSFET transistor. The drain terminal and the source terminal of the NMOS varactor are shorted with the metal layer as shown in Figure 3.3.1.4.
Fig 3.3.1.4 Structure of NCAP Varactor Standard Mode

The change from depletion to inversion mode in an NMOS transistor causes the capacitance to change from minimum to maximum [10]. This is the principal of operation in a standard mode NMOS varactor or NCAP. A depletion area is created underneath the gate area when a small positive voltage is applied between the gate terminal and the Drain/Source terminal as shown in Figure 3.3.1.5. This depletion area formed causes a separation between the two terminals within the varactor, and then causes the change in capacitance. The same way with a normal capacitor has its capacitance determined by the separation between the two plates as equation 3.3.1.1 describes,

\[ C' = \frac{\varepsilon A}{s} \]  \hspace{1cm} (3.3.1.1)

where \( C \) is the capacitance, \( \varepsilon \) is the permittivity of the substance that separates the
two plates of the capacitor, \( A \) is the area of the plates, and \( s \) is the distance between the two plates.

![Diagram of NCAP Varactor Standard Mode](image)

**Fig 3.3.1.5 Cross-section of NCAP Varactor Standard Mode [10]**

The created depletion area highlighted in the Figure shown causes the total capacitance seen from G terminal to D/S terminal to be equal to the series connection of the oxide capacitance \( C_{ox} \) and the depletion capacitance \( C_d \). When the voltage at the gate terminal increases, the depletion area underneath the gate will grow larger and deeper into the substrate. This causes the total capacitance between G terminal and D/S terminal to increase. The maximum capacitance is reached when the voltage at the gate terminal is high enough to create an inversion layer at the silicon surface. Here, the maximum value is equal to \( C_{ox} \).
3.3.2 Using PCAP in The LC VCO Circuit

Figure 3.3.2.1 is the circuit diagram of the LC VCO using a PCAP with the gate terminal connected to the positive potential, and the tuning voltage is connected to the D/S terminal of the PCAP MOS varactor. The resulting waveform indicates that the oscillation is stable and non-decaying. In this particular circuit configuration, the dimension of the varactor used in the design yields a capacitance from 62.97 fF to 924.22 fF. The transient response in time domain of the circuit is shown in Figure 3.3.2.2 with the tuning voltage of 0.1V.
The tuning voltage ranges from 0.1 volts to 0.9 volts. The resulting oscillation ranges from 20.25GHz to 22.6GHz. This gives the tuning range of 2.35 GHz. The average power consumption of the circuit is around 49.1mW at maximum operating frequency. The resulting graph is shown in Figure 3.3.2.3 indicating a slight curve with a negative slope.
Fig 3.3.2.3 LCVCO with PCAP Tuning range

From the data gathered from the results of the PCAP LCVCO circuit, the relationship between the output frequency ($f_o$) and the tuning voltage ($V_t$) is obtained in equation 3.3.2.1 from second order polynomial interpolation.

$$f_o = -0.3776V_t^2 - 2.582V_t - 22.873 \quad (3.3.2.1)$$

A simpler line interpolation in equation 3.3.2.2 can also be obtained from the graph.

$$f_o = -2.9619V_t + 22.934 \quad (3.3.2.2)$$
3.3.3 Using NCAP in The LC VCO Circuit

The LC VCO circuit shown in Figure 3.3.3.1 uses the exact same configuration, but uses NCAP instead of PCAP. The difference between the two types of MOS varactor is its Q factor. NCAP is known to have slightly higher Q factor, thus yielding higher phase noise performance.

![Fig 3.3.3.1 LC VCO Using NCAP Circuit](image)

Similar to the PCAP version, the LC tank of this VCO is comprised of two symmetrical inductors in series with two NCAP varactors, with a tuning voltage terminal
connected to the positive side of both of the NCAP varactors’ terminals, as shown in Figure 3.3.3.1. In this particular configuration, the tuning voltage will vary the capacitance of the varactors, thus changing the size of the LC tank. Figure 3.3.3.2 shows the time domain response of the circuit.

**Fig 3.3.3.2 Time domain response of the NCAP LCVCO**

The tuning range result of the LCVCO circuit is shown in Figure 3.3.3.3.
The relationship between the output frequency \( f_0 \) and the tuning voltage \( V_t \) is obtained from equation 3.3.3.1.

\[
f_0 = -2.9959V_t + 23.233
\]  

(3.3.3.1)

The LCVCO using NCAP varactor is proved to have slightly better performance. The NCAP varactor will be used in the VCO structure. The tuning voltage, like the PCAP LCVCO, ranges from 0.1 volts to 0.9 volts. The resulting oscillation ranges from 20.55GHz to 22.95GHz. This gives the tuning range of 2.4 GHz. The average power
consumption is around 49.3mW at maximum frequency. Figure 3.3.3.4 is the phase noise measurement of the circuit, which is at -98dBc/Hz at 1MHz offset.

![Phase Noise Measurement Graph]

**Fig 3.3.3.4 Phase noise measurement of the LCVC0 output signal**

Table 3.3.3 summarizes the performance in approximate between PCAP LCVC0, and NCAP LCVC0 according to the simulation result of the circuit in 90nm Technology.
<table>
<thead>
<tr>
<th></th>
<th>Tuning range</th>
<th>Maximum Frequency</th>
<th>Power consumption</th>
<th>Phase noise at Maximum Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCAP LC VCO</td>
<td>2.35GHz</td>
<td>22.60GHz</td>
<td>49.31mW</td>
<td>-95dBc/Hz at 1MHz offset</td>
</tr>
<tr>
<td>NCAP LC VCO</td>
<td>2.4GHz</td>
<td>22.95GHz</td>
<td>49.85mW</td>
<td>-98dBc/Hz at 1MHz offset</td>
</tr>
</tbody>
</table>

Table 3.3.3 PCAP and NCAP LC VCO Performance

The frequency output however, is not yet at optimum performance at this point. The sizes of the transistors and other components of the LC VCO can still be smaller to obtain even higher frequency. The width of the NMOS transistor is at 48 µm to provide enough compensation for the loss in the LC network. At the same time, this slows down the oscillation. A solution to this problem could be introducing another NMOS transistor with a much smaller width to function as a current source to sustain the oscillation. The tradeoff of higher frequency would be lowering the phase noise as the output frequency increases, simultaneously with higher power consumption.

3.3.4 Improving the frequency output in the LC VCO Circuit

The LC VCO circuit in Figure 3.3.4.1 introduces a slightly different structure. As we can see from the circuit, the invertors on both sides of the outputs are removed and replaced by NMOS transistors, thus helping to reduce the overall size of the circuit. The new configuration introduced uses an NMOS transistor at the bottom of the LC network as a current source for the LC tank. A biasing voltage at the gate terminals
of the NMOS transistors is required to enable the transistors.

![Improved LC VCO structure](image)

**Fig 3.3.4.1 Improved LC VCO structure**

The output signal of this configuration is obtained by having the NMOS transistors at both sides of the LC network output functioning as a voltage follower. When one of the output terminals of the LC tank goes to high, the connected top NMOS transistor (transistor T4 or T2) is turned on. This allows the positive voltage from $V_{dd}$ to flow to that output terminal since the gate terminal of bottom NMOS transistors (T5 or
T3) are connected to a positive biasing voltage causing it to be on at all times. When one of the output terminals of the LC tank goes to low, the connected top NMOS transistor (transistor T5 or T3) is turned off, and the bottom transistor is on, thus pulling the output to ground. The NMOS transistor at the bottom of the LC network acts like a current source when positive biasing voltage is applied to the gate terminal. This allows the LC network to have enough current to compensate the loss due to the impedances in the LC tank, thus sustaining the oscillation. The oscillating output signal of the circuit appears to be sinusoidal instead of square wave, due to the delay caused by the rising and falling time of the transistor. This is because it takes some time for the electrons to travel through the width of each transistor. The lower the frequency, the more square the output signal will appear. This is because: as frequency gets lower, the time that the signal is high or low becomes increasingly longer in comparison to the time for the signal to rise or fall, thus making the waveform looks squarer as the frequency lowers. Figure 3.3.4.2 shows the output waveform of the circuit with different tuning voltages. The operating frequency is maxed at 43.2GHz with the power consumption of 98mW.
Fig 3.3.4.2 waveform output signals with various tuning voltages

The tuning range of this circuit ranges from 42.675GHz to 43.23GHz, which is 0.55GHz, even smaller than the previous configuration discussed in section 3.3.3. This shows that as the operating frequency gets higher, the tuning range gets smaller due to the reduced size of the LC tank, since the range of maximum and minimum capacitance of the varactor is proportional to its physical size. The phase noise of this circuit comes out to be -80dBc/Hz at 1MHz offset, which is significantly higher compared to the previous circuit. Since the higher the frequency, the higher the impedances in the LC network causing more energy loss, thus lowering the Q factor. Figure 3.3.4.3 and Table 3.3.4 compares the tuning range of the two circuit configurations.
Fig 3.3.4.3 tuning range of the two LCVCO circuits

The relationship between the tuning voltage and the output frequency of the 43GHz LCVCO circuit is obtained.

\[ f_o = -0.6246V_t + 43.279 \]  

(3.3.4.1)

<table>
<thead>
<tr>
<th>LCVCO Circuit</th>
<th>Tuning range</th>
<th>Maximum Frequency</th>
<th>Power consumption</th>
<th>Phase noise at Maximum Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>22GHz LCVCO</td>
<td>2.35GHz</td>
<td>22.95GHz</td>
<td>49.85mW</td>
<td>-98dBc/Hz at 1MHz offset</td>
</tr>
<tr>
<td>43GHz LCVCO</td>
<td>0.55GHz</td>
<td>43.23GHz</td>
<td>98.49mW</td>
<td>-80dBc/Hz at 1MHz offset</td>
</tr>
</tbody>
</table>

Table 3.3.4 22GHz and 43GHz LCVCO Performance
4.1 Variable Frequency Divider Structure

4.1.1 CML Master-Slave Latch as a Divider

This structure uses the low voltage swing current mode, which allows the operation at very low power dissipation. For a conventional divider application, two Current Mode Logic (CML) latches that are identical are connected in a master-slave configuration as shown in Figure 4.1.1

![CML master-slave latch as a divider](image)

Fig 4.1.1 CML master-slave latch as a divider [3]
4.1.2 High Frequency CML Divider

The CML latch clocking structure is simplified by employing a single clock transistor pair to switch the current between the sample-and-hold pair of the master and slave latches [6]. The new configuration of the frequency divider circuit is shown in Figure 4.1.2. It uses a single biased current source for both of the two latches.

![High Frequency CML Divider Circuit Core Structure](image)

**Fig 4.1.2 High Frequency CML Divider Circuit Core Structure [3]**

The master-slave combined latch technique uses smaller transistor sizes for the hold pairs of both latches to accomplish the sample/hold current difference [6]. Because of the lower current flowing through the hold pair, the width of the current
source does not need to be doubled. This results in a reduction of the overall static power dissipation of the frequency divider circuit.

### 4.2 Proposed Variable High Frequency CML Divider

In order to make the high frequency CML divider circuit work with 40GHz, the transistor size ratio must be in an operable range. It must not be too small that it would choke the current, and it must not be too large that it would negate the sample/hold current difference. An inverter circuit with a N/P MOS transistor ratio of 5 is connected to both ends of the output of the divider circuit to provide load, as well as enhancing the output signal. This new configuration also allows the divider to vary its dividing factor as a function of load resistance from resistor R1 and R3. The proposed frequency divider circuit shown in Figure 4.2.1 takes an input frequency of 40-43GHz through “CLK” and divide up the input frequency as a function of the load resistor R1, R3 and R1, R2. To determine the relationship between the resistor value to the dividing coefficient of the circuit, an experiment was conducted to graph out the characteristics of the output frequency as a function of load resistance R1 and R3, while other components remain constant.
To determine the relationship between the resistor value to the dividing coefficient of the circuit, an experiment was conducted to graph out the characteristics of the output frequency as a function of load resistance $R_1$ and $R_3$, while other components remain constant. The following Figures illustrates the output of the frequency as the resistance $R_1$ and $R_3$ varies displaying duty cycle and the waveform shape.
Fig 4.2.2 output frequency of the variable high frequency divider

This graph shows that the duty cycle of the signal is far off from our goal of 50%. Therefore, the lower limit of our resistance value of R1 and R3 will be set higher than 50k Ohm. Figure 4.2.3 shows an improved waveform with duty cycle much closer to 50%.
When the resistor value is set to 900k Ohm, the frequency divider is no longer dividing the input signal. Therefore, the maximum resistance value of R1 and R3 is set to be lower than 900k Ohm. Figure 4.2.4 graphs the output frequency of the divider circuit as a function of R1 and R3. The relationship between the load resistances as a function of dividing constant is graphed out in Figure 4.2.5.
Table 4.2.1 output frequency as the function of load resistance

<table>
<thead>
<tr>
<th>R(kOhm)</th>
<th>f(MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>900</td>
</tr>
<tr>
<td>100</td>
<td>546</td>
</tr>
<tr>
<td>150</td>
<td>388</td>
</tr>
<tr>
<td>200</td>
<td>302</td>
</tr>
<tr>
<td>250</td>
<td>247</td>
</tr>
<tr>
<td>300</td>
<td>209</td>
</tr>
<tr>
<td>400</td>
<td>160</td>
</tr>
<tr>
<td>600</td>
<td>109</td>
</tr>
<tr>
<td>900</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Fig 4.2.4 output frequency versus load resistance

The relationship of the graph obtained appears to be a negative power function.
\[ f_0 = 27116R_L^{-0.855} \] (4.2.1)

The input frequency for this experiment is fixed at 40GHz; therefore, the dividing constant of the circuit essentially becomes the function of the load resistance \( R_L \).

![Graph showing the relationship between the dividing constant and load resistance](Image)

**Fig 4.2.5 dividing constant versus Load Resistance**

As it appears in the graph shown in Figure 4.2.5, the relationship between the dividing constant and the load resistance is strictly linear. For this reason, this variable frequency divider circuit structure can be used with other frequency...
dividing applications that require a high dividing constant. The implementation of the circuit however, needs a variable resistor in order for the dividing constant to be changed in real time. For in this case, the dividing constant will have to be fixed to the design, since it is quite difficult to implement a variable resistor in 90nm process. Equation 4.2.2 describes the function of dividing constant $N_D$ as a function of load resistance $R_L$.

$$N_D = 0.587R_L + 15.021 \tag{4.2.2}$$

The divider constant is obtained from taking the input frequency, which is 40GHz ($40 \times 10^9$Hz), and divides it by the output frequency at the corresponding load resistance. For example, the dividing constant when the load resistance is at 300 kΩ, which corresponds to an output frequency of 209 kHz ($209 \times 10^3$Hz), the diving constant is obtained by $(40 \times 10^9) / (209 \times 10^3) = 191,387$. The dividing constant has no unit.
The most difficult part in creating a reliable PLL system is the combination of the VCO and the frequency divider. The combination of the two modules must accomplish two main objectives; to generate the operating frequency, and to reduce that frequency down to where it can be match with the referencing clock signal. The expectation of the result is that there would be two frequencies produced by the combined circuit; one in the Mega Hertz range, and the other at the Giga Hertz range. When implementing the circuit however, the output signal from the VCO will need a buffer circuit since the waveform might be slightly altered due to the fact that it is being connected to the frequency divider circuit input terminal, which has resistance and some parasitic capacitance. The simulation set up will have a supply voltage of 1.2V (standard $V_{dd}$ in 90nm process), 1.2V at the bias voltage at the LCVCO and the tuning voltage varies from 0.1V to 1.2V. The load resistor in the variable frequency circuit is set to be 200 kΩ, which corresponds to the dividing constant of 103.092. The final circuit is shown in Figure 5.1.1 with the LCVC0 circuit is the smaller network at the top, and the variable frequency circuit is the larger network at the bottom. The two circuit is combined in one with connecting the output terminal from the LCVC0 to the CLK terminal of the frequency divider circuit.
5.1 Combination Result

Fig 5.1.1 LCVCO connected with Variable frequency divider circuit

Figure 5.1.2 is the output waveform of the circuit. The tuning voltage used in this
simulation is at 0.1V. The final output of the circuit is as expected; the final circuit produces two frequencies in MHz and GHz.

The top plot is the divided output signal with the frequency of 296MHz. The bottom plot is the operating frequency signal from the LCVCO circuit with a frequency of 43GHz.

**Fig 5.1.2 output signal of the final circuit**
The result indicates that the duty cycle of the divided signal is very close to the goal of 50%. The combined circuit is proved to be a success. The circuit simulation however, may contain a significant amount of margin of error since the simulation is done only in the schematic level. For the layout level simulation, the wire length, the metal resistance, and the capacitance between crossed wires are in consideration. However the simulation results obtained from the schematics level is sufficient to verify the design. The final circuit is to be used in conjunction with the rest of the PLL modules to create a fast, reliable, and low phase noise Phase Lock Loop frequency synthesizer system.
6.1 Conclusion

The inverter ring VCO circuit in chapter 2 provides a wide tuning range, but it has a limitation in producing a higher frequency. The inverter ring VCO can be used in applications that require a wide tuning range and low power consumption, but lower operating frequency. The LC tank VCO provides a higher range of output frequency but has lower tuning range. The simulation result of the variable high frequency divider circuit indicates that: the dividing constant can be adjusted by varying the load resistance of the CML latch. The relationship between the load resistance of the CML latch and the dividing constant is strictly linear. The circuit combination between the LC tank VCO, and the variable high frequency divider circuit produces both high and low frequency at the same time. The lower frequency output can be connected to the PFD for phase referencing. The higher frequency output can be used as output frequency of the PLL.
6.2 Future Work

For the variable frequency divider circuit to be used in a multiple range of frequencies in a PLL system, a type of voltage divider circuit could be developed in an attempt to change the loading resistance in real time. The VCO circuit as well as the adjustable frequency divider circuit is yet to be implemented to the full PLL system. The development of the phase frequency detector (PFD), and the loop filter is yet to be done for the completion of a PLL system. The work of this research is based upon the 90nm technology. As of now, the technology is down to 32nm. The size of the transistor affects the design aspect of the PLL system greatly. For future work, the method of designing the inverter ring VCO and LC VCO discussed in this research can still be carried on into the 32nm process.
References


