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**Gallium Nitride: Analysis of Physical Properties and Performance in High-Frequency Power Electronic Circuits**

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GALLIUM NITRIDE: ANALYSIS OF PHYSICAL PROPERTIES AND PERFORMANCE IN HIGH-FREQUENCY POWER ELECTRONIC CIRCUITS

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering

By

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Abstract


Gallium nitride (GaN) technology is being adopted in a variety of power electronic applications due to their high efficiencies even at high switching speeds. In comparison with the silicon (Si) transistors, the GaN-based devices exhibit lower on-state resistance and parasitic capacitances. The thermal performance of the GaN transistors are also better than the Si counterparts due to their higher junction temperature and lower temperature-coefficient of on-resistance. These unique properties make the gallium-nitride power transistors an appropriate selection for power electronic converters and radio-frequency power amplifiers, where size, efficiency, power density, and dynamic performance are major requirements.

Foreseeing the immense capabilities of the GaN transistors in the near future for the fast-growing electronic industry, this thesis endeavors to make the following contributions: (a) analyze the important properties of GaN as a semiconductor material, (b) study the formation of the 2-dimensional electron gas layer required for current conduction, (c) determine the functionality of the GaN as a field-effect transistor, and (d) test its performance through simulations and experiments at high switching frequencies in power electronic converters, where the Si-based transistors cease to operate normally. The critical material properties include the intrinsic carrier concentration, the specific on-resistance, and the intrinsic carrier mobility. The dependence of these properties on the temperature is investigated. The comparison of these properties are made with the silicon and silicon-carbide (SiC) semiconductor materials to give a clear view about the superior performance of GaN over the other types.

While the Si MOSFETs create a channel to conduct the electrons and holes between the source and drain terminals, the GaN field-effect transistors (FET) form a 2-dimensional electron gas (2-DEG) layer, whose thickness is controlled by the applied gate potential. Because of the high electron density in the 2-DEG layer, the GaN FETs are termed as high-electron mobility transistors (HEMT). The operation of both enhancement and depletion
mode GaN FETs are discussed in detail and the model of the drain current through the 2-DEG layer is provided. The figure-of-merit (FOM) for the GaN transistors is explained and then compared with that of Si and SiC transistors.

Two important implementations of GaN transistors are in the (a) pulse-width modulated synchronous-buck DC-DC power converters and (b) Class-D resonant inverters. These circuits are better representative examples since they comprise of one GaN FET (high-side switch) connected to a “hot” point and the other GaN FET (low-side switch) referenced to ground. While the low-side switch consumes minimum gate-drive power for turn ON/OFF transitions, the high-side switch demands a higher gate-drive power to operate the transistor as a switch. Also, these switches exhibit switching losses due to the charge/discharge process of the parasitic capacitances. The gate-drive power and switching losses increase as the switching frequency is increased. However, due to the superior performance and very low values of the device parasitic resistances and capacitances in the GaN transistors, higher switching frequencies can be achieved at very minimal switching losses. Simulations were performed to analyze the behavior of the two circuits at different switching frequencies and were compared with those using Si transistors. It is observed that the overall efficiency reduced to 48% at 5 MHz for the Si-based buck converter and down to 41% at 5 MHz for the Si-based Class-D inverter. However, using GaN transistors showed an improved performance, where the overall efficiency reduced to only 71% at 15 MHz for the buck converter and 60% at 10 MHz for the Class-D inverter.

Further, experimental validations were performed on a prototype of the synchronous buck converter developed using the high-frequency, half-bridge switching network module EPC9037 manufactured by Efficient Power Conversion Corporation. The module comprises of the enhancement-mode GaN transistors and a high-speed, dual-side, high-performance gate-driver LM5113 by Texas Instruments. The experimental results showed the immense capability of the GaN transistors to achieve high efficiencies. The experimentally measured efficiency of the synchronous buck converter was 85% at a switching frequency of 5 MHz and reduced to 60% at 8MHz. The theoretical predictions were in good agreement with simulation and experiment results.
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1 Introduction

The gallium nitride (GaN) semiconductor has turned out to be the best replacement for the existing silicon technology due to its excellent material properties. GaN has a brilliant future in a variety of power electronic applications. This thesis presents an extensive study on the properties and characteristics of gallium nitride as a semiconductor material and as a transistor, its unique advantages, when compared with its other counterparts, and its applications in high switching frequency power electronic converters.

1.1 Background

The material, which we call “semiconductor”, has a rich and interesting history that begins from 1833, when Michael Faraday discovered that semiconductor electrical conductivity increases with increase in temperature [1], [2]. This behavior of semiconductor was different from the behavior exerted by metals, where conductivity decreases with increase in temperature. The progress was slow until 1948, when point contact devices were first introduced leading to the use of silicon extensively. The history of information theory was made by silicon because of its excellent characteristics. Silicon products have evolved over time and considered as a carrier of information for a long time. It has played a tremendous role in the development of high performance electronic devices, which are part of our everyday lives [3]. Silicon is the heart of conventional computer-based technology. From our cell phones, super-fast computers to high-tech cars, most of the technology we enjoy today is because of the enormous development in computing. This advancement was possible because of the growth in the transistor industry. The transistor is one of the immense technological accomplishments of the last century. According to Intel co-founder, Gordon Moore, the number of transistors on an integrated circuit has been doubling approximately every two years to keep up with computing power we need today. This trend is called Moore’s Law [4]. However, for how long can we keep increasing this number? With the exponentially growing information, we are running out of space to store the data. The capacity to increase
the computing power by adding more and more transistors will eventually break down. Researchers have seriously started to figure out new methods to shrink the size of transistors as well as increase the processing speed higher than ever before. The performance of silicon devices is limited for today’s requirements because of inherent limitations of its properties [3]-[4]. Computing power cannot sustain its exponential growth by relying on silicon anymore. Moreover, silicon has reached its theoretical limit in power conversion. It cannot fulfill the requirements in applications for high-voltage and high-power systems. The question is, what is a good replacement for silicon? Wide band gap (WBG) semiconductors have the potential to do this job.

In the last few years, gallium nitride (GaN) and silicon carbide (SiC) have been receiving much attention. Also, SiC and GaN semiconductors are commonly attributed as compound semiconductors because they are comprised of multiple elements from different groups in the periodic table. These materials have challenged the long held dominance of silicon.

GaN and SiC have a wide band gap as compared to Si. The critical electric field or breakdown field of GaN and SiC is an order of magnitude higher than that of Si. These WBG materials can withstand high operating temperatures, high frequencies, and higher voltages leading to much efficient power conversion systems. As a result of these characteristics, the electronic devices can be made with low power losses and are smaller in size as compared to the present day technology.

GaN devices, the best alternative to Si, has the ability to switch at high frequencies with low power losses and as a result can achieve high efficiencies. High-frequency operation to achieve high bandwidth reduces the size of passive components making it far easier to make compact electronic circuits. With the excellent properties such as wider band gap, high breakdown voltage, higher breakdown electric field, and higher electron mobility, GaN devices can operate at higher voltages and high switching frequencies. In addition, GaN material has high electron saturation velocity. This property allows the GaN based devices to operate at much higher speeds. Also, GaN power transistors help lessen the losses due to
conduction and switching, hence offering a higher efficiency. The foremost application area of GaN power devices are power electronic converters and radio-frequency power amplifiers [7]-[22].

1.2 Research Motivation

In modern society, energy is the key factor of economy. Energy-saving has become a worldwide priority. The environmental issues such as depletion of our natural resources, pollution and global warming, etc., have made the introduction of new and efficient energy sources necessary. Inefficient systems cause extra cost for wasted energy. There is an immediate need to improve efficiency by choosing better components and redesigning the power systems. The requirement of efficient power devices in electrical systems for energy conservation is increasing. Therefore, it is crucial to optimize the efficiency of these devices to minimize energy loss during their operation. In power devices, there are two main sources for energy losses: conduction losses and switching losses.

- Conduction losses: The on-resistance of power devices cause dissipation of power by obstructing the flow of electric current through them resulting in conduction losses.

- Switching losses: The parasitic capacitance of the devices store energy and dissipate the energy during switching. This transition during on and off intervals cause switching losses. The switching losses are directly proportional to the parasitic capacitance and to the switching frequency. The capacitance increases with the increase in the size of the device, which increases the switching losses. In addition, the switching losses at the gate of the transistor also increase with frequency, where the energy is used to charge and discharge the gate-to-source and gate-to-drain capacitances of the transistor.

GaN transistor is the next generation power device. GaN technology can lead to many applications. It allows reduction in power losses and attain fast-speed switching because of
its attractive physical properties. Figure 1.1 shows the main properties of GaN, SiC, and Si.

The motivation behind this thesis includes investigating the critical properties of the GaN semiconductor as a material and as a device, present the necessary expression, which are relevant to making a proper transistor selection, and also to determine how well these devices perform at high switching frequencies. In addition to the current state-of-the-art, this thesis attempts to make a comprehensive analysis of GaN; a study helpful for practicing engineers, researchers in the field of electronics, and physicists. A few specific motivations are:

• Current trend in power electronic circuits is focused towards high-power, high-speed operation.

• Existing literature predominantly focuses on fabrication of GaN material.

• Advanced properties of GaN must be explored to justify its applications in various fields.

• Connect the gap between the datasheet parameters with the actual physical properties of GaN transistors.

• Go beyond the state-of-the-art to determine the hard-limits of the performance of GaN transistors (in terms of frequency of operation).

1.3 Thesis Objectives

The objectives of this thesis are as follows:

• To analyze the fundamental intrinsic characteristics of the gallium nitride semiconductor material and to compare its properties with silicon and silicon carbide semiconductor materials.
• To give an overview on the operation of the gallium nitride field-effect transistors in enhancement mode.

• To investigate the electrical and switching characteristics of EPC2020 gallium nitride high electron mobility transistor [8] through simulations and to compare its properties with its silicon counterpart.

• To investigate the switching characteristics of a half-bridge switching network composed of gallium nitride power MOSFET using EPC2020 half-bridge switching module manufactured by Efficient Power Conversion (EPC), with the help of synchronous buck dc-dc converter and Class-D resonance inverter.

• To perform experiments on a buck DC-DC power converter and investigate the operation of the converter at high switching frequencies.

• To validate the theoretical predictions by experimental results.

1.4 Existing Technology

It is not possible to ignore the wonderful material properties of the Nobel Prize winning material, which is gallium nitride (GaN). The development of efficient blue LEDs was enabled because of GaN. The excellence of GaN is explained in detail in [9]. According to the
article, “Efficient Blue Light-Emitting Diodes Leading to Bright and Energy-Saving White Light Sources” [9]:

“Today, GaN-based LEDs provide the dominant technology for back-illuminated liquid crystal displays in many mobile phones, tablets, laptops, computer monitors, TV screens, etc. Blue and UV-emitting GaN diode lasers are also used in high-density DVDs, which has advanced the technology for storing music, pictures and movies. Future application may include the use of UV-emitting AlGaN/GaN LEDs for water purification, as UV light destroys the DNA of bacteria, viruses and microorganisms. In countries with insufficient or non-existent electricity grids, the electricity from solar panels stored in batteries during daylight, powers white LEDs at night. There, we witness a direct transition from kerosene lamps to white LEDs.”

Moreover, GaN high electron mobility transistor (HEMT) has proved its significance as power devices [10]. GaN power devices, due to high breakdown voltage and high power densities are in great demand. These devices are suitable for the high-speed operation of power amplifiers. According to Wood, the GaN HEMT has enabled designing very high efficient PAs involving Class-D, Class-E, Class-F, and Class-J techniques [10].

Efficient Power Conversion Corporation (EPC) is one of the biggest provider of GaN power transistors [8]. EPC introduced their first enhancement-mode GaN high-electron mobility transistors in 2009 [8]. The products of EPC include enhancement-mode GaN FETs, enhancement-mode GaN drivers, and controllers. These products are being utilized widely in many applications such as data-communication and tele-communication systems, envelope tracking, wireless power, LIDAR, audio amplifiers, and power inverters.

The availability of gallium nitride (GaN) substrates is limited [11]. Sapphire and SiC are quality substrates, but are very costly and are not very useful in terms of commercialization. Silicon substrates are the most refined substrates for GaN. GaN on silicon offers a low cost,
high performance platform for high-frequency and high-power products.

GaN will make it as the future semiconductor device in many more applications including high-speed communication systems, automotive, radar systems, radio-frequency amplifiers, integrated circuit, lasers, solid-state microwave circuits, military, and aerospace applications, etc. [12].

1.5 Organization of the Thesis

The thesis is comprised of seven chapters. The chapters are organized as follows

- Chapter 2 discusses the physical properties of GaN and their comparison with the properties of Si and SiC. Moreover, Chapter 2 presents the various expressions of the physical properties of semiconductor materials, develops a case study for gallium nitride semiconductor material and compares its properties with silicon and silicon carbide semiconductors.

- Based on the properties discussed in Chapter 2, Chapter 3 addresses the properties of the gallium nitride field-effect transistor. The two types of GaN FETs namely, depletion-mode and enhancement-mode are discussed along with their functionality. The model of EPC2020 GaN HEMT [8] is considered and its DC and AC characteristics are observed.

- In Chapter 4, one implementation of GaN transistors in the pulse-width modulated synchronous buck dc-dc converter is discussed. Using a practical design example, the analysis of the converter and the performance evaluation is made at various frequencies of interest to determine the limitations of the GaN transistor.

- In Chapter 5, another implementation of GaN transistors in frequency-controlled Class-D resonant inverters is discussed. The efficiencies of the converter at different switching frequencies are evaluated. A comparison of its performance is made
with the silicon-based switching network to determine the critical differences between the two schemes.

• Chapter 6 discusses the main results of this thesis and provides the essential comparison results for the properties of Si, SiC and GaN materials and devices. Further, the experimental results obtained using the laboratory prototype of the synchronous buck dc-dc converter discussed in Chapter 4 are provided. The results of the Class-D resonant inverter are also included.

• Finally, Chapter 7 summarizes this thesis work, provides the conclusions, and suggests scope for future work.
2 Overview of GaN Technology

2.1 Fundamental Properties of GaN Semiconductor Material

For years, silicon-based power MOSFETs have been used in many applications such as power conversion, radio-frequency power amplifiers, analog electronics, transducers, etc. With silicon reaching its performance limit, gallium nitride (GaN) has emerged as a promising technology to replace the silicon-based technology. This new technology offers many advantages in high voltage and high frequency power management systems, and power converters. The basic properties of GaN semiconductors at room temperature are given in the Table 2.1 along with silicon and silicon carbide for comparison.

Gallium nitride is a compound of gallium and nitrogen, where gallium (atomic number 31) belongs to group 13 and nitrogen (atomic number 7) belongs to group 15. In nature, GaN exists in two allotropic forms namely, wurtzite and zinc blende EPC. In both of these structures, each group III atom, in this case the gallium atom is bonded with four nitrogen

![Figure 2.1: Structure of wurtzite GaN crystal.](image)
atoms. Figure 2.1 shows a representation of the structure of the wurtzite GaN crystal. In the figure, the large circles are the gallium atoms and the smaller dense circles are the nitrogen atoms. The pattern of the structure is hexagonal and is commonly referred to as α-GaN.

The structure of both forms of GaN are chemically very stable, which enhances the piezoelectric properties of GaN. GaN is usually doped to make a n-type or p-type material with silicon or magnesium, respectively [9]. Defects in the crystal enhance the electron conductivity of GaN material. Manufacturing the p-type GaN is difficult, hence it is usually a n-type extrinsic material. The structural properties of GaN lead to high conductivity. Piezoelectric effect in the material occurs, when the crystal is subjected to a mechanical strain [8]. By disturbing the lattice structure of the crystal, the displacement of charge particles within the crystal lattice results in the generation of an electric field.

The performance of any semiconductor devices depends on many intrinsic characteristics of the material. These characteristics include conductivity, breakdown voltage, and thermal properties. The data shown in Table 2.1 determines that the GaN semiconductors are superior than silicon (Si) in term of high breakdown voltage, higher mobility, and better thermal conductivity.

2.1.1 Band Gap Energy of GaN

The band gap energy $E_G$ of semiconductors determine the energy needed to break the covalent bonds in the lattice. Higher energy is required if these bonds are strong making it difficult for the electrons to jump from the valence band to the conduction band within a material. As shown in Table 2.1, the band gap energy of GaN is very high as compared to Si, which makes it suitable for high temperature applications [8].
Table 2.1: Properties of Silicon, Silicon Carbide, and Gallium Nitride.

<table>
<thead>
<tr>
<th>Property</th>
<th>Symbol</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon band gap energy</td>
<td>$E_{G(Si)}$</td>
<td>eV</td>
<td>1.12</td>
</tr>
<tr>
<td>Silicon band gap energy</td>
<td>$E_{G(Si)}$</td>
<td>J</td>
<td>$1.793 \times 10^{-19}$</td>
</tr>
<tr>
<td>Silicon-carbide band gap energy</td>
<td>$E_{G(SiC)}$</td>
<td>eV</td>
<td>3.26</td>
</tr>
<tr>
<td>Silicon-carbide band gap energy</td>
<td>$E_{G(SiC)}$</td>
<td>J</td>
<td>$5.216 \times 10^{-19}$</td>
</tr>
<tr>
<td>Gallium-nitride band gap energy</td>
<td>$E_{G(GaN)}$</td>
<td>eV</td>
<td>3.39</td>
</tr>
<tr>
<td>Gallium-nitride band gap energy</td>
<td>$E_{G(GaN)}$</td>
<td>J</td>
<td>$5.430 \times 10^{-19}$</td>
</tr>
<tr>
<td>Silicon breakdown electric field</td>
<td>$E_{BD(Si)}$</td>
<td>V/cm</td>
<td>$2 \times 10^5$</td>
</tr>
<tr>
<td>Silicon-carbide breakdown electric field</td>
<td>$E_{BD(SiC)}$</td>
<td>V/cm</td>
<td>$22 \times 10^5$</td>
</tr>
<tr>
<td>Gallium-nitride breakdown electric field</td>
<td>$E_{BD(GaN)}$</td>
<td>V/cm</td>
<td>$35 \times 10^5$</td>
</tr>
<tr>
<td>Silicon relative permittivity</td>
<td>$\varepsilon_r(Si)$</td>
<td>–</td>
<td>11.7</td>
</tr>
<tr>
<td>Silicon-carbide relative permittivity</td>
<td>$\varepsilon_r(SiC)$</td>
<td>–</td>
<td>9.7</td>
</tr>
<tr>
<td>Gallium-nitride relative permittivity</td>
<td>$\varepsilon_r(GaN)$</td>
<td>–</td>
<td>8.9</td>
</tr>
<tr>
<td>Silicon electron mobility at $T = 300$ K</td>
<td>$\mu_n(Si)$</td>
<td>cm$^2$/V·s</td>
<td>1360</td>
</tr>
<tr>
<td>Silicon-carbide electron mobility at $T = 300$ K</td>
<td>$\mu_n(SiC)$</td>
<td>cm$^2$/V·s</td>
<td>900</td>
</tr>
<tr>
<td>Gallium-nitride electron mobility at $T = 300$ K</td>
<td>$\mu_n(GaN)$</td>
<td>cm$^2$/V·s</td>
<td>2000</td>
</tr>
<tr>
<td>Silicon hole mobility at $T = 300$ K</td>
<td>$\mu_p(Si)$</td>
<td>cm$^2$/V·s</td>
<td>480</td>
</tr>
<tr>
<td>Silicon-carbide hole mobility at $T = 300$ K</td>
<td>$\mu_p(SiC)$</td>
<td>cm$^2$/V·s</td>
<td>120</td>
</tr>
<tr>
<td>Gallium-nitride hole mobility at $T = 300$ K</td>
<td>$\mu_p(GaN)$</td>
<td>cm$^2$/V·s</td>
<td>30</td>
</tr>
<tr>
<td>Silicon effective electron mass coefficient</td>
<td>$k_e(Si)$</td>
<td>–</td>
<td>0.26</td>
</tr>
<tr>
<td>Silicon effective hole mass coefficient</td>
<td>$k_h(Si)$</td>
<td>–</td>
<td>0.39</td>
</tr>
<tr>
<td>Silicon-carbide effective electron mass coefficient</td>
<td>$k_e(SiC)$</td>
<td>–</td>
<td>0.36</td>
</tr>
<tr>
<td>Silicon effective hole mass coefficient</td>
<td>$k_h(SiC)$</td>
<td>–</td>
<td>1</td>
</tr>
<tr>
<td>Gallium-nitride effective electron mass coefficient</td>
<td>$k_e(GaN)$</td>
<td>–</td>
<td>0.23</td>
</tr>
<tr>
<td>Gallium-nitride effective hole mass coefficient</td>
<td>$k_h(GaN)$</td>
<td>–</td>
<td>0.24</td>
</tr>
</tbody>
</table>
Table 2.2: Summary of calculated values for the thermal velocity of charge carriers for the three semiconductors at two different temperatures

<table>
<thead>
<tr>
<th>Temp. (K)</th>
<th>Charge</th>
<th>$v_{th}$ for Si (m/s)</th>
<th>$v_{th}$ for SiC (m/s)</th>
<th>$v_{th}$ for GaN (m/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T = 300$ K</td>
<td>electron</td>
<td>$2.29 \times 10^5$</td>
<td>$1.94 \times 10^5$</td>
<td>$2.43 \times 10^5$</td>
</tr>
<tr>
<td>$T = 300$ K</td>
<td>hole</td>
<td>$1.86 \times 10^5$</td>
<td>$1.16 \times 10^5$</td>
<td>$2.38 \times 10^5$</td>
</tr>
<tr>
<td>$T = 473$ K</td>
<td>electron</td>
<td>$2.87 \times 10^5$</td>
<td>$2.44 \times 10^5$</td>
<td>$2.99 \times 10^5$</td>
</tr>
<tr>
<td>$T = 473$ K</td>
<td>hole</td>
<td>$2.34 \times 10^5$</td>
<td>$1.46 \times 10^5$</td>
<td>$2.99 \times 10^5$</td>
</tr>
</tbody>
</table>

2.1.2 Thermal Velocity of Charge Carriers

Thermal electron velocity of a semiconductor can be expressed as [13]

$$v_{th(e)} = \sqrt{\frac{3kT}{k_e m_e}}$$  \hspace{1cm} (2.1)

and thermal hole velocity of a semiconductor can be expressed as

$$v_{th(h)} = \sqrt{\frac{3kT}{k_h m_e}}$$  \hspace{1cm} (2.2)

where $k$ is Boltzmann’s constant equal to $1.38 \times 10^{-23}$ J/K, $T$ is the temperature, $k_e$ is the effective mass coefficient for electrons, $k_h$ is the effective mass coefficient for holes, and $m_e$ is the mass of electrons in free space. Using equations (2.1) and (2.2) with the values mentioned in Table 2.1, the thermal velocity of electrons and the thermal velocity of holes for the different semiconductors at room temperature $T = 300$ K and at a temperature $T = 473$ K are as tabulated in Table 2.2.

2.1.3 Breakdown (Critical) Electrical Field and Breakdown Voltage

A wider energy band gap results in a higher electrical field intensity required for ionization, and hence increases the potential required to cause avalanche breakdown. A higher breakdown voltage $V_{BD}$ can be achieved, because of the high wide band gap energy of GaN. Since the breakdown voltage of the semiconductors is directly proportional to the breakdown elec-
tric field $E_{BD}$, the GaN-based devices are apt for high voltage applications also and is a suitable replacement with the lossy silicon transistors. Also, higher breakdown voltages reduce the size of the transistor resulting in smaller resistance for current flow. Thus, GaN exhibits lower on-state resistance, when used as transistors than the silicon-based devices and is discussed in great detail in the following chapter.

### 2.1.4 Intrinsic Carrier Concentration

In equilibrium and in pure form, the concentration of free electrons $n$ and concentration of free holes $p$ in intrinsic semiconductors are equal and can be expressed as [13]

$$n = p = n_i = 2 \left( \frac{2\pi m_e kT}{\hbar^2} \right)^{3/2} (k_e k_h)^{3/4} e^{-\frac{E_G}{kT}} \left( \text{carriers cm}^{-3} \right),$$  \hspace{1cm} (2.3)

where $m_e$ is the mass of a free electron, $k$ is the Boltzmann’s constant, $T$ is the temperature, $k_e$, $k_h$ are the electron and hole mass coefficients, respectively, $E_G$ is the band gap energy, and $h$ is the Planck’s constant. The numbers indicate that GaN is a very good insulator at room temperature, when compared to Si. Table 2.3 summarizes the values of the intrinsic concentration of Si, SiC, and GaN at three different temperatures. Figures 2.2, 2.3, and 2.4 show the plots of the intrinsic carrier concentration $n_i$ for silicon, silicon carbide and gallium nitride as functions of temperature $T$, respectively. It can be observed that at room temperature and below, the Si material possesses sufficiently large number of free carriers required to conduction, whereas the SiC and GaN materials release almost no carriers into

---

**Table 2.3: Summary of calculated values for the intrinsic concentrations of the three semiconductors at different temperatures**

<table>
<thead>
<tr>
<th>Intrinsic concentration (cm$^{-3}$)</th>
<th>Si</th>
<th>SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$n_i$ at $T = 273$ K</td>
<td>$1.85 \times 10^8$</td>
<td>$9.10 \times 10^{-12}$</td>
<td>$1.43 \times 10^{-13}$</td>
</tr>
<tr>
<td>$n_i$ at $T = 300$ K</td>
<td>$1.81 \times 10^9$</td>
<td>$5.31 \times 10^{-9}$</td>
<td>$1.07 \times 10^{-10}$</td>
</tr>
<tr>
<td>$n_i$ at $T = 423$ K</td>
<td>$1.63 \times 10^{12}$</td>
<td>$7.96 \times 10^{-1}$</td>
<td>$3.34 \times 10^{-2}$</td>
</tr>
<tr>
<td>$n_i$ at $T = 523$ K</td>
<td>$4.23 \times 10^{13}$</td>
<td>$5.58 \times 10^3$</td>
<td>$3.29 \times 10^2$</td>
</tr>
</tbody>
</table>
the conduction band. However, as the temperature is increased, the forbidden energy band gap $E_G$ reduces, making way for more free carriers to enter the conduction band. In other words, at $T = 473$ K and beyond, while the Si semiconductor still contains free carriers in abundance, the SiC and GaN materials slowly begin to lose the carriers in the valence band to the conduction band.

### 2.1.5 Extrinsic Carrier Concentration

The n-type extrinsic semiconductor is formed by doping impurities into the material. The conductivity of semiconductors can be significantly improved by adding donor atoms. In n-type semiconductor, the electrons are majority carriers and holes are minority carriers. The donor concentration $N_D$ is much higher than intrinsic carrier concentration. Consider a n-type semiconductor material. The majority free electron concentration $n_n$ and the minority hole concentration $p_n$ are given by [13]

$$n_n = \sqrt{\frac{N_D^2 + 4n_i^2 + N_D}{2}},$$  

(2.4)
Figure 2.3: Intrinsic carrier concentration $n_i$ as a function of temperature $T$ for silicon carbide.

Figure 2.4: Intrinsic carrier concentration $n_i$ as a function of temperature $T$ for gallium nitride.
Figure 2.5: Intrinsic carrier concentration \(n_i\), majority carrier (electrons) concentration \(n_n\), minority carrier (holes) concentration \(p_n\), and donor concentration \(N_D\) as functions of temperature \(T\) for silicon with \(N_D = 5 \times 10^{16} \text{ cm}^{-3}\).

Figure 2.6: Intrinsic carrier concentration \(n_i\), majority carrier (electrons) concentration \(n_n\), minority carrier (holes) concentration \(p_n\), and donor concentration \(N_D\) as functions of temperature \(T\) for silicon carbide with \(N_D = 5 \times 10^{16} \text{ cm}^{-3}\).
Figure 2.7: Intrinsic carrier concentration $n_i$, majority carrier (electrons) concentration $n_n$, minority carrier (holes) concentration $p_n$, and donor concentration $N_D$ as functions of temperature $T$ for gallium nitride with $N_D = 5 \times 10^{16}$ cm$^{-3}$.

$$p_n = \sqrt{\frac{N_D^2 + 4n_i^2 - N_D}{2}}. \quad (2.5)$$

Figures 2.5, 2.6, and 2.7 show the plots of the intrinsic carrier concentration $n_i$, majority electron concentration $n_n$, and minority hole concentration $p_n$ as functions of temperature $T$ for the n-type silicon, silicon carbide, and gallium nitride semiconductor materials, respectively. The assumed value of the donor concentration is $N_D = 5 \times 10^{16}$ cm$^{-3}$. From these figures, the maximum junction temperature can be evaluated. The maximum junction temperature $T_{J_{\text{max}}}$ is defined as a temperature beyond which the doped semiconductor loses its extrinsic properties and behaves as an intrinsic semiconductor. Using the data provided in the figure, one may observe the junction temperature to be at approximately 1000 K, which occurs at a carrier concentration $N_J$, where $N_D = n_i = p_n = n_n$. However, a conservative approach is considered and a temperature corresponding to $N_J/10$ is used as the junction temperature in this thesis. Therefore, an approximate junction temperature for Si is $T_{J_{\text{max}}} = 750$ K or $T_{J_{\text{max}}} = 477$ °C. Similarly, the maximum junction temperature for
SiC is relatively higher than Si. Using similar analysis, $T_{J_{\text{max}}}$ for SiC is 1800 K or 1527 °C. Based on a similar approach, the $T_{J_{\text{max}}}$ for GaN is 2000 K or 1723 °C.

### 2.1.6 Charge Carrier Mobility and Saturation Velocity

The mobility of charge carriers describes the freedom of movement in a lattice. The charge carriers move constantly in a random fashion in the lattice. When an electric field is applied to the charge carriers, the electrons and holes gain drift velocity. In a lattice, the electron mobility is greater than hole mobility. At low field, the charge carrier mobilities highly depend on doping concentration. For Si, the empirical expressions for the low-field mobilities of electrons and holes at room temperature $T = 300$ K are given as [13]

\[
\mu_{n(300)} = 92 + \frac{1268}{1 + (\frac{N_D}{1.3 \times 10^{17}})^{0.91}},
\]

\[
\mu_{p(300)} = 54.3 + \frac{406.9}{1 + (\frac{N_A}{6.3 \times 10^{17}})^{0.88}},
\]

where $N_D$ is the concentration of the donor atoms in the extrinsic semiconductor, and $N_A$ is the concentration of acceptor atoms in the extrinsic semiconductor. For SiC, the empirical expressions for the low-field mobilities of electrons and holes at room temperature $T = 300$ K are

\[
\mu_{n(300)} = 40 + \frac{947}{1 + (\frac{N_D}{9.4 \times 10^{17}})^{0.61}},
\]

\[
\mu_{p(300)} = 15.9 + \frac{124}{1 + (\frac{N_A}{1.76 \times 10^{19}})^{0.34}}.
\]

Similarly, for GaN, the empirical expressions for the low-field mobilities of electrons and holes at room temperature $T = 300$ K are [14],

\[
\mu_{n(300)} = 55 + \frac{1945}{1 + (\frac{N}{2 \times 10^{14}})^{0.0}},
\]

\[
\mu_{p(300)} = 30 + \frac{27}{1 + (\frac{N}{3 \times 10^{14}})^{2.0}},
\]
Figure 2.8: Low-field electron mobility $\mu_n$ as a function of doping concentration at room temperature $T = 300$ K for silicon.

Figure 2.9: Low-field hole mobility $\mu_p$ as a function of doping concentration at room temperature $T = 300$ K for silicon.
Figure 2.10: Low-field electron mobility $\mu_n$ as a function of doping concentration at room temperature $T = 300$ K for silicon carbide.

Figure 2.11: Low-field hole mobility $\mu_p$ as a function of doping concentration at room temperature $T = 300$ K for silicon carbide.
Figure 2.12: Low-field electron mobility $\mu_n$ as a function of doping concentration at room temperature $T = 300$ K for gallium nitride.

Figure 2.13: Low-field hole mobility $\mu_p$ as a function of doping concentration at room temperature $T = 300$ K for gallium nitride.
where $N$ is the concentration of the electrons and holes in the bulk. Figures 2.8, 2.10, and 2.12 show the plots of the low-field electron mobilities $\mu_n$ as a function of the doping concentration for silicon, silicon carbide, and gallium nitride, respectively at a room temperature $T = 300$ K. Figure 2.9, 2.11, and 2.13 show the plots of the low-field hole mobilities $\mu_p$ as a function of the doping concentration for silicon, silicon carbide, and gallium nitride, respectively at a room temperature $T = 300$ K. One may observe that the electron mobility of GaN stands highest, when compared to the other two materials. At low doping, the electron mobility of Si $\mu_n(300)$ is 1360 cm$^2$/V·s, and the mobility of SiC is 960 cm$^2$/V·s, while the mobility of GaN is 2000 cm$^2$/V·s.

The mobility of holes is the highest in Si, when compared to that of GaN and SiC. Thus, one may assume that due to the very low hole mobilities, the size of respective semiconductor device (diode or transistor) required to conduct a specific current is very large. In this regard, Si-based devices may be preferred over SiC and GaN, where the current conduction takes place through the majority hole movement.

It is clear from the above figures that GaN has high electron mobility and is suitable for high-speed applications. However, these mobilities have a strong dependence on temperature. The temperature dependance of mobility is given by the following expression [8] for all the three semiconductor materials

$$\mu_{n0} = \mu_{n(300)} \left(\frac{300}{T}\right)^\eta,$$  \hspace{1cm} (2.12)

and

$$\mu_{p0} = \mu_{p(300)} \left(\frac{300}{T}\right)^\eta,$$  \hspace{1cm} (2.13)

where $\eta$ is a material-dependent constant, which decides the magnitude of the change in the mobility with temperature. Table 2.4 summarizes the values of $\eta$ for the three different materials. Figures 2.14, 2.16, and 2.18 show the plots of low-field electron mobility $\mu_n$ as functions of temperature $T$ for silicon, silicon carbide, and gallium nitride. Figures 2.15, 2.17, and 2.19 show the plots of low-field hole mobility $\mu_p$ as functions of temperature $T$.
Figure 2.14: Low-field electron mobility $\mu_n$ as a function of temperature $T$ for silicon.

Figure 2.15: Low-field hole mobility $\mu_p$ as a function of temperature $T$ for silicon.

for silicon, silicon carbide, and gallium nitride.

The average drift velocity $v_n$ of the electrons under the influence of the electric field $E$
Figure 2.16: Low-field electron mobility $\mu_n$ as a function of temperature $T$ for silicon carbide.

Figure 2.17: Low-field hole mobility $\mu_p$ as a function of temperature $T$ for silicon carbide.

is [13]

$$v_n = \mu_n E.$$  

(2.14)
Figure 2.18: Low-field electron mobility $\mu_n$ as a function of temperature $T$ for gallium nitride.

Figure 2.19: Low-field hole mobility $\mu_p$ as a function of temperature $T$ for gallium nitride.
The dependence of the electron mobility on the electric field can be determined using

$$\mu_n = \frac{\mu_{n0}}{1 + \frac{\mu_{n0}E}{v_{sat}}} \tag{2.15}$$

where $\mu_{n0}$ is the low-field mobility of the electrons and $v_{sat}$ is the electron saturation velocity, which is dependent on the material properties. For Si, $v_{sat} = 1 \times 10^5$ m/s, for SiC, $v_{sat} = 2.2 \times 10^5$ m/s, and for GaN, $v_{sat} = 2.5 \times 10^5$ m/s. Substituting equation 2.15 into equation 2.14, we obtain

$$v_n = \frac{\mu_{n0}E}{1 + \frac{\mu_{n0}E}{v_{sat}}} \tag{2.16}$$

Figures 2.20, 2.21, and 2.22 show the average electron drift velocity $v_n$ as a function of the electric field intensity $E$ for silicon, silicon carbide, and gallium nitride, respectively. Further, Based on these curves the electric field can be divided into three regions: the low-field region ($10 < E < 10^3$), the intermediate field region ($10^3 < E < 2 \times 10^5$), and the high-field region ($E > 10^5$). In the low-field and intermediate field regions, the average velocity is directly proportional to the electric field and attains saturated value in the high-field region, i.e. at higher values of the electric field, the control over the velocity by the field intensity is diminished and then $v_n = v_{sat}$. The trend in the average electron drift velocity is due to the behavior of the field-dependent mobility. Figures 2.23, 2.24, and 2.25 show the electron mobility $\mu_n$ given in equation 2.15 as function of the electric field intensity $E$ for silicon, silicon carbide and, gallium nitride, respectively. As the electric field is increased, the mobility is reduced due to frequent collision between the carriers within the lattice. Thus, at higher electric field values, the mobility reduces. Careful consideration must be
made during the transistor design to ensure that the low-field constant mobility is achieved for constant current and voltages. Further discussion on this is made in Chapter 3.

2.1.7 Resistivity and Conductivity

Free electrons and holes results in conduction of electric current. The conductivity of intrinsic semiconductors is given by the following expression [13]

\[ \sigma_i = q\mu_n n_i, \]  
\[ \rho_i = \frac{1}{\sigma_i} = \frac{1}{q\mu_n n_i}, \]  

where \( \mu_n \) is the low-field mobility, \( q \) is the charge of the electron, and \( n_i \) is the intrinsic carrier concentration concentration of the intrinsic semiconductor. The conductivity of the semiconductors highly depends on temperature, since the intrinsic carrier concentration and the mobilities are a function of temperature as given in equations 2.3, 2.12, and 2.13. The charge carriers encounter more obstruction to move freely with increase in the temperature.
Hence, the mobility of charge carriers decreases as the temperature increases. On the other hand, the resistivity increases with rise in temperature.

Table 2.5 summarized the values of the resistivity of intrinsic Si, SiC, and GaN semiconductors at different temperatures. A complete range of values of $\rho_i$ can be observed from Figures 2.26, 2.27, and 2.28.

The resistivity of the semiconductor reduces with increase in the temperature. In contrast, in metals or any conductors, the resistivity increases with temperature. This inverse dependence of the resistivity on temperature is very critical, due to which semiconductor devices are preferred in power electronic circuits.

For an extrinsic semiconductor with a doping concentration $N_D$, the conductivity of the extrinsic semiconductor is given by

$$\sigma_n = q\mu_n N_D, \quad (2.19)$$

$$\rho_n = \frac{1}{\sigma_n} = \frac{1}{q\mu_n N_D}, \quad (2.20)$$

Figure 2.21: Average electron drift velocity $v_n$ as a function of electric field intensity $E$ for silicon carbide.
Figure 2.22: Average electron drift velocity $v_n$ as a function of electric field intensity $E$ for gallium nitride.

Figure 2.23: Electron mobility $\mu_n$ as a function of electric field intensity $E$ for silicon.
Figure 2.24: Electron mobility $\mu_n$ as a function of electric field intensity $E$ for silicon carbide.

Figure 2.25: Electron mobility $\mu_n$ as a function of electric field intensity $E$ for gallium nitride.
Table 2.5: Summary of resistivities $\rho_i$ at different temperatures for Si, SiC, and GaN

<table>
<thead>
<tr>
<th>Resistivity ($\Omega \cdot \text{cm}$)</th>
<th>Si</th>
<th>SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\rho_i$ at $T = 273$ K</td>
<td>$3.27 \times 10^7$</td>
<td>$1.67 \times 10^{27}$</td>
<td>$4.90 \times 10^{28}$</td>
</tr>
<tr>
<td>$\rho_i$ at $T = 300$ K</td>
<td>$2.53 \times 10^6$</td>
<td>$1.305 \times 10^{24}$</td>
<td>$2.90 \times 10^{25}$</td>
</tr>
<tr>
<td>$\rho_i$ at $T = 423$ K</td>
<td>$3.16 \times 10^3$</td>
<td>$1.21 \times 10^{16}$</td>
<td>$1.31 \times 10^{17}$</td>
</tr>
<tr>
<td>$\rho_i$ at $T = 523$ K</td>
<td>$0.11 \times 10^3$</td>
<td>$1.54 \times 10^{12}$</td>
<td>$1.18 \times 10^{13}$</td>
</tr>
<tr>
<td>$\rho_i$ at $T = 723$ K</td>
<td>$2.25$</td>
<td>$3.92 \times 10^7$</td>
<td>$2.01 \times 10^8$</td>
</tr>
<tr>
<td>$\rho_i$ at $T = 873$ K</td>
<td>$3.58 \times 10^{-1}$</td>
<td>$3.20 \times 10^5$</td>
<td>$1.37 \times 10^6$</td>
</tr>
<tr>
<td>$\rho_i$ at $T = 1023$ K</td>
<td>$9.42 \times 10^{-2}$</td>
<td>$1.54 \times 10^4$</td>
<td>$3.91 \times 10^4$</td>
</tr>
<tr>
<td>$\rho_i$ at $T = 1523$ K</td>
<td>$6.39 \times 10^{-3}$</td>
<td>$15.51$</td>
<td>$38.18$</td>
</tr>
<tr>
<td>$\rho_i$ at $T = 1873$ K</td>
<td>$2.55 \times 10^{-3}$</td>
<td>$9.22 \times 10^{-1}$</td>
<td>$2.49$</td>
</tr>
<tr>
<td>$\rho_i$ at $T = 2223$ K</td>
<td>$9.80 \times 10^{-4}$</td>
<td>$1.58 \times 10^{-1}$</td>
<td>$4.03 \times 10^{-1}$</td>
</tr>
</tbody>
</table>

One may observe that, the dependence of $\rho_n$ on temperature is only through the mobility $\mu_n$, while $N_D$ is constant. So, for any temperature less than the maximum junction temperature $T_{J_{\text{max}}}$, the resistivity of the extrinsic semiconductor can be controlled by the doping concentration. However, beyond $T_{J_{\text{max}}}$, the semiconductor loses its extrinsic properties and the resistivity follows equation 2.18. The values for $\rho_n$ can be calculated as follows. From Table 1, consider the mobility of Si as $\mu_n = 1360 \text{ cm}^2/\text{V} \cdot \text{s}$, mobility of SiC as $\mu_n = 900 \text{ cm}^2/\text{V} \cdot \text{s}$, and mobility of GaN as $\mu_n = 2000 \text{ cm}^2/\text{V} \cdot \text{s}$. Assume $N_D = 10N_J = 10 \times 5 \times 10^{15} \text{ cm}^{-3}$. Then the extrinsic resistivity are: for Si, $\rho = 0.918 \Omega \cdot \text{cm}$, for SiC, $\rho = 0.1.3872 \Omega \cdot \text{cm}$, and for GaN, $\rho = 0.6242 \Omega \cdot \text{cm}$. Comparing these values with those of the intrinsic resistivity given in Table 2.5, one may make the following conclusion. The extrinsic silicon semiconductor converts into an intrinsic semiconductor with conductive properties only at around 750 K ($= 473^\circ\text{C}$), the extrinsic silicon carbide semiconductor becomes intrinsic and a good conductor at around 1800 K ($= 1527^\circ\text{C}$), and the extrinsic gallium nitride semiconductor becomes intrinsic, however remains a semiconductor up to
Figure 2.26: Resistivity $\rho_i$ as a function of temperature $T$ for silicon.

around 2200 K ($= 1927 \, ^\circ\text{C}$).

Figure 2.27: Resistivity $\rho_i$ as a function of temperature $T$ for silicon carbide.
2.2 Figures-of-Merit for Semiconductor Materials

The operation of a power device in high-frequency applications highly depends on its material properties. It is demonstrated in [16] that high-frequency power devices should be fabricated based on the best material properties of semiconductors. The Figure of Merit (FOM) assists to justify the betterness of one semiconductor material over the other as well as determine the applicability of each material in any application. Three major figure-of-merits, namely Johnson’s FOM, Baliga’s FOM, and Keyes FOM are discussed here for the three semiconductor materials.

The Johnson’s figure-of-merit (JFOM) is one of the most important metrics used to determine the high-frequency and high-power performance of transistors [17]. The Johnson figure-of-merit takes into account the breakdown electric field $E_{BD}$, and saturated electron drift velocity $v_{sat}$ in defining a measure for the power handling capability at high frequencies. This figure-of-merit can be used to compare different transistor-types based on power on
Figure 2.29: Comparison of the three FOMs for Si, SiC and GaN semiconductor materials. The Johnson’s figure-of-merit is given as

\[ JFOM = \frac{E_{BD} \cdot v_{sat}}{2\pi}, \]  

where \( E_{BD} \) is the breakdown voltage for semiconductors and \( v_{sat} \) is the saturation velocity.

The Baliga figure-of-merit (BFOM) are used to determine the switching capabilities of transistors used in power electronic applications [16]. The BFOM uses the permittivity or the dielectric constant of the material \( \epsilon \), the band-gap energy \( E_g \), and the mobility \( \mu \) of the charge carriers. Since the BFOM depends on \( E_g \), characterization of the device performance based on temperature can also be performed. The BFOM assumes the low-frequency operation of transistors, where the power loss in the transistors is mainly due to the conduction loss and the switching loss is negligible. Baliga’s figure-of-merit is given as

\[ BFOM = \epsilon_o \cdot \epsilon_r \cdot \mu \cdot E_{BD}^3, \]  

where \( \mu \) is the electron mobility.
The Keyes figure-of-merit (KFOM) can be used for evaluating the performance of the transistors used in power electronic and integrated circuits [18]. The KFOM combines the effect of the material’s heat dissipation capability \( \lambda \) and the saturated drift velocity \( v_{\text{sat}} \) of the electrons. The saturated drift velocity of the electrons depends on various material properties such as geometry, mobility, and carrier concentration. Therefore, this figure-of-merit can be used to compare the transistor’s performance based on its thermal conductivity and its saturation velocity. The Keyes’s figure-of-merit is given as [18]

\[
KFOM = \lambda \sqrt{\frac{c \cdot v_{\text{sat}}}{4 \pi \epsilon}},
\]

(2.23)

where \( \lambda \) is the thermal conductivity of material and \( c \) is the velocity of light. Figure 2.29 shows the BFOM, KFOM, and JFOM for comparison of silicon, silicon carbide, and gallium nitride devices.
3 Characteristics of the Gallium Nitride Transistors

In this chapter, the characteristics of gallium nitride (GaN) transistors will be discussed using the physical properties of GaN discussed in Chapter 2. The characteristics of GaN field-effect transistor (FET) will be compared with the silicon and silicon carbide FETs. The differences in transistor properties, which makes GaN much promising as compared to its Si counterpart will be elaborated. The most important parameters for a transistor are the drain-to-source breakdown voltage $V_{BD}$, on-resistance $R_{DS(on)}$, and the threshold voltage $V_t$. The operating conditions of the power devices depend on these parameters, and the analysis of the same is the focus of this Chapter.

3.1 Operation of GaN Transistors

In this Section, the physical operation of the gallium nitride field effect transistors is discussed. Primarily, similar to silicon transistors, the GaN devices can also be categorized into (a) depletion mode (d-mode) and (b) enhancement mode (e-mode). While, the basic functions of the two modes remain the same, few critical differences exist in terms of the channel formation, reverse currents, and the electrical characteristics.

In the case of Si transistors, the channel required for the flow of electrons between the source and the drain terminals is created by application of electric field at the gate terminal. Consequently, by applying a positive charge at the drain terminal, the electrons are attracted towards the drain, while the holes (or actual current) move towards the source terminal. In essence, the width of the channel as well as its length is determined by the applied electric field; the main reason for such transistors to be termed as “field-effect transistors”.

3.1.1 2D Electron Gas

In GaN devices, the channel is formed in the form of a 2-dimensional electron gas (2DEG) layer. The 2DEG conduction layer is created due to the structural abnormalities, which results in the charge generation. As discussed in Chapter 2, the hexagonal structure of
Figure 3.1: The formation of 2DEG at the interface of GaN and AlGaN.

Figure 3.2: Electrical field is generated by applying voltage on the terminals of the device resulting in flow of electrical current.

gallium nitride leads to high conductivity. Strain is caused at the interface, when a thin layer of aluminum-gallium nitride (AlGaN) is grown on the GaN crystal. Application of electrical field at the interface induces a dense electron gas. This is called 2-dimensional electron gas (2DEG). The strain at the GaN/AlGaN junction decides the number of electrons in the gas. A large number of electrons confine near the interface of the GaN and AlGaN because of which the electron mobility is very high near the interface. Figure 3.1 shows the formation of 2DEG at the interface of GaN and AlGaN. This is the basis of high conductivity of GaN [8]. Figure 3.2 shows that an electrical field is generated by applying some potential on the terminals of the junction which results in flow of electrical current.
3.1.2 Depletion-Mode Structure of GaN FET

The depletion-mode field effect transistors (FET) are commonly termed as “normally ON” devices. In depletion-mode FET, the channel is conductive and high current flows between the drain and source with zero gate voltage \((V_{GS} = 0 \text{ V})\). Figure 3.3 shows the GaN FET with zero gate voltage. Electrons flow constantly between source and drain terminals until the 2DEG is depleted. In other words, a gate-to-source voltage is essential in order to deplete the 2DEG and turn the FET off. A negative bias at the gate of a n-channel device and a positive bias at the gate of a p-channel device reduces the electron flow in the channel. Conduction ceases by increasing the negative gate-to-source voltage until threshold voltage \((V_t)\) is reached. Since at zero gate-to-source voltage the electrons flow along the interface of GaN and AlGaN, the GaN FET is normally-on device. Figure 3.4 shows the GaN FET with a negative gate voltage.

3.1.3 Enhancement-Mode Structure of GaN FET

The enhancement-mode field effect transistors are commonly termed as “normally OFF” devices. In enhancement-mode FET, the channel is non-conductive, when the gate-to-source voltage \((V_{GS})\) is zero. Figure 3.5 shows the GaN FET with zero gate voltage. The current flows in the channel only when a gate-to-source voltage applied is higher than threshold voltage \(V_t\). A positive voltage at the gate of a n-type and a negative voltage at the gate of
p-type FET repels the holes away from the channel and let the electrons flow. By increasing the positive voltage at gate reduces the resistance of channel which in turn increases the conduction of current. Figure 3.6 shows the GaN FET with a positive gate voltage.

Enhancement-mode FETs are preferred over depletion-mode FETs because the channel is non-conducting at zero gate-to-source voltage unlike in depletion-mode where channel conducts at zero gate-to-source voltage. In depletion-mode transistors, a negative gate voltage must be applied to the device at times to keep it turned off, which makes its operation inconvenient. In order to make a depletion-mode FET work as an enhancement-
Depletion-mode or normally-on feature of GaN HEMT is usually not desirable in many applications due to less efficient, complicated, and expensive circuitry [19]. The driving voltage for depletion-mode GaN HEMT is negative. A normally-off silicon MOSFET can be cascoded in series with normally-on GaN HEMT to make it operate as normally-off. A very low voltage MOSFET is sufficient to turn the GaN transistor on at very high frequencies [20]. The cascode-configured depletion-mode GaN with enhancement-mode Si MOSFET is as shown in Figure 3.7. On applying the gate potential with a positive value, the drain-to-source voltage of the silicon MOSFET is negative and turns the d-mode GaN transistor ON. When the gate potential goes low, the drain-to-source voltage of the silicon MOSFET is positive and turns the d-mode GaN transistor OFF. Thus, the gate-drive circuitry controls the turn on/off of the silicon MOSFET. However, since the silicon-based transistors are limited to only few megahertz of operating frequency, the cascode d-mode GaN transistor becomes poor choice for high frequency applications.
Figure 3.7: Implementation of the cascode-configuration of depletion-mode gallium nitride FET with enhancement-mode silicon MOSFET.

### 3.2 Device Parameters

Several device parameters are used to characterize the different transistors. In this thesis, the two main device parameters, namely breakdown voltage and the on-resistance of the transistors are determined and its comparison with the silicon transistors is performed.

#### 3.2.1 Breakdown Voltage

The breakdown voltage in transistors depend on transistor geometry, structure, and breakdown electric field $E_{BD}$ of semiconductor material. The transistor breaks down above critical or breakdown electrical field. The breakdown electric field of GaN is much higher than that of Si which makes GaN devices withstand higher voltages. The breakdown voltage $V_{BD}$ is directly proportional to the critical electric field $E_{BD}$ and to the drift region width $w_d$ and can be approximated as [8]

$$V_{BD} \approx \frac{1}{2} w_d \cdot E_{BD}. \quad (3.1)$$

The drift region width can be expressed as

$$w_d = \frac{\varepsilon_r \varepsilon_0 E_{BD}}{qN_D}, \quad (3.2)$$
Silicon MOSFET

Figure 3.8: Size comparison of silicon and gallium nitride FET.

where $\epsilon_r$ is the relative permittivity of the material, $\epsilon_0$ is the absolute permittivity, $q$ is charge of electrons ($1.6 \times 10^{-19}$ C), and $N_D$ is the donor concentration. For GaN and Si transistors with the same breakdown voltage and equal doping concentration, the ratio of the drift region for silicon and gallium nitride FETs is given by

$$\frac{w_d(GaN)}{w_d(Si)} = \frac{E_{BD(Si)}}{E_{BD(GaN)}} = \frac{2 \times 10^5}{35 \times 10^5} \approx \frac{1}{18}.$$  \hfill (3.3)

For the same breakdown voltage, the width of drift region of GaN semiconductors can be significantly smaller than that of their Si counterparts, which notably reduces the size of GaN devices. Figure 3.8 shows the comparison of physical size of gallium nitride FET with silicon MOSFET. The reduced size of FET lowers the parasitic capacitance which in turn improves its switching speed. The high critical electric field allows GaN devices to operate at higher voltages and lower leakage currents.
3.2.2 On-Resistance of a Transistor

The on-resistance $R_{DS(on)}$ is the internal dc resistance offered by the FET in conducting state between the drain to source terminals i.e. with $V_{GS} > V_t$ for enhancement-mode and $V_{GS} = 0$ for depletion-mode. The on-resistance $R_{DS(on)}$ is a very important parameter of a device to decide the device’s operation. The resistance of the drift region is given as [13]

$$R_{dr} = \frac{w_d \times \rho_n}{A} = \frac{w_d}{q\mu_n N_D A}, \quad (3.4)$$

where $w_d$ is the width of the drift region, $\rho_n$ is the resistivity of the drift region, and $A$ is the area of the device. Also, the on-resistance can be expressed as the product of drift region resistance and area of the device as [13]

$$R_{DS(on)} = A \times R_{dr} = \frac{4V_{BD}^2}{\epsilon_o \epsilon_r \mu_n E_{BD}^3}. \quad (3.5)$$

The on-resistance $R_{DS(on)}$ of the power device is inversely proportional to the cube of the electrical breakdown and electron mobility, thus resulting in low conduction resistance. In other words, GaN devices have an on-resistance approximately 3 times lower than that of Si devices theoretically. Figures 3.9, 3.10 and 3.11 show the on-resistance $R_{DS(on)}$ as a function of breakdown voltage $V_{BD}$ for silicon, silicon carbide, and gallium nitride, respectively. From these figures, the magnitude of increase in the specific on-resistance of the different devices with variation in the breakdown voltage can be determined. For Si transistors, higher breakdown voltage results in a higher on-resistance. The resistance increases to the order few kΩ for devices with $V_{BD} \geq 10$ kV. In contrast, the SiC and GaN transistors exhibit very low on-resistances at these voltages. For SiC transistors, the on-resistance is approximately 20 Ω at a $V_{BD} = 10$ kV and is approximately 0.5 Ω at the same breakdown voltage for the GaN devices.

The on-resistance of drift region $w_d$ increases as the temperature rises. The following expression gives the specific-on resistance as a function of temperature as [13]

$$R_{DS(on)} = \frac{4V_{BD}^2}{\epsilon_o \epsilon_r \mu_n E_{BD}^3} \left( \frac{T}{300} \right)^{2.4}. \quad (3.6)$$
Figure 3.9: Plot of specific on-resistance $R_{DS(on)}$ as a function of breakdown voltage $V_{BD}$ for silicon.

Figure 3.10: Plot of specific on-resistance $R_{DS(on)}$ as a function of breakdown voltage $V_{BD}$ for silicon carbide.
Figure 3.11: Plot of specific on-resistance $R_{DS(on)}$ as a function of breakdown voltage $V_{BD}$ for gallium nitride.

Figures 3.12, 3.13 and 3.14 show the on-resistance $R_{DS(on)}$ as function of temperature $T$. This is an important characteristic since most of the electronic applications are subject to change in temperature. As can be seen from these figures, the resistance increases with increase in the temperature, which is an obvious effect similar to conductors. However, The magnitude of increment in the resistance is very minimal in the GaN transistors as opposed to the Si and SiC-based devices. Thus, the GaN transistors along with SiC-based devices are the best choices for high temperature applications.

3.2.3 On-Resistance of GaN Transistor

There are several resistive elements in the transistors which sum up to give the device’s on-resistance $R_{DS(on)}$ such as gate region, channel, and parasitic elements. $R_{DS(on)}$ varies with variation in temperature. Figure 3.15 shows the main resistances which give the $R_{DS(on)}$ of the transistor. The resistance of the 2DEG layer is given as [8]
Figure 3.12: Plot of specific on-resistance $R_{DS(on)}$ as a function of temperature $T$ for silicon transistors.

Figure 3.13: Plot of specific on-resistance $R_{DS(ON)}$ as a function of temperature $T$ for silicon carbide transistors.
Figure 3.14: Plot of specific on-resistance $R_{DS(on)}$ as a function of temperature $T$ for gallium nitride transistors.

$$R_{(2DEG)} = \frac{L_{(2DEG)}}{q\mu_{(2DEG)}N_{(2DEG)}W_{(2DEG)}},$$  \hfill (3.7)

where $\mu_{(2DEG)}$ is the mobility of electrons at the interface of GaN and AlGaN, $N_{(2DEG)}$ is the carrier concentration of electrons in 2DEG, $W_{(2DEG)}$ is the width of 2DEG, and $L_{(2DEG)}$ is the length of 2DEG. $R_{DS(ON)}$ of GaN HEMT can be expressed as

$$R_{DS(on)} = 2R_C + R_{(2DEG)} + R_P.$$  \hfill (3.8)

Due to the high concentration of electrons and high electron mobility at the GaN/AlGaN interface, GaN material makes excellent and attractive transistors. Next section discusses the performance measures for GaN, SiC, and Si devices in terms of figure-of-merit.

### 3.3 Static and Dynamic Characteristics of GaN FET

This section discusses the electrical characteristics of the gallium nitride field-effect transistor used in electronic applications. A commercially available transistor namely EPC2020 is
selected as the device-under-test. The transistor is rated to withstand a maximum voltage stress of 60 V and a maximum current stress of 40 A [8]. The device is capable of operating at frequencies as high as 15 MHz. The on-state resistance, parasitic capacitance, and the turn-off turn-off times are very small and is a suitable candidate for high-voltage, high switching frequency power electronic applications. First the dc analysis on this transistor is performed and then the ac analysis is conducted by considering the first-order capacitance model of the transistor.

3.3.1 DC Characteristics of GaN FET

The DC analysis of GaN FET is carried by utilizing EPC2020 GaN HEMT. Using SPICE model of EPC2020, the schematic shown in Figure 3.16 is simulated on SABER simulator. The value of the drain resistor $R_D = 10 \, \Omega$. The drain-to-source voltage $V_{DS}$ (or its power supply $V_{DD}$) is fixed and the gate-to-source voltage is varied from 0.5 V to 5 V. The drain current $i_D$ is plotted using the simulation tool and the activity is repeated for different values of $V_{DS}$. Figure 3.17 shows simulation results of the drain current as a function of the gate-to-source at different levels of $V_{DS}$. The threshold voltage $V_t$ is measured as approximately 1.5 V. The measured trans-conductance $g_m \approx 5 \, \text{A/V}$. It can be seen that all the curves saturate at $V_{GS} \approx 2 \, \text{V}$ due to the velocity saturation effect.
Figure 3.16: Circuit to analyze the DC characteristics of EPC2020 GaN HEMT.

The analysis is then performed to obtain the $i_D$ vs. $v_{DS}$ characteristics or the output characteristics of the EPC2020 e-mode GaN FET. The dc input voltage supply $V_{DD}$ is varied over from 0 to 3 V to observe the trend of the curve for different fixed values of the gate-to-source voltage $V_{GS}$. Figure 3.18 shows the drain current as a function of drain-to-source voltage at different fixed values of $V_{GS}$. At lower $V_{DS}$ values lower than $V_{GS}-V_t$, the transistor is in the linear mode and the drain-to-source conductance or the output trans-conductance $g_{ds}$ is approximately 500 $1/\Omega$. Thus, the drain-to-source resistance or the on-resistance can be estimated as $r_{ds} = 1/g_{ds} = 2 \text{ m}\Omega$. This value matches with that of the data-sheet provided in [8].

3.3.2 Small-Signal Model of GaN FET

The small-signal model is used to determine the frequency-domain characteristics of a device or a circuit. The small-signal characteristics are evaluated around pre-described DC operating point. Figure 3.19.a shows the symbol of a MOSFET along with its parasitic capacitances, namely gate-to-source capacitance $C_{gs}$, drain-to-source capacitance $C_{ds}$, and gate-to-drain capacitance $C_{gd}$. Figure 3.19.b shows the equivalent model of the MOSFET with $g_m$ as the small signal trans-conductance and $r_o$ as the output resistance. Figure 3.19.c shows the modified equivalent small-signal model obtained using Miller’s theorem.
Figure 3.17: Drain current $i_D$ as a function of gate-to-source $v_{GS}$ for different values of $V_{DS}$.

Figure 3.18: Drain current $i_D$ as a function of drain-to-source $v_{DS}$ for different values of $V_{GS}$.
Figure 3.19: Symbol and small-signal model of a transistor. (a) Symbol of transistor with parasitic capacitances. (b) Low-frequency small-signal model of the transistor. (c) Small-signal equivalent model obtained using Miller’s theorem with drain-to-source terminals short-circuited. (d) Small-signal equivalent model with lumped capacitances.
3.19.d shows the final modified small-signal with lumped capacitances.

The dynamic characteristics of enhancement-mode power transistor are evaluated using EPC2020 GaN HEMT. From the data-sheet of enhancement-mode power transistor EPC2020, the parasitic parameters obtained are given in Table 3.1.

The gate-to-source capacitance $C_{gs}$ is

$$C_{gs} = C_{iss} - C_{rss} = 1.8 - 0.031 = 1.769 \text{ nF}.$$  \hspace{1cm} (3.9)

The gate-to-drain capacitance $C_{gd}$ can be calculated using

$$C_{gd} = C_{rss} = 0.031 \text{ nF}.$$ \hspace{1cm} (3.10)

The drain-to-source capacitance $C_{ds}$ is

$$C_{ds} = C_{oss} - C_{rss} = 1.1 - 0.031 = 1.069 \text{ nF}.$$ \hspace{1cm} (3.11)

By assuming $g_m$ to be equal to 5 (A/V) and $R_D = 500 \Omega$ (section 3.3.1), transistor gain $A_{vo}$ can be expressed as

$$A_{vo} = -g_m \cdot R'_D,$$ \hspace{1cm} (3.12)

where $R'_D$ is the equivalent parallel resistance of $R_D || r_o$. Since $r_o \gg R_D$, $R'_D$ can be approximated as equal to $R_D$. Hence equation 3.12 can be written as

$$A_{vo} = -g_m \cdot R_D = -5 \times 500 = -2500.$$ \hspace{1cm} (3.13)

<table>
<thead>
<tr>
<th>Table 3.1: Properties of EPC2020</th>
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<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>----------------------------------</td>
</tr>
<tr>
<td>Input Capacitance $C_{iss}$</td>
</tr>
<tr>
<td>Output Capacitance $C_{oss}$</td>
</tr>
<tr>
<td>Reverse Transfer Capacitance $C_{rss}$</td>
</tr>
<tr>
<td>Gate Resistance $R_G$</td>
</tr>
<tr>
<td>Gate Charge $Q_G$</td>
</tr>
</tbody>
</table>
The equivalent capacitances $C_1$ and $C_2$ (see Figure 3.19.c), can be calculated as

$$C_1 = C_{gd}(1 - A_{vo}) = 0.031 \times [1 - (-2500)] = 77.53 \text{ nF}, \quad (3.14)$$

and

$$C_2 = C_{gd} \left(1 + \frac{1}{A_{vo}}\right) = 0.031 \times \left(1 + \frac{1}{650}\right) = 31.041 \text{ pF}. \quad (3.15)$$

Further, the input and output capacitances $C_i$ and $C_o$ (see Figure 3.19.d), can be calculated as

$$C_i = C_1 + C_{gs} = 79.29 \text{ nF}. \quad (3.16)$$

$$C_o = C_2 + C_{ds} = 1.1 \text{ nF}. \quad (3.17)$$

The poles of the transfer function due to the input and output capacitances can be calculated as follows

$$f_{p1} = \frac{1}{2\pi r_g C_i} = \frac{1}{2 \times \pi \times 0.3 \times 21.95 \times 10^{-9}} = 6.69 \text{ MHz}, \quad (3.18)$$

and

$$f_{p2} = \frac{1}{2\pi R'_D C_o} = \frac{1}{2 \times \pi \times 500 \times 1.1 \times 10^{-9}} = 289.36 \text{ kHz}. \quad (3.19)$$

Based on the above analysis, the small-signal voltage gain of the transistor is of the form

$$A_v = \frac{v_{ds}}{v_{gs}} \frac{g_m R'_D}{[s + (2\pi f_{p1})][s + (2\pi f_{p2})]}, \quad (3.20)$$

The magnitude and phase of the voltage gain $A_v$ are plotted as a function of frequency using MATLAB. The magnitude and phase plots are shown in figures 3.20 and figure 3.21, respectively. The dominant pole is at $f_{p2} = 289.36 \text{ kHz}$ and the unity-gain crossover frequency $f_T = 69.4 \text{ MHz}$. 

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Figure 3.20: Magnitude plot of the small-signal voltage gain $A_v$ of EPC2020 GaN HEMT.

Figure 3.21: Phase plot of the small-signal voltage gain $A_v$ of EPC2020 GaN HEMT.
4 Synchronous Buck Converter Using GaN Transistors

Various applications of gallium nitride (GaN) power devices are discussed in [21] - [27] in detail. DC-DC power converters are used in many applications such as power supplies for computers, telecommunication systems, portable applications, battery chargers, radio-frequency power amplifiers, and medical devices, etc. In these converters, the output voltage is regulated using the pulse-width modulation (PWM) technique. In PWM converters, the transistor behaves as a switch, which turns ON and OFF at a switching frequency $f_s$. The switching frequency depends on the material properties of the semiconductor. Because of high breakdown voltage and high carrier mobility, the GaN transistors can realize high switching frequency operation at low switching losses. In addition, the size of GaN transistors get smaller at high switching frequencies. Analysis of such properties can be performed on the circuit level. This chapter focuses on the analysis of the performance of GaN transistors in a PWM synchronous buck dc-dc converter operating at frequencies in the megahertz range. Detailed circuit operation, design, and performance evaluation of the GaN-based synchronous buck converter are presented in this Chapter.

4.1 PWM Synchronous Buck DC-DC Converter

In power converters, there is a high demand to increase the switching frequency and to reduce the size of the converter. Gallium nitride transistors are fully capable of fulfilling these objectives because of their outstanding material properties as mentioned in the

![Circuit diagram of the synchronous buck dc-dc converter.](image)

Figure 4.1: Circuit diagram of the synchronous buck dc-dc converter.
earlier chapters. In [25], 96% efficiency is achieved for dc-dc boost power converter using enhancement-mode GaN FET. The ability of GaN transistors in switched-capacitor circuits for high efficiency performance is well described in [26]. In [27], comparison of GaN transistors with silicon transistors are presented to evaluate the performance of LLC resonant converters. In this thesis, synchronous buck dc-dc converter with GaN transistors as switches is utilized for frequency and efficiency analysis.

4.1.1 Circuit Description

Figure 4.1 shows the circuit diagram of the synchronous buck dc-dc converter. The circuit consists of two power MOSFETs, an inductor, a capacitor, and a dc load resistor. As shown in Figure 4.1, $M_1$ and $M_2$ are the high-side and low-side MOSFETs, respectively, $L$ is the inductor, $C$ is the capacitor, and $R_L$ is the load resistor. The buck converter is a step-down converter. A pulse-width modulator controls both the transistors in complimentary fashion by turning the transistors ON and OFF at a switching frequency $f_s$ or a switching period $T = 1/f_s$. The operation of the PWM synchronous buck converter is explained in detail in [13]. For an ideal buck converter, the voltage transfer ratio $M_{V_{DC}}$ of the output voltage $V_O$ to the input voltage $V_I$ is the duty cycle $D$ given as $D = V_O/V_I$. The longer the switch must be kept ON, the higher is the required $D$. After a time interval $DT$, When the switch $M_1$ is closed, current flows through the inductor $L$ and charges it to feed the load resistance $R_L$. When the switch $M_1$ is turned OFF and low-side switch $M_2$ is turned ON to provide a path for the inductor to discharge its energy through the load. This operation ensures a continuous current flow to the load. Synchronous operation of buck converter is more efficient than the operation of conventional converter because replacing the diode with a MOSFET reduces the conduction losses.

4.1.2 Circuit Design

The following analysis considers the following assumptions:
The reactive components are ideal, i.e., their parasitic resistances do not vary with temperature and frequency.

- The converter is operating in steady state.

- The switching period \( T = 1/f_s \) is much shorter than the time constants of reactive components.

The average current through the inductor is equal to the current into the load. The ripple in the inductor current is the change in the current as the switches turn ON an OFF. The maximum inductor current ripple is

\[
\Delta i_{\text{Lmax}} = \frac{V_O(1 - D_{\text{min}})}{f_s L_{\text{min}}},
\]

where \( D_{\text{min}} \) is the minimum value of duty cycle, \( L_{\text{min}} \) is the minimum value of inductance required to keep the inductor current above zero and \( V_O \) is the output voltage of the buck converter.

The minimum inductance required for CCM operation is [13]

\[
L_{\text{min}} = \frac{V_O(1 - D_{\text{min}})}{2 f_s I_{\text{Omin}}} = \frac{R_{\text{Lmax}}(1 - D_{\text{min}})}{2 f_s}.
\]

The minimum value of capacitance is

\[
C_{\text{min}} = \max \left\{ \frac{D_{\text{max}}}{2 f_s r_C}, \frac{1 - D_{\text{min}}}{2 f_s r_C} \right\},
\]

where \( r_C \) is the parasitic resistance of the capacitor, \( D_{\text{min}} \) is the minimum value of the duty cycle, and \( D_{\text{max}} \) is the maximum value of duty cycle.

The dc voltage transfer function of the buck dc-dc converter is

\[
M_{\text{VDC}} = \frac{V_O}{V_I} = D.
\]

In reality, the components are imperfect and exert detrimental effect on the circuit operation. Hence, for a lossy converter the equation (4.4) becomes

\[
M_{\text{VDC}} = \frac{V_O}{V_I} = \eta D.
\]
In equation 4.5, $\eta$ is the efficiency and is expressed as

$$
\eta = \frac{N_\eta}{D_\eta}, 
$$

(4.6)

where

$$
N_\eta = 1 + M_{VDC} \left( \frac{r_C R_L}{6 f_s^2 L^2} - \frac{r_{DS1} - r_{DS2}}{R_L} \right) 
$$

$$
+ \left\{ \left[ 1 + M_{VDC} \left( \frac{r_C R_L}{6 f_s^2 L^2} - \frac{r_{DS1} - r_{DS2}}{R_L} \right) \right]^2 
$$

$$
- \frac{M_{VDC}^2 r_C R_L}{3 f_s^2 L^2} \left( 1 + \frac{r_{DS2} + r_L}{R_L} \right) 
$$

$$
- \frac{M_{VDC}^2 r_C R_L}{3 f_s^2 L^2} \left( \frac{f_s C_o R_L}{M_{VDC}^2} + \frac{r_C R_L}{12 f_s^2 L^2} \right)^\frac{1}{2}, 
$$

(4.7)

$$
D_\eta = 2 \left( 1 + \frac{r_{DS2} + r_L}{R_L} + \frac{f_s C_o R_L}{M_{VDC}^2} + \frac{r_C R_L}{12 f_s^2 L^2} \right), 
$$

(4.8)

where $r_L$ is the equivalent series resistance (ESR) of the inductor, $r_{DS1}, r_{DS2}$ are the on-state resistances of the high-side and low-side transistors, respectively, $D$ is the duty cycle, $R_L$ is the load resistance, $r_C$ is the ESR of the capacitor, $V_O$ is the output voltage, $f_s$ is the switching frequency, and $C_{o1}, C_{o2}$ are the output capacitances of the MOSFET. From equation (4.6) it can be seen that the efficiency of the converter depends on the switching frequency.

The voltage and current stresses of the transistors are expressed as

$$
V_{SM_{max}} = V_{I_{max}}, 
$$

(4.9)

and

$$
I_{SM_{max}} = I_{O_{max}} + \frac{V_O (1 - D_{min})}{2 f_s L}. 
$$

(4.10)

The following section presents a design example and the required components and their values are estimated. Also, component selections are made based on the predicted current and voltage stresses, which is a starting point for the simulations.
Table 4.1: Minimum inductance and capacitance values for the designed synchronous buck dc-dc converter

<table>
<thead>
<tr>
<th>$f_s$ (kHz)</th>
<th>Inductance $L_{min} , (\mu H)$</th>
<th>Capacitance $C_{min} , (\mu F)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>28.0612</td>
<td>61.1111</td>
</tr>
<tr>
<td>1</td>
<td>2.8061</td>
<td>6.1111</td>
</tr>
<tr>
<td>10</td>
<td>0.2806</td>
<td>0.6111</td>
</tr>
<tr>
<td>15</td>
<td>0.1871</td>
<td>0.4074</td>
</tr>
</tbody>
</table>

### 4.1.3 Design Example

A synchronous buck dc-dc converter is designed for the following specifications: input voltage $V_I = 12 \, \text{V}$, output voltage $V_O = 6 \, \text{V}$, minimum output current $I_{Omin} = 0.7 \, \text{A}$, maximum output current $I_{Omax} = 1.5 \, \text{A}$, and maximum output power $P_{Omax} = 9 \, \text{W}$. The reactive component values are estimated at different switching frequencies. The minimum values of the inductance and the capacitance at different selected frequencies obtained using equations (4.2) and (4.3) are given in Table 4.1. The duty cycle is

$$D = \frac{V_O}{V_I} = \frac{6}{12} = 0.5 \quad (4.11)$$

The converter is designed to operate in the continuous-conduction mode and its analysis in the discontinuous-conduction mode is not within the scope of this thesis.

Using the expressions for the voltage stress, it can be found that $V_{SM_{max}} = 12 \, \text{V}$ and

![Figure 4.2: Circuit schematic for dc-dc synchronous buck converter on SABER circuit simulator](image-url)
the maximum current stress occurs at the lowest switching frequency given by

\[ I_{SM\text{ max}} = 1.5 + \frac{6 \times (1 - 0.5)}{2 \times 100 \times 10^3 \times 28.06 \times 10^{-6}} = 2.03 \text{ A} \quad (4.12) \]

In this thesis, the EPC2020 enhancement-mode GaN power field-effect transistor by Efficient Power Conversion [8] is realized as the perfect candidate, which is capable of withstanding the predicted voltage and current stresses given above. The maximum drain-to-source voltage for EPC2020 is \( V_{DSM\text{ (max)}} = 60 \text{ V} \), the maximum drain current is \( I_{DM\text{ (max)}} = 60 \text{ A} \), and on-resistance \( r_{DS} = 2 \text{ m} \Omega \). The different specifications of EPC2020 are given in [8] in detail. The output capacitance \( C_o \) of EPC2020 is equal 1.069 nF. Due to such a low value of the output capacitance, its transient response is very high leading to efficient operation at high switching frequencies. The switching losses of this transistor are also very small. A few of the applications of EPC2020 include high-frequency dc-dc conversion, rectification, and audio-amplifiers.

The Spice model EPC2020 was procured from the manufacturers website [8] and converted to use with SABER circuit simulation software. Circuit simulations are performed for the synchronous buck converter at different switching frequencies in order to evaluate the its efficiency and power losses. The following section presents the simulation results for synchronous buck converter using EPC2020 GaN transistor for different frequencies and one test case with silicon MOSFET for comparison. Figure 4.3 shows the plot of efficiency as a function of frequency.

Before the validation is made through simulation, a theoretical plot of the variation in the efficiency as a function of the switching frequency can be observed. Let us assume the following values for the parasitic components and are equal for all the frequencies:
\( r_L = 0.11 \text{ Ohm} \), \( r_C = 0.02 \), \( r_{DS1} = r_{DS2} = 2 \text{ m} \Omega \), and \( C_{o1} = C_{o2} = 1.069 \text{ nF} \). Then using equation 4.6, the overall efficiency as a function of the switching frequency varies as shown in Figure 4.3.
Figure 4.3: Theoretically obtained plot of efficiency as a function of switching frequency for the synchronous buck dc-dc converter.

Figure 4.4: Simulation results of gate-to-source voltage $v_{GS}$ and drain-to-source voltage $v_{DS}$ for switch $M_1$ at 100 kHz.
4.1.4 Simulation Results

The intention of this section is to determine the switching frequency limits on the EPC2020 transistor, when used in the synchronous buck converter for the given specifications. It must be noted that these results may differ once the specifications are changed. For example, the switching frequency limit may be increased, when the output voltage and output power levels are very small or the limit decreased when the output power is very high. It is envisaged that the waveforms of the gate-to-source voltage, drain-to-source voltage, and the drain current of the transistors are very good indicators of the normal operation of the converter. Any deviation from the normal shapes of the waveforms, can be treated as the break point, beyond which proper and efficient operation of the converter becomes questionable.

Figure 4.2 shows the schematic of the synchronous buck dc-dc converter constructed on SABER circuit simulator. The circuit is simulated at frequencies of 100 kHz, 1 MHz, 10 MHz, and 15 MHz. Simulation results of the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOSFET $M_1$ and $M_2$ are recorded for all the frequencies mentioned above.
In addition, the inductor current $i_L$, output voltage $V_O$, input power $P_I$, and output power $P_O$ are also obtained. Efficiency is measured at each frequency.

1. **Simulation Results at 100 kHz:**

   Figure 4.4 shows the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOS-FET $M_1$ at 100 kHz. Figure 4.5 shows the gate-to-source voltage $v_{GS}$, drain-to-source
Figure 4.8: Simulation results of gate-to-source voltage $v_{GS}$ and drain-to-source voltage $v_{DS}$ for MOSFET $M_1$ at 1 MHz.

voltage $v_{DS}$ for MOSFET $M_2$ at 100 kHz. Figure 4.6 shows the inductor current $i_L$ and output voltage $V_O$ at frequency of 100 kHz. One may confirm that the operation of the converter at this switching frequency provides the voltage and current waveforms, which can be considered as benchmark waveforms for the other cases. Apart from the conduction losses, the switching losses at this frequency is usually very low. The inductor current is in continuous conduction mode and the output voltage is 6 V as expected. From the simulation results the efficiency is measured to be 99.8%, a a strong feature of the synchronous buck converters.

2. Simulation Results at 1 MHz:

Figure 4.8 shows the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOSFET $M_1$, Figure 4.9 shows the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOSFET $M_2$ and Figure 4.10 shows the inductor current $i_L$ and output voltage $V_O$ at a switching frequency of 1 MHz. The shapes of the waveforms are similar to the 100 kHz situation. At this frequency, the switching losses are higher than that of the 100 kHz case. The effect of the parasitic capacitance becomes significant at this
Figure 4.9: Simulation results of gate-to-source voltage $v_{GS}$ and drain-to-source voltage $v_{DS}$ for MOSFET $M_2$ at 1 MHz.

Figure 4.10: Simulation results of inductor current $i_L$ and output voltage $V_O$ at 1 MHz.

frequency. The efficiency at this frequency was recorded as 97%.

3. Simulation Results at 10 MHz:

Figure 4.12 shows the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOSFET $M_1$, Figure 4.13 shows the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOSFET $M_2$, and Figure 4.14 shows the inductor current $i_L$ and output
Figure 4.11: Simulation results of input power $P_I$ and output power $P_O$ at 1 MHz.

Figure 4.12: Simulation results of gate-to-source voltage $v_{GS}$ and drain-to-source voltage $v_{DS}$ for MOSFET $M_1$ at 10 MHz.

voltage $V_O$ at frequency of 10 MHz. The shapes of the waveforms are retained to a certain degree at this switching frequency. However, the gate-to-source voltage and the drain-to-source voltage exhibit lower rise and fall times. This is mainly due to the effect of the output capacitance of the transistors, which require sufficient time to discharge. The efficiency of the converter at this frequency is around 81.4%. One may
Figure 4.13: Simulation results of gate-to-source voltage $v_{GS}$ and drain-to-source voltage $v_{DS}$ for MOSFET $M_2$ at 10 MHz.

Figure 4.14: Simulation results of inductor current $i_L$ and output voltage $V_O$ at 10 MHz.

conclude that a switching frequency of 10 MHz is where the transistor performance begins to drastically reduce, keeping in view the specifications of the converter. It can be predicted that the current and voltage waveforms of the switches beyond this frequency no longer indicates the normal behavior of the transistor.
4. Simulation Results at 15 MHz:

Figure 4.16 shows the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOSFET $M_1$ at 15 MHz. Figure 4.17 shows the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOSFET $M_2$ at 15 MHz. Figure 4.18 shows the inductor current $i_L$ and output voltage $V_O$ at frequency of 15 MHz. It can be seen that
the waveforms of the gate-to-source voltage $v_{GS}$, and drain-to-source voltage $v_{DS}$ of both the switches are distorted at 15 MHz. The inductor current is in continuous conduction mode and the output voltage is 6 V as expected. However, the efficiency is measured to be 70.99%, which is very poor as compared to the efficiencies calculated in previous cases of low frequencies. The switching loss are very high resulting in a
reduced efficiency. The switching loss is expressed as [13]

\[ P_{SW} = f_s C_O V_I^2, \]  \hspace{1cm} (4.13)

where \( f_s \) is the switching frequency and \( C_o \) is output capacitance of a transistor, which is assumed to be linear. Any further increase in frequency causes the transistor to breakdown. It is concluded that EPC2020 GaN transistor can operate at high frequencies. However, an operation beyond 10 MHz is not recommended. The following section presents the simulation results for synchronous buck converter using IRF540 silicon MOSFET.

5. Simulation Results for Synchronous Buck Converter with Silicon MOSFETs at 5 MHz:

Similar set of simulation results are obtained for the synchronous buck converter with silicon MOSFETs. The GaN transistors are replaced by the already-available Spice models of IRF540. The activity is repeated and the different results are obtained as discusses below. Figure 4.20 shows the gate-to-source voltage \( v_{GS} \), drain-to-source voltage \( v_{DS} \) for silicon MOSFET \( M_1 \), and Figure 4.21 shows the gate-to-source voltage
Figure 4.20: Simulation results of gate-to-source voltage $v_{GS}$ and drain-to-source voltage $v_{DS}$ for silicon MOSFET $M_1$ at 5 MHz.

Figure 4.21: Simulation results of gate-to-source voltage $v_{GS}$ and drain-to-source voltage $v_{DS}$ for silicon MOSFET $M_2$ at 5 MHz.

$v_{GS}$, drain-to-source voltage $v_{DS}$ with silicon MOSFET $M_2$ at 5 MHz. Figure 4.22 shows the inductor current $i_L$ and output voltage $V_O$, and Figure 4.23 shows the input power $P_I$ and output power with silicon MOSFET $P_O$ at 5 MHz.

It can be seen that the waveforms of the drain-to-source voltage $v_{DS}$ of both the
switches are completely distorted at 5 MHz. The output voltage is reduced to 5.5 V. Also, the efficiency of the converter is measured to be 48%, which is far less than the efficiency of the converter with GaN transistor at the even higher frequencies. This proves that silicon transistors are bad choices for high-frequency converters.
5 Half-Bridge Class-D Series Resonant Inverter Using GaN Transistor

High-frequency and high-power application requirements are based on characteristics of transistors. High-frequency operation of transistors depends on semiconductor material. Semiconductor materials with wide-band gap, which results in high breakdown voltage and high electron velocity can achieve high-frequency operation. Resonant inverters are used in variety of applications including dc-dc resonant converters, radio-frequency power transmitters, electronic ballasts, and fiber-optics production etc [28]. The performance of these inverters is highly affected by the characteristics of the transistors. Low on-resistance of transistors reduces the conduction losses, yielding high efficiency. Due to low on-resistance, high carrier concentration, and low capacitance gallium nitride FET offers fast switching and high efficiency performance. This chapter presents an application of GaN based transistors in class-D resonant inverter.

5.1 Class-D Resonant Inverter

A few of the many applications of class-D resonant inverters include wireless power charging, induction heating, motor-drives, and isolated power converters. Operation at high switching frequency to achieve high efficiency with low switching losses is in increasing demand.

![Circuit diagram of half-bridge Class-D series resonant inverter.](image)
The low output capacitance and low reverse recovery charge allow the transistors higher switching frequency and lower switching loss. Resonant inverter converts a DC voltage into a sinusoidal voltage, which provides ac power to a load. The GaN transistors are capable of achieving high power density, show the benefits of higher efficiency in resonant inverters [27]. In this thesis work, Class-D resonant inverter with GaN transistor as a switch is utilized for frequency and efficiency analysis.

5.1.1 Circuit Description

Figure 5.1 shows the circuit of Class-D half-bridge series resonant inverter. The circuit consists of two transistors $M_1$ and $M_2$, an inductor $L_R$, a capacitor $C_R$, and a load resistor $R$. The transistors behave as switches and turn ON and OFF alternatively at a switching frequency $f_s$. The input voltage at the series-resonant circuit is the voltage across the switch $M_2$, which is square-wave of magnitude equal to the input voltage $V_I$. The operation of the Class-D half-bridge series resonant inverter is explained in details in [28]. The switch in synchronous class-D can conduct positive or negative current. For operating frequency higher or lower than resonance frequency, the current flows through the anti-parallel diode. Cross-conduction or shoot-through occurs if drain-to-source voltages $v_{GS}$ for switch $M_1$ and $M_2$ overlap. Very high current spikes due to cross-conduction can cause device failure. To prevent this condition, dead time between the ON and OFF states of both switches can be provided.

5.1.2 Circuit Design

The following assumptions are made for the analysis of Class-D inverter:

- The loaded quality factor of series resonance circuit is high to ensure the sinusoidal shape of current through the resonant circuit.
- The operation of Class-D is above resonance.
The resonant frequency of the series resonant circuit is

$$\omega_0 = \frac{1}{\sqrt{LC}}. \quad (5.1)$$

The loaded quality factor is expressed as

$$Q_L = \frac{\omega_o L}{R + r} = \frac{1}{\omega_o C(R + r)}, \quad (5.2)$$

where

$$r = r_{DS} + r_L + r_C; \quad (5.3)$$

and $r_{DS}$, $r_L$, and $r_C$ are the parasitic resistances of the transistor, inductor, and capacitor, respectively. The resonant inductance is

$$L = \frac{Q_L(R + r)}{\omega_o}. \quad (5.4)$$

The resonant capacitance is

$$C = \frac{1}{\omega_o Q_L(R + r)}. \quad (5.5)$$

The efficiency of the Class-D inverter is

$$\eta = \frac{P_O}{P_O + P_L}, \quad (5.6)$$

where $P_O$ is the output power and $P_L$ is the total power loss in the Class D inverter. For above resonance i.e $f_s > f_o$, (where $f_s$ is switching frequency and $f_o$ is the resonant frequency), the power loss is expressed as

$$P_L = 2P_{rDS} + P_{rL} + P_{rC} + 2P_{SWoff} + 2P_G, \quad (5.7)$$

where $P_{rDS}$ is the conduction loss in each transistor, $P_{rL}$ is the conduction loss in the inductor, $P_{rC}$ is the conduction loss in the capacitor, $P_{SWoff}$ is the turn-off switching loss, and $P_G$ is the gate-drive power loss in the MOSFETs.

The turn-off switching power loss $P_{SWoff}$ is expressed as

$$P_{SWoff} = f_s V_I I_{off} \left( \frac{t_r}{3} + \frac{t_f}{2} \right), \quad (5.8)$$
where $I_{OFF}$ is the switch current through $M_2$ during rise time, $t_r$, and $t_f$ are the switch current rise and fall times, respectively. Also the gate-drive power loss $P_G$ is expressed as

$$P_G = 2f_sQ_gV_{GSPP}, \quad (5.9)$$

where $Q_g$ is the gate charge of each MOSFET and $V_{GSPP}$ is the peak-to-peak (or maximum) value of the gate-to-source voltage $v_{GS}$. The voltage and current stresses of the transistors are expressed as

$$V_{DSM \text{max}} = V_I = \frac{2}{\pi}V_m, \quad (5.10)$$

and

$$I_{DSM \text{max}} = I_m = \pi I_f. \quad (5.11)$$

### 5.1.3 Design Example

A Class-D half-bridge series resonant inverter is designed for the following specifications: input voltage $V_I = 12$ V, output power $P_O = 10$ W, and loaded quality factor $Q_L = 5.5$. The switching frequency $f_s$ is varied as 100 kHz, 1 MHz, 10 MHz, and 15 MHz. According to [24], high efficiency can be achieved if operating frequency of Class-D dc-dc series resonant converter is higher than resonant frequency. Hence, the circuit is simulated at operating frequency higher than resonant frequency. The values of components for the resonant circuit are calculated ensuring the operation above resonance and given in Table 5.1. In this thesis, the EPC2020 enhancement-mode GaN power field-effect transistor by Efficient Power Conversion [8] is realized as the perfect candidate, which is capable of withstanding the predicted voltage and current stresses given above. The maximum drain-to-source voltage

<table>
<thead>
<tr>
<th>$f_s$</th>
<th>Inductance $L$ ($\mu$H)</th>
<th>Capacitance $C$ (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 kHz</td>
<td>27.5867</td>
<td>110.1849</td>
</tr>
<tr>
<td>1 MHz</td>
<td>2.75867</td>
<td>11.01849</td>
</tr>
<tr>
<td>5 MHz</td>
<td>0.5517</td>
<td>2.2037</td>
</tr>
<tr>
<td>10 MHz</td>
<td>0.2759</td>
<td>1.1018</td>
</tr>
<tr>
<td>15 MHz</td>
<td>0.1839</td>
<td>0.7346</td>
</tr>
</tbody>
</table>
for EPC2020 is $V_{DSM(max)} = 60$ V, the maximum drain current is $I_{DM(max)} = 60$ A, and on-resistance $r_{DS} = 2$ mΩ. The different specifications of EPC2020 are given in [8] in detail.

The output capacitance $C_o$ of EPC2020 is equal 1.069 nF. Due to such a low value of the output capacitance, its transient response is very high leading to efficient operation at high switching frequencies. The switching losses of this transistor are also very small. A few of the applications of EPC2020 include high-frequency dc-dc conversion, rectification, and audio-amplifiers.

The Spice model EPC2020 was procured from the manufacturers website [8] and converted to use with SABER circuit simulation software. Circuit simulations are performed for the synchronous buck converter at different switching frequencies in order to evaluate the its efficiency and power losses. The following section presents the simulation results for synchronous buck converter using EPC2020 GaN transistor for different frequencies and one test case with silicon MOSFET for comparison. Figure 4.3 shows the plot of efficiency as a function of frequency. Before the validation is made through simulation, a theoretical plot

Figure 5.2: Circuit schematic for Half-Bridge Class-D RF power amplifier in SABER simulator.
of the variation in the efficiency as a function of the switching frequency can be observed.

Let us assume the following values for the parasitic components and are equal for all the frequencies: $r_L = 0.11 \, \Omega$, $r_C = 0.02$, $r_{DS1} = r_{DS2} = 2 \, \text{m}\Omega$, and $C_{o1} = C_{o2} = 1.069 \, \text{nF}$. From equation 5.6 it can be seen that the efficiency of the converter depends on the switching frequency. Figure 5.3 shows the plot of efficiency as a function of frequency.

### 5.1.4 Simulation Results

Figure 5.2 shows the circuit of Class-D half-bridge series resonant inverter in SABER circuit simulator. The circuit is simulated at the frequencies of 100kHz, 1MHz, 10MHz, and 15MHz. Simulation results for gate-to-source voltage $V_{GS}$, drain-to-source voltage $V_{DS}$, and drain current $i_D$, for MOSFET $M_1$ and $M_2$ are obtained. In addition, input and output power waveforms are plotted. Efficiency is measured at each frequency operation.
1. Simulation Results at 100 kHz:

Figure 5.4 shows the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOSFET $M_1$, Figure 5.5 shows the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOSFET $M_2$, Figure 5.6 shows the drain current $i_D$ through the MOSFETs $M_1$
Figure 5.6: Simulation results of drain current $i_D$ for switch $M_1$ and $M_2$ at 100 kHz.

Figure 5.7: Simulation results of input power $P_I$ and output power $P_O$ at 100 kHz.

and $M_2$ at frequency of 100 kHz, and Figure 5.7 shows the input power $P_I$ and output power $P_O$ at a switching frequency of 100 kHz. It can be seen that the waveforms of the gate-to-source voltage $v_{GS}$ and drain-to-source voltage $v_{DS}$ of both the switches are very close to the ideal case at 100 kHz. The peaks in the drain current of both switches are due to cross-conduction in the transistors and can be eliminated by pro-
Diagram showing waveforms of gate-to-source voltage $v_{GS}$ and drain-to-source voltage $v_{DS}$ for switch $M_1$ at 1 MHz.

2. Simulation Results at 1 MHz:

Figure 5.8 shows the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOSFET $M_1$, Figure 5.9 shows the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOSFET $M_2$, Figure 5.10 shows the drain current $i_D$ through the MOSFETs $M_1$ and $M_2$, Figure 5.11 shows the input power $P_I$ and output power $P_O$ at a switching frequency of 1 MHz. The gate-to-source voltage $v_{GS}$ and drain-to-source voltage $v_{DS}$ of both the switches reflect normal operating conditions at this frequency. From the simulation results the efficiency is measured to be 92%. 

viding appropriate dead times. From the simulation results the efficiency is measured to be 93.2%. The efficiency was estimated by considering the ratio of the average values of the output to the input power. At this frequency, the switching losses are low.

Figure 5.8: Simulation results of gate-to-source voltage $v_{GS}$ and drain-to-source voltage $v_{DS}$ for switch $M_1$ at 1 MHz.
3. Simulation Results at 10 MHz:

Figure 5.12 shows the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOSFET $M_1$, Figure 5.13 shows the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOSFET $M_2$, Figure 5.14 shows the drain current $i_D$ through the MOS-
Figure 5.11: Simulation results of input power $P_I$ and output power $P_O$ at 1 MHz.

Figure 5.12: Simulation results of gate-to-source voltage $v_{GS}$ and drain-to-source voltage $v_{DS}$ for switch $M_1$ at 10 MHz.

FETs $M_1$ and $M_2$, and Figure 5.15 shows the input power $P_I$ and output power $P_O$ at a switching frequency of 10 MHz. It can be seen that, while the gate-to-source voltage waveform $v_{GS}$ has retained its shape, the drain-to-source voltage waveform $v_{DS}$ shows a lower fall time due to slower discharge time of the output capacitance. High peaks are observed in drain current of both switches, causing switching losses.
From the simulation results, the efficiency is measured to be 65.3%.

4. Simulation Results at 15 MHz:

Figure 5.16 shows the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOSFET $M_1$, Figure 5.17 shows the gate-to-source voltage $v_{GS}$, drain-to-source volt-
Figure 5.15: Simulation results of input power $P_I$ and output power $P_O$ at 10 MHz.

Figure 5.16: Simulation results of gate-to-source voltage $v_{GS}$ and drain-to-source voltage $v_{DS}$ for switch $M_1$ at 15 MHz.

Figure 5.18 shows the drain current $i_D$ through the MOSFETs $M_1$ and $M_2$, and Figure 5.19 shows the input power $P_I$ and output power $P_O$ at a switching frequency of 15 MHz. It can be observed that the waveforms of the gate-to-source voltage $v_{GS}$, and drain-to-source voltage $v_{DS}$ of both the switches totally distorted and the operation of the inverter at this frequency is inappropriate. High
Figure 5.17: Simulation results of gate-to-source voltage $v_{GS}$ and drain-to-source voltage $v_{DS}$ for switch $M_1$ at 15 MHz.

Figure 5.18: Simulation results of drain current $i_D$ for switch $M_1$ and $M_2$ at 15 MHz.

peaks are observed in drain current of both switches. From the simulation results the efficiency is measured to be 45.75%. It is concluded that EPC2020 GaN transistor can operate at high frequencies. However, an operation beyond 10 MHz is not recommended. The following section presents the simulation results for synchronous buck converter using IRF540 silicon MOSFET.
5. Simulation Results with Silicon MOSFETs at 5 MHz:

Similar set of simulation results are obtained for the Class-D series resonant inverter with silicon MOSFETs. The GaN transistors are replaced by the already-available Spice models of IRF540. The activity is repeated and the different results are obtained as discusses below.

Figure 5.20 shows the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOSFET $M_1$, Figure 5.21 shows the gate-to-source voltage $v_{GS}$, drain-to-source voltage $v_{DS}$ for MOSFET $M_2$, Figure 5.22 shows the inductor current $i_L$ and output voltage $V_O$, and Figure 5.23 shows the input power $P_I$ and output power $P_O$ at a switching frequency of 5 MHz. It can be seen that the waveforms of the drain-to-source voltage $v_{DS}$ of both the switches are completely distorted at 5 MHz. Also, the efficiency of the converter is measured to be 41.84%, which is far less than the efficiency of the converter with GaN transistor at the even higher frequencies. This proves that silicon transistors are bad choices for high-frequency converters.
Figure 5.20: Simulation results of gate-to-source voltage $v_{GS}$ and drain-to-source voltage $v_{DS}$ with silicon MOSFET $M_1$ at 5 MHz.

Figure 5.21: Simulation results of gate-to-source voltage $v_{GS}$ and drain-to-source voltage $v_{DS}$ with silicon MOSFET $M_2$ at 5 MHz.
Figure 5.22: Simulation results of drain current $i_D$ with silicon MOSFETs $M_1$ and $M_2$ at 5 MHz.

Figure 5.23: Simulation results of input power $P_I$ and output power $P_O$ with silicon MOSFETs at 5 MHz.
6 Results

6.1 Summary of Results

• The material properties of gallium nitride (GaN) have been analyzed in detail and compared with silicon (Si) and silicon carbide (SiC) semiconductor materials in Chapter 2. Few important results are discussed in this Chapter in Section 6.2.

• The device properties of GaN, SiC, and Si have been analyzed in great depth in Chapter 3 and compared with those of Si and SiC. The results are discussed in Section 6.3.

• The performance of the GaN-based transistors in PWM synchronous buck dc-dc converters was evaluated in Chapter 4. The theoretically predicted and simulation results are validated through experiments and the results are presented in Section 6.4.

• The performance of the GaN-based transistors in Class-D resonant inverters was evaluated in Chapter 5. The theoretical and simulation results are presented in this Chapter in Section 6.5.

6.2 Comparison of Material Properties of Gallium Nitride, Silicon Carbide, and Silicon

Figure 6.1 shows the plots of intrinsic carrier concentration $n_i$ of gallium nitride, silicon carbide, and silicon as functions of temperature $T$. At room temperature, the intrinsic carrier concentration $n_i$ for GaN is very low, when compared to that of Si. The values indicate that almost no free electron is available for conduction in the GaN semiconductor at room temperature, making it a good insulator. The difference in carrier concentration of GaN and SiC is relatively low due to similar values of the band gap energy.

At any temperature, the electron mobility of GaN is very high, when compared to Si. Figure 6.2 shows the plot of electron mobility $\mu_n$ of gallium nitride, silicon carbide, and silicon as a function of temperature $T$. The movement of charges takes place in confined
Figure 6.1: Intrinsic carrier concentration $n_i$ as functions of temperature $T$ for gallium nitride, silicon carbide, and silicon.

layers of the 2-dimensional electron gas (2-DEG). The conductivity of this layer is very high and increases with increase in temperature. Thus, GaN semiconductors are a great choice for high-speed applications resulting in compact transistor size.

The low electric-field drift electron velocity is directly proportional to the electric field intensity $E$ and saturates at high electric field values. Saturation drift electron velocity is higher for GaN as compared to Si. Figure 6.3 shows the plot of drift electron velocity $\mu_n$ of gallium nitride, silicon carbide, and silicon as functions of electric field intensity $E$.

6.3 Comparison of Device Properties of Gallium Nitride, Silicon Carbide, and Silicon

Silicon MOSFETs have a high $R_{DS(on)}$ over a unit area. A large die size is required to achieve a low $R_{DS(on)}$. The $R_{DS(on)}$ is directly proportional to the breakdown voltage $V_{BD}$. As the die area gets bigger, the on-resistance increases proportionally to the breakdown voltage. Hence, for a specific $V_{BD}$ and die size, the $R_{DS(on)}$ of a GaN FET will be less than that of the Si MOSFET. Figure 6.4 shows the on-resistance of GaN, SiC, and Si transistors as
Figure 6.2: Electron mobility $\mu_n$ as functions of temperature $T$ for gallium nitride, silicon carbide, and silicon.

Figure 6.3: Drift electron velocity $\mu_n$ as functions of electric field intensity $E$ for gallium nitride, silicon carbide, and silicon.

a function of breakdown voltage. Specific on-resistance increases with increase in junction temperature. Figure 6.5 shows, the variation in on-resistance $R_{DS(on)}$ with variation in
Figure 6.4: On-resistance $R_{DS(on)}$ of gallium nitride, silicon carbide, and silicon transistors as functions of breakdown voltage $V_{BD}$. The $R_{DS(on)}$ for GaN FETs is very low as compared to that of Si MOSFET at the same temperature. The product of on-resistance $R_{DS(on)}$ and gate charge $Q_g$ of gallium nitride, silicon carbide, and silicon transistors as a function of temperature $T$ is shown in Figure 6.6. The inverse of the product of on-resistance $R_{DS(on)}$ and gate charge $Q_g$ of gallium nitride, silicon carbide, and silicon transistors as functions of temperature $T$ is shown in Figure 6.7. The Figure-of-Merit (FOM), which is $R_{DS(on)} \times Q_g$ is a very good indicator of the device’s conduction losses, switching losses, and the speed. A higher FOM like that of GaN indicates minimization of losses and improvement in the speed of operation.

6.3.1 Figure-of-Merit

The gate charge $Q_g$ is the amount of charge required by the gate of the transistor to turn-on completely. The transistor’s speed directly depends on the gate charge. High speed and
low gate losses are achieved with low gate charge which results in high efficiency. The on-resistance \( R_{\text{DS(on)}} \) determine the conduction losses of a transistor. The product of required gate charge \( Q_g \) and \( R_{\text{DS(on)}} \) provides the insight into the transistor’s performance. The lower this product the better the transistor is. Figure 6.8 shows the \((R_{\text{DS(on)}} \times Q_g^{-1})\) figure-of-merit. The higher the inverse of this product is the better the device.

### 6.4 Results for PWM Synchronous Buck DC-DC Converter

For the design example discussed in Chapter 4, the summary of results for the performance of the PWM synchronous buck dc-dc converter using EPC2020 GaN FETs at different switching frequencies is analyzed. It is observed that the efficiency of circuit of PWM synchronous buck dc-dc converter highly depends on the operating frequency. The efficiency of PWM synchronous buck dc-dc converter using GaN FET is much higher that the efficiency of the same circuit using Si MOSFET at same frequency. Moreover, Si MOSFET gives
Figure 6.6: The product of on-resistance $R_{DS(on)}$ and gate charge $Q_g$ of gallium nitride, silicon carbide, and silicon transistors as functions of temperature $T$.

up at much lower frequencies than that of GaN FET. Figure 6.9 shows the comparison of theoretical efficiency of PWM synchronous buck dc-dc converter for GaN and Si transistors. In order to validate the analysis, experiments are performed on a laboratory prototype of a synchronous buck dc-dc converter. Following this is the comparison of the theoretical, simulation, and experiments.

### 6.4.1 Comparison of Theoretical and Simulation Results

Figure 6.10 shows the comparison of theoretical and simulated efficiencies of PWM synchronous buck dc-dc converter using EPC2020 GaN FET for the circuit design example mentioned in Chapter 4. The simulation results are in good agreement with theoretical results.
Figure 6.7: The inverse of the product of on-resistance $R_{(DS_{on})}$ and gate charge $Q_g$ of gallium nitride, silicon carbide, and silicon transistors as functions of temperature $T$.

Figure 6.8: The bar graph of figure-of-merit ($R_{(DS_{on})} \times Q_g^{-1}$) of gallium nitride, silicon carbide, and silicon transistors.
6.4.2 Experimental Results

A laboratory prototype of the PWM synchronous buck dc-dc converter was built to evaluate the efficiencies of the converter at high-frequencies using the gallium nitride (GaN) transistors. EPC9037 development board from Efficient Power Conversion was used in place of the half-bridge network for the synchronous buck converter. The EPC9037 development board is a half-bridge configuration with two enhancement-mode GaN FETs and on-board gate drivers. The factory-built EPC2101 is driven by high-frequency gate-driver namely LM5113 manufactured by Texas Instruments. The pulse-width modulated waveforms to the two transistors are enabled using a NAND logic, which offers the required delay for the gating pulses.

The specifications of the synchronous buck dc-dc converter presented in Chapter 4 was considered and is repeated here for the sake of convenience:
Figure 6.10: The comparison of theoretical and simulated efficiency of PWM synchronous buck dc-dc converter using gallium nitride transistors.

- Input voltage $V_I = 12$ V
- Output voltage $V_O = 6$ V
- Minimum output current $I_{Omin} = 0.7$ A
- Load resistance $R_L = 5$ Ω
- Switching frequencies $f_s = 100$ kHz, 500 kHz, 1 MHz, 2 MHz, 5 MHz, 8 MHz, 10 MHz

The minimum value of inductance and the minimum value of capacitance required for CCM

<table>
<thead>
<tr>
<th>$f_s$</th>
<th>$L_{min}$ (µH)</th>
<th>Used $L$ (µH)</th>
<th>$C_{min}$ (µF)</th>
<th>Used $C$ (µF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 kHz</td>
<td>28.0612</td>
<td>33</td>
<td>61.111</td>
<td>100</td>
</tr>
<tr>
<td>1 MHz</td>
<td>2.8061</td>
<td>3.3</td>
<td>6.1111</td>
<td>10</td>
</tr>
<tr>
<td>2 MHz</td>
<td>1.4031</td>
<td>1.8</td>
<td>3.0556</td>
<td>5</td>
</tr>
<tr>
<td>8 MHz</td>
<td>0.3508</td>
<td>0.47</td>
<td>0.7639</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 6.1: Inductance and capacitance values for the synchronous buck dc-dc converter
operation at switching frequencies mentioned above were calculated. The values of these components and the correspondingly chosen values for the experiment are given in Table 6.1.

Figure 6.11 shows the photograph of full experimental set-up. The circuit of PWM synchronous buck dc-dc converter using EPC9037 development board was constructed as shown in Figure 6.12. The experiment was performed by changing the switching frequency to different values: 100 kHz, 1 MHz, 10 MHz, and 15 MHz. A zoomed in picture of EPC9037 development board is shown in figure 6.12. The high-frequency pulse-width modulated signals to the gate-driver were generated using the Tektronix AFG3251 arbitrary function generator. The inductor currents were measured using the Tektronix AM 503B high-bandwidth high sensitivity current dc/ac current probe. The various voltage and current waveforms were recorded using the Tektronix TDS2004C digital oscilloscope.

![Picture of full experimental set-up.](image-url)
Figure 6.12: Picture of PWM synchronous buck dc-dc converter with EPC9037 half bridge module.

Figure 6.14 shows the experimentally obtained waveforms of the gate-to-source voltage, drain-to-source voltage, and the inductor current for a switching frequency of 100 kHz. Due to the use of an ac current probe, only the ac component of the inductor current was recorded. However, for an output voltage of 6 V and a load resistance of 5 Ω, the average inductor current is 1.2 A. By adding the average inductor current with its ac component indicates the operation of the converter well in the continuous-conduction mode. The maximum voltage across the lower transistor was equal approximately equal to \( V_I \). A maximum value of 14.62 V was observed and the ripple voltage due to transistor switching was also evident in the observations. In summary, the shapes of these critical waveforms were in good shape and in an acceptable condition yielding an efficiency as high as 96.75%.

Figure 6.15 shows the experimentally obtained waveforms of the gate-to-source voltage,
Figure 6.13: Picture of EPC9037 half bridge module, which includes the voltage regulator MCP1703, high-frequency gate-drive LM5113, and EPC2101 half-bridge module of enhancement-mode GaN transistors.

drain-to-source voltage, and the inductor current for a switching frequency of 500 kHz. Some undesirable ringing is observed in the gate-to-source voltage waveform, which is predominantly due to the probe reactance and traces of the inductance of the breadboard. On the whole, the shapes of the waveforms represented a proper buck action and resulted in an overall converter efficiency of 95.85%.

Figure 6.16 shows the experimentally obtained waveforms of the gate-to-source voltage, drain-to-source voltage, and the inductor current for a switching frequency of 1 MHz. This frequency can be treated as a high-frequency case for the converter. At 1 MHz, the transistor’s performance was well within acceptable conditions. The overall efficiency was observed to be 93.98%.

Figure 6.17 shows the experimentally obtained waveforms of the gate-to-source voltage, drain-to-source voltage, and the inductor current for a switching frequency of 2 MHz. The shapes of the drain-to-source voltage and the inductor current were retained at normal
conditions, whereas the shape of the gate-to-source voltage waveform was highly distorted due to severe ringing. The fall time of the drain-to-source voltage waveform was decreased at this frequency. The overall efficiency was reported to be 88.68%.

Further experimentation involved high switching frequencies. As the switching frequency was increased beyond 5 MHz, the ringing in the gate-to-source voltage waveform was very dominant and was not in representable condition. The inductor current waveform also did not reflect better waveforms, owing to the probe reactance and limited bandwidth of the current probe, thus it has not been shown in the future figures.

Figure 6.18 shows the experimentally obtained waveforms of the drain-to-source voltage and the output voltage for a switching frequency of 5 MHz. From the plot it can be seen that the transistor’s rise and fall times have become comparable with the switching period. The output voltage was reduced to only 3.63 V as opposed to a rated value of 6 V. One may consider the operation at this frequency to be unacceptable. Similar waveforms were obtained through simulations at a switching frequency of 8 MHz. However, due to the naturally existing parasitics in the converter set-up, the converter exhibited poor performance at 5 MHz. The overall efficiency as observed as 78.96%.

Final set of results were obtained at 8 MHz. Figure 6.19 shows the experimentally obtained waveforms of the drain-to-source voltage and the output voltage for a switching frequency of 8 MHz. The drain-to-source voltage waveform indicated a poor performance situation, where the waveform could cease to discharge completely to zero before the start of the next cycle. Also, the output voltage was extremely lower, approximately 3 V. This frequency was considered as the hard limit beyond which the converter fails to perform any switching.

For the sake of curiosity, the frequency was increased to 10 MHz and the waveforms were observed. The drain-to-source voltage failed to reduce to zero at this frequency due to the incapability of the output capacitance to discharge to zero. The input current increased since the transistor conducted through the output capacitance. This undesirable effect can
Figure 6.14: Experimentally obtained plots of gate-to-source voltage $v_{GS}$ (upper trace), drain-to-source voltage $v_{DS}$ (middle trace), and inductor current $i_L$ (lower trace) at $f_s = 100$ kHz.

Table 6.2: Theoretical, simulated, and measured efficiencies of sync. buck dc-dc converter

<table>
<thead>
<tr>
<th>Switching Frequency</th>
<th>Theoretical %</th>
<th>Simulated %</th>
<th>Experimental %</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 kHz</td>
<td>99.30</td>
<td>98.42</td>
<td>96.75</td>
</tr>
<tr>
<td>500 kHz</td>
<td>98.50</td>
<td>98.13</td>
<td>95.85</td>
</tr>
<tr>
<td>1 MHz</td>
<td>97.51</td>
<td>97.82</td>
<td>93.98</td>
</tr>
<tr>
<td>2 MHz</td>
<td>95.60</td>
<td>93.81</td>
<td>88.68</td>
</tr>
<tr>
<td>5 MHz</td>
<td>90.29</td>
<td>88.63</td>
<td>78.96</td>
</tr>
<tr>
<td>8 MHz</td>
<td>85.54</td>
<td>82.04</td>
<td>70.55</td>
</tr>
<tr>
<td>10 MHz</td>
<td>82.64</td>
<td>81.45</td>
<td>-</td>
</tr>
<tr>
<td>15 MHz</td>
<td>76.18</td>
<td>71.08</td>
<td>-</td>
</tr>
</tbody>
</table>

be avoided only if the switching frequency is held below 8 MHz.

The values for theoretical, simulated, and experimental efficiencies are obtained and are shown in Table 6.2. Figure 6.20 shows the comparison of theoretical and experimental efficiencies obtained for the design example discussed in Chapter 4. The experimental efficiency is lower than that of theoretical efficiency.
Figure 6.15: Experimentally obtained plots of gate-to-source voltage $v_{GS}$ (upper trace), drain-to-source voltage $v_{DS}$ (middle trace), and inductor current $i_L$ (lower trace) at $f_s = 500$ kHz.

6.5 Results for Half-Bridge Class-D Resonant Inverter Using GaN Transistor

6.5.1 Comparison of Theoretical and Simulation Results

The values for theoretical and simulated efficiencies of half-bridge class-D resonant inverter using EPC2020 GaN FET for the circuit design example mentioned in Chapter 5 are obtained and are shown in Table 6.3. Figure 6.21 shows the plots of theoretical and simulated efficiencies. The simulation results are in good agreement with the theoretical results.

<table>
<thead>
<tr>
<th>Switching Frequency</th>
<th>Theoretical %</th>
<th>Simulated %</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 kHz</td>
<td>94.15</td>
<td>93.22</td>
</tr>
<tr>
<td>1 MHz</td>
<td>89.16</td>
<td>88.56</td>
</tr>
<tr>
<td>5 MHz</td>
<td>72.17</td>
<td>70.02</td>
</tr>
<tr>
<td>8 MHz</td>
<td>63.15</td>
<td>62.51</td>
</tr>
<tr>
<td>10 MHz</td>
<td>58.29</td>
<td>60.29</td>
</tr>
<tr>
<td>15 MHz</td>
<td>48.89</td>
<td>45.75</td>
</tr>
</tbody>
</table>
Figure 6.16: Experimentally obtained plots of gate-to-source voltage $v_{GS}$ (upper trace), drain-to-source voltage $v_{DS}$ (middle trace), and inductor current $i_L$ (lower trace) at $f_s = 1$ MHz.

Figure 6.17: Experimentally obtained plots of gate-to-source voltage $v_{GS}$ (upper trace), drain-to-source voltage $v_{DS}$ (middle trace), and inductor current $i_L$ (lower trace) at $f_s = 2$ MHz.
Figure 6.18: Experimentally obtained plots of drain-to-source voltage $v_{DS}$ (upper trace) and output voltage $V_O$ (lower trace) at $f_s = 5$ MHz.

Figure 6.19: Experimentally obtained plots of rain-to-source voltage $v_{DS}$ (upper trace) and output voltage $V_O$ (lower trace) at $f_s = 8$ MHz.
Figure 6.20: The comparison of theoretical and experimental efficiency of PWM synchronous buck dc-dc converter with gallium nitride transistors.

Figure 6.21: The comparison of theoretical and simulated efficiency of half-bridge class-D resonant inverter using gallium nitride transistors.
7 Conclusions and Future Work

7.1 Thesis Summary

The three aspects related to gallium nitride (GaN), which have been presented in this thesis are as follows:

- **GaN Semiconductor Material:**
  A detailed study on the properties of the gallium-nitride (GaN) semiconductor material has been presented. The various expressions of the physical properties of GaN semiconductor materials have been presented. Moreover, the effect of temperature on the intrinsic carrier concentration, the carrier mobilities, and the resistivity for the silicon (Si), silicon carbide (SiC), and GaN semiconductor materials have been discussed and compared. The different figures-of-merit (FOM) for the GaN, Si, and SiC semiconductor materials have been presented and compared.

- **GaN Field-Effect Transistors:**
  The properties of the GaN field-effect transistor (FET) have been compared with silicon Si and SiC counterparts. The principle of operation of the GaN FET has been discussed. The critical differences in the process of formation of the electron conduction path in Si and GaN transistors have been highlighted. The figure-of-merit for the GaN power transistor has been explained and compared with that of Si and SiC transistors. Further, using the Spice model of EPC2020 enhancement-mode GaN power transistor, the dc and ac dynamic characteristics have been investigated and the results agreed with those presented in the manufacturer’s datasheet.

- **Applications of GaN transistors in Power Electronic Circuits:**
  The applications of the GaN power transistor in power electronic circuits has been explored. Two practical implementation of the GaN power transistors are (a) pulse-width modulated (PWM) synchronous buck dc-dc power converter and (b) half-bridge
class-D series resonant inverter. These circuits have been designed for practical design specifications. Theoretical power losses of all the components and efficiencies were derived, and the voltage and current stresses of all the components were determined. Circuit simulations were performed on these circuits using SABER circuit simulator. The EPC2020 enhancement-mode GaN transistors from Efficient Power Conversion Corporation (EPC) were used in the half-bridge switching network. Initial observations were first made at lower switching frequencies to verify the correctness of the designed circuit. Further, the switching frequency was increased to higher values to determine the maximum operable limits of the GaN transistor. Similar simulations were performed using the Si transistor. The shape of the drain-to-source voltage waveforms were observed after each trial. The circuit with Si transistor produced highly distorted waveforms due to very high switching losses at about 5 MHz, whereas the circuit with GaN transistors performed well at high efficiencies until 15 MHz. The deviation from the normal shape of the drain-to-source voltage waveform was observed only above 15 MHz. Experimental validations were performed on the PWM synchronous buck converter operating in continuous-conduction mode. The prototype of the converter was built using the EPC9037 half-bridge switching network module, which was driven using the LM5113 high-speed, dual-side gate-driver. The performance of the converter has been evaluated at different switching frequencies, starting from 100 kHz to 8 MHz. It was observed that at 8 MHz, the drain-to-source capacitor ceased to discharge and the converter failed to perform the switching action. An efficiency of about 98% has been recorded at 100 kHz and 55% at 8 MHz. The theoretical predictions were in agreement with the simulation and experimental results.

7.2 Semiconductors and Their Target Applications

Every semiconductor has its own market and target consumers. The reliability of silicon (Si) transistors is fairly high in the CMOS and microelectronics industry, whereas the appli-
cability of silicon carbide (SiC) is better in high-voltage and high-temperature conditions. The introduction of gallium nitride (GaN) and a solid research in its application domain has shown that the GaN devices share the markets of both Si and SiC. Figure 7.1 shows a chart of the different areas of applications, where GaN devices are being used. The applications shown in the chart can be divided into three different categories, namely: (a) high/low-voltage and low-frequency, (b) low-voltage and high-frequency, and (c) high-voltage and high-frequency.
7.2.1 High/Low-Voltage and Low-Frequency Applications

The number of applications in this voltage and frequency range is manifold. The frequency range is 100 kHz to 10 MHz while the voltage range is 50 V to 600 V. Most of the switched-mode power supplies for portable applications, lighting, consumer electronic applications, etc., appear in this category. For frequencies of 100 kHz to 1 MHz and a voltage range of 50 V to 200 V, the use of Si is justified in this range since its switching losses and conduction losses are low. Due to the nature of the application, the temperature at which they operate is also low, resulting in smaller heat sinks and much compact modules. Thus, for these voltage values and the above mentioned frequency range, the silicon transistors operate at efficiencies, which are comparable with those of GaN transistors.

The Si MOSFETs exhibit huge on-resistance at a higher voltage range, i.e. 200 V and above and at low frequencies, which is undesirable for high-voltage applications. While the SiC transistors rule the high-voltage market, the GaN transistors have also begun to show their presence. The inherent capability of SiC to withstand higher temperatures due to high thermal conductivity and achieve high breakdown voltages due to higher breakdown electric field makes them the best choice amongst the three semiconductor types. Therefore, at these voltages and frequencies a strong competitor to SiC is the GaN transistor. However, its use may be limited due to its cost and availability, when compared with SiC devices.

7.2.2 Low-Voltage and High-Frequency Applications

Present day research is gaining pace in this category of applications. The advent of wirelessly charged portable applications, high-bandwidth mobile, and cellular transmitter schemes have been demanding much efficient power supplies. The frequency range is 10 MHz to 5 GHz while the voltage range is 50 V to 600 V. The use of Si beyond 2.5-5 MHz and 500 V is not justified due to its severely high switching losses. The SiC cannot be used due to the bulky nature of the switching modules. Thus, GaN shows a superiority over the other two devices and is a potential candidate for future applications in this voltage and frequency range.
However, at low voltages and at very high frequencies, such as 2 GHz to 5 GHz, Si transistors have shown their major importance. This is due to their high reliability, ease in fabrication, and most importantly the abundance of silica in nature. The CMOS and IC technology, which runs today’s electronic world has a very high dependence on Si and will definitely take few years for GaN to prove its feasibility in this field of applications.

7.2.3 High-Voltage and High-Frequency Applications

This category is where GaN can make its mark, where Si and SiC fail to operate reliably. Few applications in this category are AM and FM radio broadcasting stations, high-voltage rectifiers, power supplies for aircraft, ships, military vehicles, etc. These applications involve generation of very high voltages (to the order of 20 kV – 25 kV) and at frequencies of around 15 MHz - 20 MHz. A higher frequency is usually a consequence of high ac line voltage frequency, which is usually 250 Hz to 400 Hz. The cost of the equipment is back-burnered since its reliability, safety, and effectiveness are given higher importance.

7.3 Take-Home Lessons

In the process of working on this thesis, various lessons have been learned. I made a decision to do some challenging research on a topic, which has shown a growing interest in many research areas in electrical and electronic communities. That special topic has turned out to be the topic of my M.S. thesis. The most important lessons, which also apply to any research were to read, read, and read. Writing an M.S. thesis imposes some special challenges such as literature survey, analysis, simulations, experiments, comparisons, and drawing conclusions. I have garnered many skills during the process. Although the topic was challenging, I have learned about a new technology, which has not been discussed in detail in the text books. The entire process of working on this thesis also helped me connect the diverse technical knowledge I had. The topic of this M.S. thesis was a great education experience for me.
7.4 Conclusions

The following conclusions can be drawn from this M.S. thesis:

1. The gallium nitride semiconductors are superior than the silicon (Si) semiconductors in several aspects including mobility, maximum junction temperature, thermal velocity, and conductivity.

2. Due to the wide band gap energy of GaN semiconductors (similar to silicon carbide), it possesses a very high temperature handling capability; a major requirement for high power, high current, and high temperature applications.

3. The 2-dimensional electron gas (2-DEG) contributes to the majority of the current conduction at the interface between AlGaN and GaN hetero-structures. The mobility of electrons in the 2-DEG is of the order of 2000 cm$^2$/V·s.

4. The specific on-resistance is very low, which is a major improvement over the Si transistors and is mainly due to the high electron mobility and the wide band gap energy of GaN. This is also the main reason for smaller transistor size, when compared to Si transistors.

5. For the GaN transistors, the trans-conductance is at least twice that of Si. Also, the low intrinsic capacitances ($C_{gs}$ and $C_{gd}$) result in a higher unity-gain frequency $f_T$ for the GaN transistors, which is a good indicator of high-speed devices.

6. The drain-to-source capacitance $C_{ds}$ is also very low. Thus, the switching losses are very low in GaN transistors, which is an attractive feature for high-frequency applications.

7. The GaN enhancement-mode FET is much easier to drive than the depletion-mode FET.
8. For synchronous buck converters with practical specifications, the simulations results show that the overall efficiency of the converters using GaN-based transistors reduced to 60% at around 15 MHz, while the overall efficiency of the Si-based power converters reduced to 40% at 5 MHz. The experimental limit of switching frequencies is 8 MHz. Operation beyond this range resulted in switching intervals, where the output capacitance ceased to discharge, which is undesirable for normal operating conditions.

9. For Class-D series resonant converter, the simulations have indicated efficiencies up to the order of 80% even at 5 MHz using GaN-based transistors, whereas 40% at 5 MHz using Si-based transistors. Also, by operating the inverter at zero-voltage switching (ZVS), the maximum achievable switching frequency with lower losses is around 10 MHz. Operation beyond this resulted in improper shapes of the waveforms and unpredictable current and voltage spikes.

10. A careful layout of the circuit prototype in the megahertz range is important because the circuit parasitic components become dominant leading to unpredictable behavior.

7.5 Contributions

1. The material properties of GaN have been studied and compared with SiC and Si, which include thermal velocity of charge carriers, breakdown voltage, breakdown electrical field, intrinsic carrier concentration, extrinsic carrier concentration, charge carrier mobility, saturation velocity, resistivity, and conductivity.

2. The properties and features of the GaN transistor used in power electronic circuits such as: (a) figure-of-merit, (b) specific-on resistance, and (c) device operation have been summarized and presented.

3. The dc and dynamic ac characteristics of EPC2020 enhancement-mode GaN have been evaluated.
4. The performance of the synchronous buck dc-dc converter using GaN half-bridge module through simulations has been evaluated and validated through experiments for a range of frequencies (100 kHz to 15 MHz).

5. The performance of the half-bridge class-D resonant inverter using GaN half-bridge module has been evaluated through simulations for a range of frequencies (100 kHz to 15 MHz).

7.6 Future Work

The following research topics are suggested for the future work:

- Analysis of the effect of temperature on the performance of the gallium-nitride (GaN) transistors and comparison with silicon-carbide power transistors.

- Development of a robust mathematical model for the drain current in the GaN field-effect transistor.

- Development of spice models for the enhancement-mode and depletion-mode GaN transistors based on the EKV model.

- Analysis of the behavior of the nonlinear capacitances of the GaN transistors as a function of the applied voltage.
8 Bibliography

GaN Material


GaN Transistors


GaN Applications


[43] T. Song, N. Huang, and A. Ioinovici, “A family of zero-voltage and zero-current-switching (ZVZCS) three-level DC-DC converters with secondary-assisted regener-


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Publications


Appendix A

Physical Constants and Values of Semiconductor Material Properties

This appendix provides the values of the physical constants and the values of the physical properties of silicon (Si), silicon-carbide (SiC), and gallium nitride (GaN) semiconductor materials.

Table A.1 provides the values of physical properties. Table A.2 lists the values of all the critical physical properties of Si, SiC, and GaN semiconductor materials.

<table>
<thead>
<tr>
<th>Property</th>
<th>Symbol</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal voltage</td>
<td>$V_T = kT/q$</td>
<td>V</td>
<td>0.0259 at $T = 300 \text{ K}$</td>
</tr>
<tr>
<td>Boltzmann’s constant</td>
<td>$k = E_f/k$</td>
<td>J/K</td>
<td>$1.3806488 \times 10^{-23}$</td>
</tr>
<tr>
<td>Boltzmann’s constant</td>
<td>$k = E_f/k$</td>
<td>eV/K</td>
<td>$8.62 \times 10^{-5}$</td>
</tr>
<tr>
<td>Planck’s constant</td>
<td>$h$</td>
<td>J-s</td>
<td>$6.62617 \times 10^{-34}$</td>
</tr>
<tr>
<td>Planck’s constant</td>
<td>$h$</td>
<td>eV·s</td>
<td>$4.14 \times 10^{-15}$</td>
</tr>
<tr>
<td>Magnitude of electron charge</td>
<td>$q$</td>
<td>C</td>
<td>$1.60218 \times 10^{-19}$</td>
</tr>
<tr>
<td>Free-space permittivity</td>
<td>$\epsilon_0 = \frac{10^{-9}}{36\pi}$</td>
<td>F/m</td>
<td>$8.85418 \times 10^{-12}$</td>
</tr>
<tr>
<td>Free-space permeability</td>
<td>$\mu_0$</td>
<td>H/m</td>
<td>$4\pi \times 10^{-7}$</td>
</tr>
<tr>
<td>Speed of light in free space</td>
<td>$c = \frac{1}{\sqrt{\epsilon_0 \mu_0}}$</td>
<td>m/s</td>
<td>$2.998 \times 10^8$</td>
</tr>
<tr>
<td>Mass of free electron</td>
<td>$m_e$</td>
<td>kg</td>
<td>$9.31 \times 10^{-31}$</td>
</tr>
<tr>
<td>Mass of free hole</td>
<td>$m_h$</td>
<td>kg</td>
<td>$1.673 \times 10^{-27}$</td>
</tr>
</tbody>
</table>
Table A.2: Properties of silicon, silicon carbide, and gallium nitride

<table>
<thead>
<tr>
<th>Property</th>
<th>Symbol</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon band gap energy</td>
<td>$E_{G(Si)}$</td>
<td>eV</td>
<td>1.12</td>
</tr>
<tr>
<td>Silicon band gap energy</td>
<td>$E_{G(Si)}$</td>
<td>J</td>
<td>$1.793 \times 10^{-19}$</td>
</tr>
<tr>
<td>Silicon-carbide band gap energy</td>
<td>$E_{G(SiC)}$</td>
<td>eV</td>
<td>3.26</td>
</tr>
<tr>
<td>Silicon-carbide band gap energy</td>
<td>$E_{G(SiC)}$</td>
<td>J</td>
<td>$5.216 \times 10^{-19}$</td>
</tr>
<tr>
<td>Gallium-nitride band gap energy</td>
<td>$E_{G(GaN)}$</td>
<td>eV</td>
<td>3.39</td>
</tr>
<tr>
<td>Gallium-nitride band gap energy</td>
<td>$E_{G(GaN)}$</td>
<td>J</td>
<td>$5.430 \times 10^{-19}$</td>
</tr>
<tr>
<td>Silicon-dioxide band gap energy</td>
<td>$E_{G(SiO_2)}$</td>
<td>eV</td>
<td>9</td>
</tr>
<tr>
<td>Silicon-dioxide band gap energy</td>
<td>$E_{G(SiO_2)}$</td>
<td>J</td>
<td>$1.449 \times 10^{-19}$</td>
</tr>
<tr>
<td>Silicon breakdown electric field</td>
<td>$E_{BD(Si)}$</td>
<td>V/cm</td>
<td>$2 \times 10^5$</td>
</tr>
<tr>
<td>Silicon-carbide breakdown electric field</td>
<td>$E_{BD(SiC)}$</td>
<td>V/cm</td>
<td>$22 \times 10^5$</td>
</tr>
<tr>
<td>Gallium-nitride breakdown electric field</td>
<td>$E_{BD(GaN)}$</td>
<td>V/cm</td>
<td>$35 \times 10^5$</td>
</tr>
<tr>
<td>Silicon-dioxide breakdown electric field</td>
<td>$E_{BD(SiO_2)}$</td>
<td>V/cm</td>
<td>$60 \times 10^5$</td>
</tr>
<tr>
<td>Silicon relative permittivity</td>
<td>$\epsilon_r(Si)$</td>
<td>–</td>
<td>11.7</td>
</tr>
<tr>
<td>Silicon-carbide relative permittivity</td>
<td>$\epsilon_r(SiC)$</td>
<td>–</td>
<td>9.7</td>
</tr>
<tr>
<td>Gallium-nitride relative permittivity</td>
<td>$\epsilon_r(GaN)$</td>
<td>–</td>
<td>8.9</td>
</tr>
<tr>
<td>Silicon-dioxide relative permittivity</td>
<td>$\epsilon_r(SiO_2)$</td>
<td>–</td>
<td>3.9</td>
</tr>
<tr>
<td>Silicon electron mobility at $T = 300$ K</td>
<td>$\mu_{n(Si)}$</td>
<td>cm$^2$/V·s</td>
<td>1360</td>
</tr>
<tr>
<td>Silicon-carbide electron mobility at $T = 300$ K</td>
<td>$\mu_{n(SiC)}$</td>
<td>cm$^2$/V·s</td>
<td>900</td>
</tr>
<tr>
<td>Gallium-nitride electron mobility at $T = 300$ K</td>
<td>$\mu_{n(GaN)}$</td>
<td>cm$^2$/V·s</td>
<td>2000</td>
</tr>
<tr>
<td>Silicon hole mobility at $T = 300$ K</td>
<td>$\mu_{p(Si)}$</td>
<td>cm$^2$/V·s</td>
<td>480</td>
</tr>
<tr>
<td>Silicon-carbide hole mobility at $T = 300$ K</td>
<td>$\mu_{p(SiC)}$</td>
<td>cm$^2$/V·s</td>
<td>120</td>
</tr>
<tr>
<td>Gallium-nitride hole mobility at $T = 300$ K</td>
<td>$\mu_{p(GaN)}$</td>
<td>cm$^2$/V·s</td>
<td>30</td>
</tr>
<tr>
<td>Silicon effective electron mass coefficient</td>
<td>$k_e$</td>
<td>–</td>
<td>0.26</td>
</tr>
<tr>
<td>Silicon effective hole mass coefficient</td>
<td>$k_h$</td>
<td>–</td>
<td>0.39</td>
</tr>
<tr>
<td>Silicon-carbide effective electron mass coefficient</td>
<td>$k_{e(SiC)}$</td>
<td>–</td>
<td>0.36</td>
</tr>
<tr>
<td>Silicon effective hole mass coefficient</td>
<td>$k_{h(SiC)}$</td>
<td>–</td>
<td>1</td>
</tr>
<tr>
<td>Gallium-nitride effective electron mass coefficient</td>
<td>$k_{e(GaN)}$</td>
<td>–</td>
<td>0.23</td>
</tr>
<tr>
<td>Gallium-nitride effective hole mass coefficient</td>
<td>$k_{h(GaN)}$</td>
<td>–</td>
<td>0.24</td>
</tr>
</tbody>
</table>