Design of an 8-bit Successive Approximation Pipelined Analog to Digital Converter (SAP-ADC) in 90 nm CMOS

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Design of an 8-bit Successive Approximation Pipelined Analog to Digital Converter (SAP-ADC) in 90 nm CMOS

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering

by

Vivek Kotti.
B. Tech, Krishna University, 2014

2017
Wright State University
I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Vivek Kotti ENTITLED Design of an 8-bit Successive Approximation Pipelined Analog to Digital Converter (SAP-ADC) in 90nm CMOS BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Electrical Engineering.

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ABSTRACT

Kotti Vivek. M.S.E.E, Department of Electrical Engineering, Wright State University, 2017. Design of an 8-bit Successive Approximation Pipelined Analog to Digital Converter (SAP-ADC) in 90nm CMOS.

Analog to Digital Converters bridge the gap between physical world and digital signal processing. Most times analog signals received from the real world needs to be amplified and converted to digital to impart various signal enhancements to the received signal. The digital signal is much suitable to operate on with less noise and well defined logic levels when compared to continuously varying analog signal. Communication systems demand ever-increasing bandwidth which unfortunately has been a huge limitation for present day ADCs. Hence, an architecture which combines the accuracy of a SAR -ADC with the concept of pipelining to increase the bandwidth can be a great solution to achieve high sampling frequency (GHz) and broad bandwidth. The 8- bit SAP ADC implemented in this thesis using 90nm COMS technology achieves a sampling rate of 1GHz with input frequencies up to 125MHz.
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Dedicated to

My family and friends.
1 INTRODUCTION

1.1 ADC Overview:

Any naturally occurring physical quantity must be inevitably represented in the form of an analog signal. But the components for processing analog signals are complex to design and occupy more chip size when compared to digital components. Hence companies today are keen in cutting down costs and increase information accuracy by converting an analog signal to digital form. This is achieved through a high linear Analog to Digital converter (ADC). Any physical signal be it magnetic, optical, acoustic or thermal can be converted into respective electric signals for processing which is generally in analog form. Now, the ADC converts the incoming analog signal into digital one by performing three main operations on it namely

1. Sampling the continuous signal using a S/H (sample and hold) circuit.

2. Quantize.

3. Digitize.

![ADC Block diagram](image)

Figure 1 ADC Block diagram [1]
The incoming analog signal which is continuous in time and amplitude is sampled and held typically using Track and Hold circuit. The sampling is done satisfying the Nyquist criterion which states that the sampling rate $f_s$ should be greater than or equal to the maximum bandwidth of the input signal $f_B$ [2].

$$f_s \geq 2f_B$$  \hspace{1cm} (1.1)

Figure 2 Aliasing Effect [3]

Quantization is the process of rounding off the held values in the previous step to the nearest decimal equivalent number. The level of quantization or the level of closeness of the rounded off value to the original analog value depends on the resolution of the converter. Suppose a 2bit converter has four quantization levels or it can be said that a 2-bit converter divides the entire full scale range into four quantization levels. Whereas the level of sampling simply defines the bandwidth of that converter. This process of sampling and quantizing introduces errors which is known as quantization error or quantization noise [4]. This can be obtained by subtracting the quantized value from the original amplitude value at that sampling instant of time. Hence, it can be stated that higher the resolution of the converter, lower is the quantization noise.
The dynamic range of the ADC depends on its linearity and resolution and can be measured using a quantity called ENOB (Effective number of bits). An ideal ADC generally has ENOB equal to its resolution. But due to the presence of quantization noise and jitter ENOB is always less than resolution and hence perfect reconstruction of the original signal is a hard task. Each quantization level is said to be separated by 1 LSB (Least significant bit). 1 LSB is defined as the minimum amount of change at the input needed to produce a change or level transition at the output.

\[
\text{LSB} = \frac{V_{\text{ref}P} - V_{\text{ref}N}}{2^N}
\]  

(1.2)

There are many parameters used to characterize a ADC namely resolution, speed, DNL (Differential non-linearity), INL (Integral non-linearity), signal to noise and distortion ratio (SNDR), total harmonic distortion (THD) etc. There are many types of ADCs used in the industry right now and some of them are Flash, Pipelined, SAR ADC, Sigma Delta converters and time interleaved ADC. They can be differentiated basing on their design style, sampling rate [5]. For instance, all the above mentioned are Nyquist ADCs except the sigma delta and time interleaved are over and under sampling ADCs respectively. Each of these are used basing on the specifications and requirement for that job. Say for instance Flash gives top speed when compared to others but cannot attain high resolutions. In a conventional SAR ADC, the number of clock cycles required to make one complete conversion process is equal to the number of bits of the A/D converter. This number of clock cycles pose a fundamental limit on the speed at which a complete conversion from analog domain to digital domain takes place.

Also, in a conventional SAR converter, the fundamental bottleneck for high-precision comes from the matching requirements in a Capacitive Digital to Analog Converter. Typically, in a high precision SAR ADC, the mismatch in the capacitors that occur during fabrication is trimmed at final test using in-package trimming mechanism. This is a time intensive process and increases test cost enormously.
1.2 ADC ARCHITECTURES

1.2.1 Serial ADC

![Diagram of Serial Analog to Digital Converter](image)

Figure 3 Serial Analog to Digital Converter [6]

This is the basic type of Analog to Digital Converter which compares the input analog voltage to a reference ramp. The complexity of the circuit is very less and hence very high resolutions of the order 12-15 bits are obtained.

The disadvantage with the Serial conversion is that the conversion process takes very long. A single conversion is proportional to $2^{\text{No.of bits}}$.

The advantage is that very high accuracy can be achieved. Hence these ADCs are used in applications where time is not a constraint [6].
1.2.2 Flash ADC

In Flash Analog to Digital Converters the input is fed parallely to an array of comparators usually 1-bit to compare it with the reference voltage generated using a string of resistors as shown in the figure. The outputs from the comparators is then sent to Thermometer to Binary encoder for obtaining the final digital output.

The advantage with Flash architecture is it is very fast owing to the parallel conversion. Each conversion takes just one clock period [6].

The major disadvantage with Flash converters comes with their circuit complexity that requires $2^n - 1$ Comparators and $2^n$ resistors to provide reference voltage for each comparator which is one LSB greater than the one below it.
1.2.3 SAR ADC

Figure 5 Successive Approximation ADC [6]

A conventional N-bit SAR A/D converter takes N clock cycles for one full complete conversion process. This A/D converter consists of a sample-and-hold (S/H) circuit, a comparator, a digital-to-analog converter (DAC) and digital logic. The ADC employs a binary-search algorithm that uses the digital logic circuitry to determine the value of each bit in a sequential or successive manner based on the outcome of a comparison between the outputs of the S/H circuit and DAC [7]. Figure above illustrates a basic block diagram of a conventional binary search SAR A/D. The digital logic then sets the Most-Significant-Bit (MSB) to '1'. With the remaining bits set to '0', the digital word is then applied to the DAC to produce an analog output voltage that, once settled within 0.5 LSB of accuracy, is compared with the sampled voltage by the comparator. The analog equivalent of the digital word produced from DAC will be equal to the mid-scale of the reference voltage, $V_{ref}$. A comparator output of '1' means that the sampled signal is larger than the DAC’s output. If this is the case the MSB remains as '1', otherwise, it is set to '0'. In a similar way, every bit is set and is compared with a known reference value to decide its value. Hence each conversion takes 'N' clock cycles to complete [8].
1.2.4 Pipelined ADC

Higher resolution with a fewer number of Comparators can be achieved through this architecture. Each stage consists of a Sample and Hold Amplifier, Analog to Digital Converter and Digital to Analog converter and an Analog Subtractor.

The gain of the SHA block is generally $2^N$ where $N$ is the number of bits in that stage. If the input is high enough we can use Sample and Hold Buffer instead. The error correction logic is a Digital Pipe which contains large number of registers. Suppose it is a 4-bit ADC and each stage handles 4-bits and there are four such stages. So, a total of 16 bits are generated in the Digital Pipe which is later converted to 4-bit by shifting right method.

The advantage with this structure is that higher sampling rates and higher resolution can be achieved with a limited number of Comparators (typically $2^{N+1} - 2$).

The disadvantage is that the Latency of the Converter is increased. Also, it is very hard to design accurate analog Subtractors and Multipliers.
1.2.5 Delta Sigma Modulator

As it can be seen DSM consists of an Integrator and a Quantizer. ADC and DAC are connected back to back in Quantizer as shown in Figure 7. The output from the ADC is back converted to Analog and is fed back to the subtractor whose output is an error signal. The Integrator consists of a Subtractor and a unit delay block connected next to each other with output of delay feeding the input of a subtractor forming a loop. DSMs along with oversampling is very effective in achieving high resolutions. In First order DSMs SNR is increased by 9dB when the over sampling rate (OSR) is doubled. In Second order DSM, it increases by 15dB. Third order DSMs are very unstable under high frequencies and causes oscillations as we have more noise at higher frequencies. Pipelining can be used to further enhance the performance of the DSM. For example, we can implement an 8-bit ADC using just a 4-bit Quantizer.

However, disadvantages are, increased latency and the throughput is limited by the requirement for oversampling.
1.3 DAC Overview

DACs shortened for Digital to Analog Converters has utmost prominence in communication theory and electronic systems. They work by taking in Digital bits and convert them to a binary word ‘D’ as shown below.

\[ D = \frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{N-1}}{2^N} \]  

(1.3)

Where \( b_0, b_1, b_2, \ldots, b_{N-1} \) are input digital bits that are applied to the DAC. They output a reference analog voltage corresponding to each binary code. If a DAC takes in \( N \) bits it typically generates \( 2^N \) reference voltages. Many DAC architectures work by having a reference voltage that is divided into smaller references that correspond to the digital input [9]. With this reference voltage \( V_{ref} \), the analog output at any given digital input can be calculated as

\[ V_{out} = V_{ref} \left[ \frac{D}{2^N} \right] \]  

(1.4)

LSB shortened for Least Significant Bit is the shortest distance or the step size between adjacent analog references generated at the output. LSB can be defined as

\[ \text{LSB} = \frac{V_{ref}}{2^N} \]  

(1.5)

The reference voltages at the outputs create a staircase pattern. In communication receivers, the input signal received by the antenna is passed through the Low Noise Amplifiers and then the ADCs to convert the power amplified signal to digital bits. These digital bits are then fed into the Digital Signal Processors to make certain enhancements and modifications depending upon the application it is going to be used in. Then the digital signal must be converted back to analog domain for modulation and transmission. High speed data converters are need of the hour in present day technology finding ever-growing demand and application in high bandwidth communication systems and electronic circuits.
1.3.1 Resistor String DAC

This is the simplest of DAC architectures. The $2^N$ digital bit output coming from the encoder are used to operate the switches above. If the bit is logic ‘1’ the switch is closed and it is open for logic ‘0’. The resistor string consists of equal valued resistors terminated by reference voltage at one end and ground at the other end. The voltage reference across the successive resistor correspond to one LSB difference. The outputs of all the switches are tied together to form the equivalent analog output.

The advantage of this structure is that its output is monotonic and circuit complexity is less. The disadvantage is that all the resistors needs to be matched and consume a lot of area unless implemented by active devices. Switches induce a lot of parasitic capacitances which limit the speed of the converter.
1.3.2 Binary Weighted Resistor Ladder DAC

This architecture is almost like the previous architecture except that there is an increment in resistor values from ‘R’ for MSB to $2^{N-1}R$ for the LSB.

![Binary Weighted Resistor Architecture](image)

**Figure 9 Binary Weighted Resistor Architecture [6]**

Each resistor is connected to a switch which is controlled by the digital input word just like in the previous case. The outputs from the switches is connected to an op-amp in unity gain configuration to increase the output drive capability of the DAC. The main disadvantage is the area increases with the resistor value at higher resolutions. Matching is also very difficult which results in an error grater the one LSB even if there is a minute mismatch.
1.3.3 R-2R DAC

This architecture uses only two values of resistors R ad 2R which is a major improvement to the binary weighted resistor DAC. Though the area consumption is reduced, matching is still a problem unless it is implemented by active devices like diode connected loads or current sources.

![Figure 10 R-2R architecture](image)

The above figure shows a voltage mode R-2R DAC where the switches are used to switch between Vref and ground terminals. These switches are controlled by the incoming digital input word as in the case of previous architectures. The output is then connected to an op-amp which is optional. The connection to an op-amp has advantages like increase in drive capability and disadvantages like limiting the bandwidth of the converter and introducing non-linearity errors.
1.3.4 Current Steering

The implementation of current steering DAC is simple. It just requires N current sources to be connected between reference voltage and ground as shown in Figure 11. The output voltage is produced though voltage division occurring between the reference and voltage drop produced by the current sources during the current draw. This current draw is in turn controlled by switches which switch as per the digital input applied to the DAC.

The main advantage of the current steering architecture is that an output op-amp is not needed as the currents are converted to output voltages through the resistors in place as shown. The disadvantage is that there may be glitches in the output if the switching is improper [10].
1.3.5 Charge Scaling DAC

As the name indicates charge is scaled using the capacitors just like the voltage was scaled using the resistor architectures previously. Due to the advancements in sub-micron technologies a capacitor can be designed easily which also takes up less area than the resistors. Figure below shows the implementation of a 4-bit charge scaling DAC in binary weighted fashion.

![Charge scaling architecture](image)

**Figure 12 Charge scaling architecture [6]**

The design also uses a technique known as split capacitor array to save up even more space when designing the CDAC for higher resolutions. The switches are controlled by the incoming digital signal which in turn charges or does not the capacitor connected to it. The capacitor which is connected in between and parallel to the LSB array is called attenuation capacitor. There is also a terminating capacitor present at the end of the LSB array. The sum of the attenuation capacitor and the total LSB array should properly terminate the MSB array. So the value of the attenuation capacitor can be calculated as below.
\[ C_{\text{attenuation}} = \frac{C_{\text{LSB array}}}{C_{\text{MSB array}}} \times C \]  \hspace{1cm} (1.6)

The main advantages of the CDAC is it is fast and accurate. The power consumption and area are also less compared to the resistor DAC architecture. The disadvantage is parasitic loading, need of a reset switch and the use of Op-amp which limits the resolution.

### 1.4 Performance Metrics

The performance of an ADC can be assessed using many metrics but they are broadly classified into two types. They are Static performance and Dynamic performance. Some of the static performance metrics include Offset error, Gain error, differential nonlinearity, integral nonlinearity, monotonicity etc. They are measured by applying input to the ADC under test to produce a full-scale output range. The output at each code is measured and compared to the ideal value. The deviation of the actual value from the ideal value gives each of the above errors. On the differential nonlinearity is measured by applying a sine input to the ADC under test and FFT is done on the outputs of the ADC to see how it performs.

#### 1.4.1 Signal to Noise Ratio (SNR)

Signal to noise ratio is one of the significant and fundamental measure of dynamic nonlinearity of the ADC. Unlike static nonlinearity SNR measurement gives more practical functional ability of the ADC. It is defined as the ratio of fundamental signal power to the noise power excluding DC component and first nine largest spurs in the FFT plot. The measurement must be done applying full scale input to the ADC under test as it is obvious that SNR is directly related to the signal power. SNR is given b
\[ \text{SNR} = 10 \log \left( \frac{p_{\text{signal}}}{\sum p_{\text{noise}}} \right) \]  

(1.7)

As it is mentioned in the introduction most of the noise in the ADC comes from the quantization error. The above SNR equation can be modified as

\[ \text{SNR} = 10 \log \left( \frac{V_{\text{inrms}}}{V_{Q\text{rms}}} \right) \]  

(1.8)

By substituting the RMS values of signal amplitude and noise amplitude (taking the stochastic approach) SNR for an N bit analog to digital converter can be calculated as

\[ SNR_{dB} = 6.02N + 1.76 \text{dB} \]  

(1.9)

### 1.4.2 Spurious Free Dynamic Range

A spur is known as the highest distortion component present in FFT plot that limits the dynamic performance of the ADC. It is one of the most important performance metrics to understand the real-time performance of the ADC or DAC.

The distortion components are generally the second and third order harmonics \([11]\) of the fundamental frequency or their aliases. But in interleaved ADCs there are certain spurs which are even higher than these harmonics. Also, some companies in their datasheets differentiate SFDR as narrow band and wide band. Hence the exact definition of SFDR can be given as the ratio of fundamental power to the largest spur whether harmonically related or not measured from zero to the Nyquist bandwidth in the FFT plot of the ADC \([12]\). SFDR can be given as
17

\[ SFDR = \text{Signal power (dB)} - \text{Largest spur power (dB)} \]  
\[ (1.10) \]

**Figure 13 FFT plot with spurs [13]**

### 1.4.3 EFFECTIVE NUMBER OF BITS

Linearity is a very important measure of the ADC’s performance. Since all the ADCs are not ideal there is always some non-linearity like the quantization noise, presence of harmonics and distortions in the dynamic characterization which limits the actual resolution of the ADC. This reduction in resolution is calculated using effective number of bits (ENOB). Ideal SNR calculation gives the exact resolution of the ideal ADC. From that calculation ENOB is done performing reverse engineering with the simulated SNR. The real-time resolution of an Analog to Digital Converter can hence be given as

\[
ENOB_{SNR} = -\frac{SNR - 1.76}{6.02}
\]  
\[ (1.11) \]
1.5 OBJECTIVE OF THIS THESIS

Traditional SAR ADCs have been the architecture of choice for medium-high resolution applications. The architecture itself makes high-performance, low power ADCs ideal for a wide variety of applications. Another notable feature of SAR ADC is that its power dissipation scales with sampling rate unlike flash and pipelined architectures which usually have constant power dissipation. This makes SAR ADC an ideal choice in low power applications. Though flash ADCs are fast it is harder to find flash ADCs with resolution more than 8 bits. Not only the number of comparators and resistors increase by a factor of 2 for every extra bit of resolution, but also the accuracy and matching between resistors need to be twice than before. Similarly, Pipelined architecture trade area for speed and Sigma-Delta converters trade speed for resolution. Hence SAR architecture has been chosen to be the ideal architecture for this design which accounts for countless applications needing high accuracy, moderate-high resolution and low power consumption.

The main limitations of conventional SAR ADCs are that they have moderate resolution and conversion rate. It includes a 1-bit comparator, N-bit DAC and produces N-bit digital output after N- clock cycles [7]. Hence to increase the conversion rate pipelining of ADCs was opted in this design. Pipelining is nothing but a parallel arrangement of number of ADC blocks which after certain latency produces N-bit output for every clock cycle. But pipelined ADCs are very hard to design as they need accurate residue generating circuits like analogue subtractors and multipliers which are hard to realize and takes up a lot of on-chip area. Hence a new architecture called Successive Approximation Pipelined ADC (SAP ADC) [14] was used to implement N-bit SAR ADC combined with merits of pipelining not only to make the conversion rate equal to that of the master clock frequency but also to eliminate the need for the traditional residue circuits which are inherent in conventional Pipelined ADCs. In [14] R2R DAC is used, this thesis is focusing on charge scaling DACs.
2. Successive Approximation Pipelined ADC

2.1 Design Overview

The block diagram of 8-bit SAP ADC with Charge scaling DACs is shown in Figure 14. It includes eight 1-bit comparators, digital/analogue delay circuits and charge scaling DACs (from 1 to 7 bits). The circular buffer array of sample and hold circuits and analogue switching matrix generates required eight analogue samples each delayed by one clock period. These analog samples are then fed to the comparators in a parallel fashion. The first comparator has a fixed reference value of $V_{ref}/2$ to find the MSB. This MSB is given as input to the second stage 1-bit CDAC to give an output of $V_{ref}/4$ or $3V_{ref}/4$. These reference voltages are fed to the input of the second comparator which compares the single clock delayed, sampled and held input values to the references from 1-bit DAC to generate the next most significant bit OUT7. The MSB and OUT7 are given as inputs to 2bit DAC present in stage 3 and this process continues. As it is evident, the successive approximation algorithm is applied in parallel here. Hence the SAP-ADC has a conversion rate and input sampling rate equal to clock frequency. This design also eliminates the sub-circuits inherent in traditional Pipelined ADCs which saves area and also the errors don’t get accumulated as each input conversion is done in parallel. It can be easily implemented in CMOS technology saving circuit area and power. The design also eases sensitivity to comparator offset and components mismatch. Hence, we can have an N-bit SAP-ADC produce N-bit output for each clock cycle after an initial latency of N-bits. 90nm CMOS technology is used to implement this ADC. A top-level schematic is given in Figure 15.
Figure 14 Block Diagram of 8-bit SAP ADC
Figure 15 Cadence Schematic of 8-bit Successive Approximation Pipelined ADC
2.2 Sub Circuit Design
2.2.1 Track and Hold Switch

As a first step a simple CMOS analog switch using a transmission gate with both PMOS and NMOS was designed and respective inputs and clocks are given. Widths of both PMOS and NMOS transistors individually were adjusted while simultaneously changing the output load capacitance. The main advantage of constructing a CMOS switch is to cancel both positive and negative errors. Time constant of the circuit is the product of ‘Ron’ and ‘\(C_{\text{total}}\)’ (load + parasitic) [15]. Hence time constant of a circuit can be reduced by reducing either Ron or \(C_{\text{total}}\) or both simultaneously. To decrease Ron we can vary the transistor parameters like width. Width is related inversely to Ron. Hence to decrease Ron we need to increase the width. But increasing width too much may influence \(C_{\text{total}}\) as \(C_{\text{total}} = C_{\text{load}} + C_{\text{parasitic}}\). The final term is parasitic capacitance and are related directly to width. Hence there should be a tradeoff in the increment of the widths such that it effects on Ron and not ‘\(C_{\text{total}}\)’. In this way time-constant can be reduced and circuit speed can be increased.

On the other hand, there are holding errors caused due to both charge induction and clock feed through. The design uses PMOS and NMOS dummies which are connected and controlled in an inverted way to induce opposing feedthrough. The hold capacitor ‘\(C_H\)’ shown in red is formed from the inherent parasitics on the output of the switch and input cap of the buffer circuit as show in Figure 16. There is no special capacitor used to hold the input to enable high sampling rates [16].

The circuit to the right is a Double sided common source active load (DSCSAL) buffer [17]. The normal source follower has been a classical circuit for implementing a unity gain buffer. However, since output is taken at source the device threshold varies due to body effect as the input increases. Hence this special architecture is used to provide wide operating range with 3-dB bandwidth of up to 3GHz and gain of approximately 0dB. The input capacitance is 10fF and it can drive a load of 200fF. The input and output offsets are adjusted to be approximately 0.6V and can be operated up to 230mV on both sides of the offset (0.6V) with less than 2% gain variation.
Figure 16 Cadence Schematic of Track and Hold Switch
In the track and hold circuit shown in Figure 16, lengths of both PMOS and NMOS are 100nm. The widths of the transistors are adjusted in such a way that the switch can drive a load of 250fF and can be operated at 1GSPS. Figure 17 shows the output waveform of the T/H circuit with 1ns out of phase clocks for tracking and holding a 100MHz input sine wave. The input is at an offset of 600mV with an amplitude of 200mV.

2.2.2 Analog Comparator

Comparator compares two signals present at its input. The output polarity is either high or low depending upon the signals present at differential inputs. The signals are essentially analog in nature and hence the comparator is also called 1-bit ADC. If the analog input present at the input of the positive terminal is greater than that of the input present at the negative terminal a logic high is produced at the output. If the voltage present at the negative input terminal is greater, then the output would be a logic low.

For achieving the above phenomenon two types of architectures are used to construct the comparators. They are Open Loop Comparators and Regenerative comparators. Open loop comparators are generally achieved with a two stage Op-amp as shown in Figure 18.
Figure 18 Cadence Schematic of two stage Open Loop Comparator

The regenerative comparators generally employ a positive feedback as shown below.

Figure 19 Regenerative Latch Comparator [111]
Some of important performance metrics of a comparator are described below.

- Resolution is the minimum amount of input change needed to yield a correct output. This is generally degraded by noise and offset factors in a non-ideal comparator.
- Speed is the maximum clock frequency at which the comparator can correctly respond to the subsequent 1-LSB input after a full-scale overdrive.
- Gain of the comparator is the ratio of full-scale reading to the smallest resolvable voltage of the comparator.
- Offset voltage is the voltage produced at the output of comparator when the two inputs are connected. Ideally the output and hence the offset should be zero.
- Slew rate is the output driving capability of the comparator and is related to the input applied differential voltage. When large input voltage is applied propagation delay of the comparator is improved.

The first stage of an open loop comparator is a differential amplifier stage with NMOS input differential pair and PMOS diode connected loads followed by a current sink inverter stage. The main advantage of an open loop comparator is that if enough gain is provided resolution of the comparator increases. But as gain increases bandwidth of the comparator decreases which reduces the speed of the comparator. Thus, there is always a trade-off between speed and resolution of the comparator.

But in the case of regenerative latch comparator due to the employment of positive feedback the circuit can be very fast if the input resolvable voltage is large enough to overcome the large offset voltages which arise due to mismatch [18] of the cross coupled transistors.

Hence the optimal solution is to combine the open loop and regenerative latch configurations to get good resolution and speed that is to be able to operate the circuit with high bandwidths. If enough amplification is provided by the pre-amplifier for the latch to overcome the input offset voltage and operate in exponential region of input/output characteristic to achieve both speed and resolution. Hence the design shown in Figure 20.
Figure 20 Cadence schematic of Comparator Design

Figure 21 Comparator Output Waveform at highest resolvable reference (799mV)
Figure 22 Comparator Output Waveform at lowest resolvable reference (401mV)

*Figure 21* and *Figure 22* shows the output waveforms of the comparator. All the lengths of the transistors used in open loop and regenerative blocks are 100nm. The Pre-amp is designed to have a gain of 40dB to cancel the offset of the following D-flipflop. The input is a sine wave with 600mV offset, 200mV amplitude and 100MHz frequency. The reference voltage is varied from a DC value of 401mV to 799mV to verify the comparator is working for all inputs in the range from 0.4V to 0.8V. *Figure 21* shows the output of the comparator when the reference is placed at 799mV and *Figure 22* shows the output of the comparator when the reference is placed at 401mV. The delay of the comparator is approximately 300ps and the minimum resolvable voltage is 1mV which is adequate for this design.
2.2.3 Analog Delay

If space is not a criterion, then analogue delay can be introduced through a sufficient length co-ax cable. But it is always advisable to generate delay using active components to save circuit space. The below described phenomenon shows how to generate perfect track and hold outputs each delayed by exactly one clock period.

*Figure 16* shows the implementation of analog switch which uses dummy transistors to cancel out the feedthrough problems that exist in the normal CMOS switches [19]. *Figure 17* shows the output waveform of the Track and hold switch. The sampled and held signal is then passed through the buffer which drives load capacitances without affecting the actual wave. Buffer can be realized in several ways. A normal source follower has been a unity gain buffer for many applications. Owing to the linearity and gain accuracy problems it cannot be used. Another common architecture is a normal op-amp connected in unity gain configuration [20]. The problem with this architecture is reduced input range as it is required to keep all transistors in saturation. This gets extremely difficult especially in sub-micron technologies. Also, it is hard to realize op-amps operating at such high bandwidths. As the open loop gain, must be very high to close the loop, this has a direct tradeoff with bandwidth. Also, the use of compensation capacitor to stabilize the op-amp reduces the bandwidth. Hence a special architecture called Double Sided Common Source active load which was developed from basic cascading of Common source amplifiers is used to achieve GHz operating frequencies and high gain accuracies over a wide input range.

![Figure 23 Track and hold Buffer circuit](image-url)
The circular buffer array consists of ten Track and hold circuits which generates eight analog samples each delayed by one clock period. To control the 10 to 8 switching matrix we need ten control clock phases. This can be achieved by using ten D-flipflops connected in loop [21] as shown in Figure 24
The track time and hold times of these pulses are greater than one sample period. If $T$ is the time-period of the master clock, then an output sample is produced every $T$ seconds. These $T/H$ control clocks cycle around the array in a circular manner [19] as shown in Figure 25. For each control phase, the sampled value in time $T$ seconds is held constant for period of $9T$ seconds as shown.

![Figure 25 Circular Control Clocks](image)

**Figure 25 Circular Control Clocks.**

The Analog phase switch matrix shown in Figure 26 acts as a 10 to 8 multiplexer. It has a group of analog switches arranged as shown in ten rows and eight columns. The inputs to these switches are 10 control clock phases generated by the pulse generator and 10 outputs from the T/H circuits. It has 8 outputs. For each phase sample, there is only one clock period to sample the input and nine clock periods of hold time. It is controlled in such a fashion that only one switch operates at any given time in each column and the outputs from the matrix are eight sampled and held signals each delayed by one clock period as shown in Figure 28.
Figure 26 Analog Switching matrix
The entire implementation of the above stated concept has been shown in Figure 27.

**Figure 27 Circular T/H Buffer Array**

From left in Figure 27 the first block is pulse generator which generates 10 control clock phases as described above. The outputs are fed into T/H circuits which are basically analog switches mentioned previously. These are followed by an array of DSCSAL buffers to drive the switches present in the 10 by 8 MUX shown in Figure 26. Finally, the buffered outputs from the switching matrix are generated to drive the next stage Comparators.
Figure 28 shows the final outputs from the Circular buffer array, input sine wave and the master clock signal. By defining the pulse width or duty cycle of the preset signal which is used to generate the control clock phase in the pulse generator block described above, we can control the delay between each sampled and held sine wave. The outputs in the above figure are each delay by 1 clock cycle.

The main advantage of the Circular buffer architecture is that as the inputs are applied in a parallel fashion to the T/H circuits, the errors from each T/H do not get accumulated as they do in a serial T/H delay line. Also, each output can be separately controlled and can be precisely delayed to the required value from the previous one as is obvious from Figure 28.
2.2.4 Digital Delay

A simple shift register can be used as a digital delay provided both the clock and input signal are applied at the same instant of time. In the figure shown above the “data in” has been delayed by one clock period as it has only one flip-flop. Similarly, as the number of flip-flops increase in the shift register, the input gets delayed by so many clock periods.

A simple D Flip-flop can be implemented using two transistors connected back to back with one transmission gate driving the input ‘D’ to the inverter loop and another transmission gate present in the loop itself. The gates are operated using complementary clocks so that only one transmission gate is turned on at a time. Figure 30 shows the implementation of the D flip-flop using cadence 90nm process where all the lengths of transistors are fixed to 100nm. The design is based upon the above discussed concept with a slight change to include the active low reset. So, the flip-flop functions normally if the reset is ‘1’ and resets if reset is set to ‘0’. Figure 31 shows the transient analysis output for the D flip-flop. The input applied is a pulse with high and low voltage values of 1.2V and 0V respectively. The time-period of the clock is 100ps and the input frequency is 1GHz. It is observed that the propagation of delay the D flip-flop is 100ps with a rise time and fall times of approximately 50ps each.

Figure 32 and Figure 33 shows the implementation of digital delay and transient output waveforms respectively. When a clock of 2ns is applied a delay of 2ns is obtained at the end of second stage. The delay value can be controlled with time-period of the clock.
Figure 30 Cadence schematic of D-Flip flop with a reset switch

Figure 31 DFF output waveform
Figure 32 Digital Delay implemented with Shift register using Flip-Flops

Figure 33 Digital Delay output waveform
2.2.5 Charge Scaling DAC

There are many different types of DAC architectures such as voltage scaling, current scaling, charge scaling etc. All these parallel DAC architectures produce the output analog voltage in a single clock cycle. There are also many configurations of a serial DAC which takes N clock cycles to produce the output. But in SAR ADCs where the binary search is carried out, usually parallel DACs are used to finish one complete analog to digital conversion process within N clock cycles. Current scaling DAC’s disadvantages include the required area and poor matching of resistors that limit the resolution below 10 bits to which R-2R is the alternative. But the main disadvantage of R-2R is the requirement of large number of resistors and switches, limiting the resolution to about 7 bits or less and the speed will also be much lower in this architecture. The remedy to this area consumption is the use of charge scaling method which consists of a capacitor array with a combination of switches that distributes the circuit’s total charge among the capacitors. But even in this architecture, as the resolution increases, the value of the capacitors required increase to the power of two. Thus, matching becomes tough and a lot of area is used up. Hence split capacitor architecture [22] or the segmented DAC approach shown in Figure 34 has been used as a counter act to the problem. Figure 34 shows the cadence schematic of 7-bit CDAC which has been designed in 90nm CMOS with a supply voltage of 1.2v. b0-b3 correspond to the LSB array and b4-b6 correspond to the MSB array. The architecture itself has been explained in detail in previous sections. Depending on the incoming logic value of each bit the switch chooses which voltage the capacitor needs to be charged to. If input bit is logic ‘1’ capacitor is charged to ‘$V_{ref^+}$’ and ‘$V_{ref^-}$’ when input is logic ‘0’.

The main bottleneck of CDACs has been operating bandwidths although it has huge advantages like area and power consumptions when compared to other architectures. In traditional SAR ADCs, the output of the DACs are directly fed to the comparators in [23] and [24]. These induce errors as the input capacitance of the comparators hugely affect the matching between capacitors in the original CDAC array. As a solution output buffers using op-amps and OTAs connected in unity gain configuration are used in [25] and [26]. But such architectures only operate at MS/s as it is very hard to achieve op-amp buffers operating at such high bandwidths. This design tackles the problem using a special kind of buffer called DSCSAL buffer [17] whose properties are discussed in section 2.2.1.
This buffer is designed to achieve very high unity gain bandwidth, large output to input capacitance ratio. It can drive a load of 230fF with less than 2% variation in gain for input amplitudes of up to 230mV.

Figure 34 Segmented CDAC Approach
The secret to the increase in bandwidth over other unity gain buffers lies in the elimination of compensation capacitor inherent in traditional op-amps using active load design. The design has a diode connected load and common source transistors just like a normal differential amplifier. But the current sink is replaced with a transistor which operates in linear region as a resistor. The process is called source degeneration [27]. With very less $V_{ds}$ across the source degeneration transistor just enough to keep the common source transistors in saturation, this topology facilitates operation of buffer for low rail voltages (1.2V in this case). Also, the double-sided architecture provides minimal offset error over very high operating frequency range.

The unit capacitance for the CDAC is chosen to be 100fF. All the other capacitors can be implemented as a parallel combination of the unit capacitance. There is also a coupling capacitor and bias resistor between the CDAC array and DSCSAL buffer. This is to bias the output from the capacitor array at exactly 0.6V offset so that the buffer produces the same voltage levels at output with an offset of 0.6V even when driving higher capacitive loads. In simple terms the load has been isolated from the capacitive array to keep their matching intact. The value coupling capacitor is chosen to be 1.59nF. This value allows a minimum voltage drop across it and facilitates the ADC operates in full base band region 1MHz to 125MHz.

Figure 35 Simple switch using pass transistors for CDAC design
The simple switch used in the CDAC shown in Figure 35 just needs two transmission gates which are operated using the selection signal ‘vin’ and an inverter. Depending on the logic values of ‘vin’ only one transmission gates is ‘ON’ at a single time and the corresponding input value to the transmission gate is connected to the output.

Figure 36 shows the output of a transient analysis performed using cadence ADEL window on the switch above. The widths of the transistors can be adjusted to drive the desired load. The switch in shown in Figure 35 has been optimized to drive a capacitive load of 1pF. The analysis is performed with a clock frequency of 1GHz. The rise time and fall time of the switch are found out to be 150ps and 100ps respectively.

![Switch output waveform showing control voltage and output.](image)

Figure 36 Switch output waveform showing control voltage and output.
Figure 37 7-bit Split Capacitor CDAC dividing input range (0.4V to 0.8V) to 128 levels.
Figure 38 4-bit CDAC output waveform for full scale input range (0.4v to 0.8v)

Figure 37 shows the output waveform for the 7-bit CDAC and Figure 38 shows the output waveform for the 4-bit CDAC for a full-scale input range. For the 7-bit segmented CDAC, the input b6 which is the most significant bit (MSB) is applied a pulse input of 128ns and higher and lower amplitudes of 1.2V and 0V respectively. The inputs to all other lower bits are given in such a way that they are equal in amplitudes but the time-periods are reduced to the power ‘2’ for each lower bit. The same is done for the 4-bit DAC. This is to verify the full scale operating range of the DAC. From Figure 38 the 4 bit DAC divides the entire range from 0.4v to 0.8v to 16 levels. The accuracy of each level is verified with the theoretical value. The error is only 0.1% which means the DACs are fairly accurate. The simulations are performed driving 100fF caps at the load to emulate the Comparators that are to be driven by these DACs in the main circuit. The top and bottom level values are plotted in the waveform.
3. RESULTS
3.1 8-bit SAP-ADC test bench

The 8-bit SAP-ADC once completed outputs data at every clock period after an initial latency of eight clock periods. Now a test bench to verify the functionality and the dynamic performance of the SAP-ADC was created using Cadence ahdILib. This library contains many circuits built using Verilog-A code. The input is given to the SAP-ADC under test and the output from SAP-ADC is given to the ideal 8-bit DAC added from ahdILib to the test bench as shown. The same input is also given to the Ideal 8-bit ADC from ahdILib and the output from the Ideal ADC is fed into another Ideal 8-bit DAC. These two outputs are then compared.

Figure 39 Block diagram of SAP-ADC test bench

Another way to find the correctness of the digital output bits produced by the ADC under test is to perform a weighted sum on the output bits. If $V_{in}, V_{out}, V_{ref}$ are the input output and reference voltages of the ADC respectively, then $V_{out}$ can be calculated as follows. As this design has both positive and negative references, the range is calculated as show in equation (3.1).
\[ V_{\text{range}} = (V_{\text{ref}+}) - (V_{\text{ref}-}) \]  \hspace{1cm} (3.1)

Equation (3.2) shows the method to calculate weighted sum from the digital output bits from the ADC.

\[ V_{\text{out}} = V_{\text{ref}-} + \left[ \text{MSB} \times \frac{V_{\text{range}}}{2} + (\text{MSB}-1) \times \frac{V_{\text{range}}}{4} + \ldots + \text{LSB} \times \frac{V_{\text{range}}}{2^N} \right] \]  \hspace{1cm} (3.2)

\textbf{Figure 40} shows the weighted sum plot for 8 -bit SAP-ADC under test. This entire calculation can be performed in the calculator present in the ADE window after running the transient analysis on the ADC. The simulation has been run for 10 micro seconds. The output of the SAP-ADC takes 1 micro second to settle. Then after eight clock cycles of initial latency there are 8 bits produced for every clock cycle. This can be seen in \textbf{Figure 41}.

\textbf{Figure 40} Weighted sum plot for the 8-bit SAP-ADC with 100MHz i/p and 1GHz clock.
Figure 41 Digital outputs (out1 to out8) of 8-bit SAP-ADC with 100MHz i/p and 1GHz clock.
3.2 Dynamic Performance

Spur free dynamic range (SFDR) is an important parameter to assess the performance of high speed converters which are to be used in the real-world applications. The procedure for obtaining the SFDR for the 8-bit SAP-ADC is as follows.

An input sine wave is applied to the 8-bit SAP-ADC and the output bits “out1” to “out8” are used to calculate the weighted sum equation of the ADC. Weighted sum is nothing but the representation of output digital bits in terms of the input sine wave applied which is shown in Figure 40. Calculator tool in cadence is used to plot the weighted sum against the input. Then DFT is performed on this weighted sum equation to obtain the FFT plot. The dB20 plot is taken for the FFT thus obtained which can be seen in Figure 42.

![Figure 42 FFT plot of 8-bit SAP-ADC showing the SFDR of 52.53dB](image_url)
Fourier analysis is a powerful tool to graphically represent the signal, noise levels and other undesired harmonics present in the desired frequency range of operation. To reduce the distortion in the FFT plot the input frequency and sampling frequency should be set up to a relationship. The minimum requirement being always that sampling frequency ‘$f_s$’ should be twice to that of the signal frequency ‘$f_{in}$’ to avoid aliasing and aid perfect reconstruction at the output, an additional improvement technique called Coherent sampling which is used to fit ‘M’ number of input cycles into ‘N’ FFT bins is used here. This reduces the distortion in the FFT plot. The ratio itself is shown in equation (3.3)

$$\frac{f_{in}}{f_s} = \frac{M}{N}$$  \hspace{1cm} (3.3)

The N value is set to power of two, with the number in the power being the resolution of the converter. (Here $2^8= 256= N$). First the value of M is calculated for the given $f_s$ and $f_{in}$ putting N=256. Then the value obtained for M is corrected to the nearest prime number and substituted back in the above equation. This time we calculate for $f_{in}$ and the obtained value is found to be slightly different from the initial value.

In Figure 42. the transient analysis is run up to 10 micro seconds. The 8-bit SAP ADC takes 1 micro second to settle to the correct output. The input and sampling frequencies are 100MHz and 1GHz respectively. Rectangular window with an interval from 2.8us to 3.44us is chosen to accommodate 61 cycles of input. This is the value of ‘M’ in equation (3.3). In general, it is good to choose odd prime values for ‘M’. The value for ‘N’ in equation (3.3) is chosen to 1024. This is usually a power of 2. If we increase the value of ‘N’, the noise floor of the FFT plot gets better but the amplitudes of spurs remain constant. From the plot, the fundamental or the first harmonic frequency of 100MHz is at -13.64dB and the next largest spur is at -66.17dB. So, the SFDR is calculated to be 52.53dB and SNR is measured to be 47.72dB which suggests that the architecture supports 8-bit resolution.
3.3 Power Dissipation and Performance

The total power dissipation by the 8-bit SAP-ADC is the sum of powers consumed by all the sub-circuits present. Table 3.1 shows overall power consumption by all the sub-circuits and total power consumed by the 8-bit SAP-ADC is measured to be 22.6mW

Table 3.1 Average sub-circuits Power

<table>
<thead>
<tr>
<th>Sub- Circuit</th>
<th>Quantity</th>
<th>Average Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital delay</td>
<td>36</td>
<td>3.024</td>
</tr>
<tr>
<td>Track and hold buffer array</td>
<td>1</td>
<td>2.186</td>
</tr>
<tr>
<td>Comparator</td>
<td>8</td>
<td>5.696</td>
</tr>
<tr>
<td>1-bit DAC</td>
<td>1</td>
<td>1.2705</td>
</tr>
<tr>
<td>2-bit DAC</td>
<td>1</td>
<td>1.2905</td>
</tr>
<tr>
<td>3-bit DAC</td>
<td>1</td>
<td>1.7495</td>
</tr>
<tr>
<td>4-bit DAC</td>
<td>1</td>
<td>1.7962</td>
</tr>
<tr>
<td>5-bit DAC</td>
<td>1</td>
<td>1.845</td>
</tr>
<tr>
<td>6-bit DAC</td>
<td>1</td>
<td>1.8869</td>
</tr>
<tr>
<td>7-bit DAC</td>
<td>1</td>
<td>1.9214</td>
</tr>
<tr>
<td>8-bit SAP ADC</td>
<td>1</td>
<td>22.66</td>
</tr>
</tbody>
</table>

While all the static and dynamic parameters INL, DNL, SFDR etc. can be used to measure the performance of a converter, Figure of merit (FOM) can be used to combine several performance metrics to get one single number. The below equation suggests an important tradeoff between speed, power consumption and ENOB.

\[
\text{FOM} = \frac{\text{Power}}{2\text{ENOB}_{\text{SNR}}f_s} \quad (3.4)
\]

The values for the power and \(f_s\) are 22.6mW and 1GHz respectively. Plugging the value of SNR, into equation (1.1) \(ENOB_{SNR}\) is calculated to be approximately 7.63 which is decent for this design. As this is not an ideal ADC the value never reaches 8 bits due to the presence of quantization error. Substituting the three values into the equation (3.4) gives a figure of merit of 65.52fJ/conversion. A few modern SAR ADCs are designed to consume power in microwatts but their sampling rates are in KS/s and some managed to sample at MS/s. This design samples at GS/s sacrificing a bit more power. Hence this is an acceptable power to speed tradeoff.
4. Conclusion and Future Work

4.1 Conclusion

An 8-bit SAP ADC using charge scaling DACs is implemented which incorporates a successive approximation algorithm in a parallel pipelined architecture. Conversion rate of the SAP ADC equal to the clock frequency (1GHz) is achieved for an input frequencies of up to 125MHz.

4.2 Future Work

A few things could be done to increase the performance and accuracy of the SAP ADC. Firstly, as the design includes all separate blocks, each block could be further optimized. This could be done in terms of power consumption and accuracy for the CDAC, designing a faster comparator with higher resolution etc. A designated bandgap reference could be designed to provide stable bias to comparators, buffers and other components used in the design. Main limitations of SAR ADC include speed (conversion/sampling rate) and accurate component matching when the resolution starts going above 10 bits. The first limitation is successfully tackled in this design. But as the resolution increases it is good to have calibration and digital trimming mechanisms. This is a huge area which could be investigated for each component in specific. Techniques like dynamic element matching could be incorporated to counteract PVT variations and improve static performance the converters.
Bibliography


