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PWM Buck Converter as a Dynamic Power Supply for Envelope Tracking and Amplitude Modulation

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PWM BUCK CONVERTER AS A DYNAMIC POWER SUPPLY FOR ENVELOPE TRACKING AND AMPLITUDE MODULATION

A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Engineering

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Abstract


Modern energy transmission and signal reproduction techniques rely upon power amplifier (PA) architectures that must operate with high efficiency. Current-source PAs are linear but inherently inefficient; switch-mode PAs are efficient-yet-nonlinear systems, often lacking an efficient means of amplitude modulation (AM) for power transmission. A promising technique for addressing these problems involves replacing the fixed PA supply voltage $V_{DD}$ with a controlled, variable voltage provided by a dynamic power supply. High-efficiency envelope tracking and amplitude modulation can thereby be provided to both current-source and switch-mode PAs, respectively. This work presents a pulse-width modulated (PWM) dc-dc buck converter for use as the core power stage of a dynamic supply. Although buck converters typically function as fixed-output supplies, this work provides new theoretical dc analysis for operation wherein the output voltage is controlled and variable over a wide, continuous range. A new design procedure for the variable-output PWM dc-dc buck converter is derived. The new dc analysis and design procedure are verified experimentally. Open-loop ac characteristics, such as transient response, frequency response, and dynamic modulation efficiency are assessed via simulation and experimental measurements. The variable-output buck converter is found to operate as designed, with bandwidth dependent upon a sufficiently high PWM switching frequency $f_s$. Within this bandwidth, minimal modulation distortion is observed, measured efficiency is greater than 90%, and supplied power-on-demand is verified.
## Contents

1 Introduction ........................................ 1
   1.1 The Need for High-Efficiency Power Conversion ................. 1
   1.2 Dynamic Power Supplies ........................................ 1
       1.2.1 Current-source PAs ....................................... 2
       1.2.2 Switch-mode PAs ......................................... 3
       1.2.3 Topological Approaches ................................ 4
   1.3 Literature Search ........................................ 4
   1.4 Research Focus and Rationale .................................. 6
       1.4.1 Buck Converter as Dynamic Supply .......................... 6
       1.4.2 Rationale Behind This Work ................................ 7
   1.5 Research Objectives ........................................ 8
   1.6 Anticipated Contributions .................................... 9

2 DC Analysis and Design ................................ 10
   2.1 CCM Operation Requirement .................................. 10
   2.2 Effect of Total Converter Efficiency ........................... 12
   2.3 Inductor Current and CCM-DCM Boundary of Variable-Output Buck
       Converter ..................................................... 13
   2.4 Output Ripple Voltage ....................................... 19
   2.5 Device Stresses .............................................. 23
       2.5.1 Switch .................................................... 23
       2.5.2 Diode ..................................................... 27
       2.5.3 Inductor .................................................. 28
       2.5.4 Capacitor ................................................ 28
   2.6 Variable Switching Loss ..................................... 29
   2.7 Total Converter Efficiency ................................... 34
**List of Figures**

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Block diagram of RF power amplifier with envelope-tracking supply.</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>Block diagram of RF power amplifier with amplitude modulation.</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>PWM buck converter with diode rectifier.</td>
<td>7</td>
</tr>
<tr>
<td>4</td>
<td>Standard diode-rectified buck converter.</td>
<td>10</td>
</tr>
<tr>
<td>5</td>
<td>CCM versus DCM converter operation.</td>
<td>11</td>
</tr>
<tr>
<td>6</td>
<td>CCM-DCM boundary of inductor current.</td>
<td>14</td>
</tr>
<tr>
<td>7</td>
<td>Waveforms of $\Delta i_L$, as $D$ is varied, for (a) fixed-output and (b) variable-output buck converters operating in CCM.</td>
<td>16</td>
</tr>
<tr>
<td>8</td>
<td>Ripple currents and voltages of CCM buck converter output stage.</td>
<td>20</td>
</tr>
<tr>
<td>9</td>
<td>Piecewise linear model of p-n junction diode in forward-biased mode.</td>
<td>24</td>
</tr>
<tr>
<td>10</td>
<td>Possible waveforms of switch current $i_S$ where $I_{SM_{\text{max}}}$ does not occur at maximum output.</td>
<td>25</td>
</tr>
<tr>
<td>11</td>
<td>Nominal output capacitance $C_{\text{oss}}$, nominal reverse transfer capacitance $C_{\text{rss}}$, and output capacitance $C_O = C_{\text{oss}} - C_{\text{rss}}$ of Si power MOSFET (plot courtesy of Microsemi Corporation).</td>
<td>29</td>
</tr>
<tr>
<td>12</td>
<td>Change in $V_{DS}$ as a function of $D$.</td>
<td>30</td>
</tr>
<tr>
<td>13</td>
<td>Normalized effect of nonlinear $C_O$ on switching loss in low- to medium-power dynamic buck converters with Si MOSFET switch ($V_{DS} = 25$V, $V_B \leq 0.9$V) and $V_F \leq 0.9$V.</td>
<td>33</td>
</tr>
<tr>
<td>14</td>
<td>Normalized comparison of exact value and approximation of dynamic switching loss $P_{SW}$ for $V_B = V_F = 0.9$V.</td>
<td>34</td>
</tr>
<tr>
<td>15</td>
<td>Asynchronous buck converter with device parastics and equivalent device models.</td>
<td>35</td>
</tr>
<tr>
<td>16</td>
<td>Comparison of iterative ($\eta$) and simplified ($\eta'$) calculated efficiency characteristic of dynamic buck converter.</td>
<td>39</td>
</tr>
</tbody>
</table>
17 Dynamic buck converter power stage design for $3 \leq V_O \leq 23$ V, $V_r \leq 140$ mV. ........................... 47
18 Dynamic buck converter power stage design with high-side gate driver. 48
19 Test bench for dc and ac circuit measurements. ....................... 49
20 Currents and voltages measured for dc characterization of variable-output buck converter design. .......................... 50
21 Theoretical total efficiency of dynamic buck converter design over 20-V operating range. ............................................. 51
22 Comparison of measured and theoretical total efficiency of dynamic buck converter over 20-V operating range. .............. 52
23 Theoretical total converter efficiency matched to measured efficiency by varying theoretical parasitics of switch and diode. ........ 53
24 Theoretical dc transfer characteristic of variable-output voltage buck converter design. ............................................. 54
25 Comparison of driver input $v_{PWM}$ (top) and gate drive $v_{GS}$ (bottom) signals, showing delay and duty cycle loss of over 1%. ........ 55
26 Comparison of measured and theoretical dc transfer characteristics of variable-output voltage buck converter. ....................... 55
27 Experimental disparity between $D$ and $1 - D_{DS}$ contributing to non-linearity in measured $V_O(D)$ transfer characteristic, $V_O \cong V_{min}$. .... 56
28 DC transfer characteristic of variable-output buck converter, $0 \leq V_O \leq V_I$. ......................................................... 57
29 Theoretical peak-to-peak inductor current over operating range of variable-output buck converter design. ....................... 58
30 Comparison of measured and theoretical peak-to-peak inductor current for full operating range of converter. ....................... 59
31 Theoretical peak-to-peak inductor current matched to measured values by compensating for +7% tolerance in actual value of L. 
32 Theoretical inductor current waveforms of dynamic buck converter design, for $V_O = 3$ V, $V_O = 13.4$ V, and $V_O = 23$ V.
33 Measured inductor current waveforms of dynamic buck converter for (a) $V_O = 23$ V, (b) $V_O = 13.4$ V, and (c) $V_O = 3$ V.
34 Theoretical output power of dynamic buck converter design.
35 Comparison of measured and theoretical output power of dynamic buck converter design.
36 Measured output ripple voltage of dynamic buck converter design over full range of output.
37 Measured output ripple voltage compared to theoretical ripple for full operating range of dynamic buck converter.
38 Measured maximum current stresses of (a) switch $I_{SM_{max}}$, (b) diode $I_{DM_{max}}$, and (c) inductor $I_{LM_{max}}$, $V_O = 23$ V.
39 Measured maximum voltage stresses of (a) switch $V_{SM_{max}}$, (b) diode $V_{DM_{max}}$, and (c) capacitor $V_{CM_{max}}$.
40 Schematic of simulated dynamic buck converter with PWM generator.
41 Simulated ideal op-amp ramp comparator.
42 Simulated ideal ramp comparator (a) non-inverting input $v_{REF}$ at $f_m = 100$ Hz and (b) inverting input $v_{ramp}$ at $f_s = 1$ MHz.
43 Simulated PWM generation, via ideal ramp comparator, for (a) $D = 0.846$, (b) $D = 0.477$, and (c) $D = 0.127$.
44 Simulated ideal gate driver.
45 Simulated dynamic buck converter power stage.
46 Simulated $P_i$, $P_o$, $v_{REF}$, and modulated output voltage $v_O$ of dynamic buck converter, $f_m = 50$ Hz, $h = 1$. 
Simulated input $v_{REF}$ and output $v_O$ of dynamic buck converter, $h = 1$, for (a) $f_m = 100$ Hz, (b) $f_m = 1$ kHz, (c) $f_m = 10$ kHz. 86

Simulated transient response of dynamic buck converter, demonstrating (a) rise time $t_r = 33.1 \mu s$ and (b) fall time $t_f = 272.3 \mu s$. 87

Simulated frequency response of dynamic buck converter, $h = 1$. 88

Simulated input $v_{REF}$ and output $v_O$ of dynamic buck converter with reduced modulation index $h = 0.5$, for (a) $f_m = 100$ Hz, (b) $f_m = 2$ kHz, and (c) $f_m = 20$ kHz. 89

Test and measurement setup for ac characterization of dynamic buck converter design. 90

Measured input $v_{REF}$ (lower) and output $v_O$ (upper) waveforms of dynamic buck converter, $h = 1$, for (a) $f_m = 100$ Hz, (b) $f_m = 1$ kHz, (c) $f_m = 10$ kHz. 91

Measured transient response of dynamic buck converter, demonstrating (a) rise time $t_r = 38 \mu s$ and (b) fall time $t_f = 290 \mu s$. 92

Measured frequency response of dynamic buck converter, $h = 1$. 93

Measured input $v_{REF}$ (lower) and output $v_O$ (upper) waveforms with reduced modulation index $h = 0.5$, for (a) $f_m = 100$ Hz, (b) $f_m = 2$ kHz, and (c) $f_m = 20$ kHz. 94

Measured frequency response of dynamic buck converter, $h = 0.5$. 95

Measured modulated (a) input power $P_i$ and (b) output power $P_o$ waveforms of dynamic buck converter, $f_m = 50$ Hz, $h = 1$. 96

Composite overlay of measured $P_i$ and $P_o$ waveforms for $f_m = 50$ Hz, $h = 1$, demonstrating $\eta_m = \frac{P_{o(\text{AV})}}{P_{i(\text{AV})}} = 0.912$. 97

Measured $P_i$ and $P_o$ waveforms for (a) $f_m = 100$ Hz, (b) $f_m = 1$ kHz, and (c) $f_m = 10$ kHz. 98
Measured $P_i$ and $P_o$ waveforms for $f_m = 100$ kHz, showing modulated power approaching dc.

Measured $P_i$ and $P_o$ waveforms with reduced modulation index $h = 0.5$, for (a) $f_m = 100$ Hz, (b) $f_m = 1$ kHz, and (c) $f_m = 10$ kHz.

VRF148A Si RF power MOSFET, $r_{DS(on)} \cong 4 \Omega$, $C_{oss} = 40$ pF, M113 direct-mount package.

EPC2012 GaN-on-Si “eGaN” FET, $r_{DS(on)} = 100$ m$\Omega$, $C_{oss} = 73$ pF, die-packaged.

Comparison of $v_{DS}$ between EPC2012 GaN-on-Si and VRF148A Si power FETs, $f_s = 10$ MHz.

Transformer-coupled high-side driver with charge pump.

Unloaded output $v_{GS}$ of transformer-coupled discrete driver, $f_s = 2$ MHz, for (a) $D = 0.8$, (b) $D = 0.5$, and (c) $D = 0.2$.

Prototype mounting for LTC4440-5 high-side gate driver.

Schematic of driver subcircuit for power stage.

Loaded output $v_{GS}$ of LTC4440-5-based driver subcircuit, $f_s = 2$ MHz, for (a) $D = 0.8$, (b) $D = 0.5$, and (c) $D = 0.2$.

Prototype dynamic buck converter (a) layout and (b) completed test PCB.
List of Tables

1  Summary of dynamic supply techniques presented in literature . . . . 5
2  Experimental error in measurements of dc operating characteristics . 71
3  Critical specifications of variable-output buck converter design . . . . 72
4  Selected high-speed, high-side driver ICs . . . . . . . . . . . . . . . . 110
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1 Introduction

1.1 The Need for High-Efficiency Power Conversion

Modern energy transmission and signal reproduction systems rely upon power amplifier (PA) technology that must exhibit high efficiency in addition to linearity and good frequency response. High-efficiency power transmission is particularly critical in wireless systems where size, weight, and/or energy consumption of the system are key design specifications. As a general rule, power consumption and system footprint both increase as efficiency decreases, resulting in larger hardware that is more costly to operate.

Much work has been devoted to increasing PA efficiency through use of improved devices and switch-mode amplifier topologies [67]. Both of these methods address the device-specific power losses inherent in semiconductors and passive and reactive components. However, once the limits of device physics and speed are reached, other approaches to PA system architecture must be sought in order to further enhance performance. Additionally, highly-efficient switch-mode PAs are nonlinear amplifiers that have no built-in means of providing efficient amplitude modulation (AM) required for many wireless standards. This research therefore centers around use of external circuitry to improve the efficiency of existing PA topologies such as Class A, B, D, E, etc.

1.2 Dynamic Power Supplies

One PA efficiency-enhancement technique that has shown significant promise is dynamic power management [1, 8, 14, 34, 37, 41, 53, 54, 56, 57, 59, 64, 65]. A dynamic
power supply, also called “dynamic drain bias” or “drain modulation”, refers to any means of varying the dc level of the PA supply voltage $V_{DD}$ as a function of time. The supply voltage can be toggled between two or more discrete levels, or varied continuously. Discrete dynamic supplies can be used with certain classes of power amplifiers to improve baseline efficiency [62], [69]. However, if the dynamic supply is continuously variable over a wide range of voltage, it can be used to improve the efficiency of linear PAs or provide efficient AM for a nonlinear PAs [2, 5, 67].

1.2.1 Current-source PAs

In the Class A, AB, B, C, and F family of PAs, the power transistor is operated as a dependent current source. The efficiency of this type of amplifier depends upon the ratio of the drain-to-source voltage fundamental component $V_m$ to the dc supply voltage $V_{DD}$, i.e.

$$\eta \propto \left(\frac{V_m}{V_{DD}}\right)^n$$

(1)

where $n = 1$ for Class B and C, $n = 2$ for Class A, etc. Therefore, to improve efficiency in these amplifiers, $V_{DD}$ can be made variable such that $\frac{V_m}{V_{DD}}$ is maximized at all times. This can be accomplished through the use of an efficient dynamic power supply to vary $V_{DD}$ and “track” the envelope of the output signal $v_O(t)$, as illustrated in Fig. 1.
1.2.2 Switch-mode PAs

In the Class D, DE, and E family of PAs, the power transistor is operated as a switch. With this type of amplifier, the output voltage magnitude does not depend upon the magnitude of the drive voltage signal $v_{in}(t)$. Amplitude modulation can therefore be achieved by simply varying $V_{DD}$, as seen in Fig. 2. It follows, however, that the efficiency of the transmitter depends upon that of the amplitude modulator. The AM circuit must also have sufficient linearity to accurately reproduce the desired envelope, just as the tracking supply must have enough linearity to follow the output envelope.
1.2.3 Topological Approaches

A continuously-variable dynamic power supply can function as an envelope tracker or amplitude modulator, depending upon the type of PA present. Both applications improve the operating efficiency of the entire system, to the extent that the supply itself operates efficiently.

Power circuits suitable for dynamic supply operation include:

- Pulse-width modulated dc-dc converters (buck, boost, SEPIC)
- Resonant power converters (Class D)
- Hybrid configurations (switch-mode converter or amplifier, in parallel with linear amplifier or regulator)

1.3 Literature Search

A comprehensive search of the existing literature has been conducted in order to quantify the state-of-art and identify gaps in published knowledge involving dynamic
power management. The full list of sources reviewed to-date is provided at the end of this document. Table 1 below compares existing dynamic supply topologies, specifications, and characteristics presented in the literature. This information drives the rationale for this research and provides a benchmark for evaluating the results.

### Table 1
**Summary of Dynamic Supply Techniques Presented in Literature**

<table>
<thead>
<tr>
<th>Topology</th>
<th>BW</th>
<th>$\eta$</th>
<th>Comments</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>Synchronous buck</td>
<td>$&lt; 200$ kHz</td>
<td>96% (peak)</td>
<td>High efficiency, Low bandwidth; $\eta$ varies with $P_O$</td>
<td>[59]</td>
</tr>
<tr>
<td>Multi-input buck</td>
<td>100 kHz</td>
<td>$&gt; 90 %$</td>
<td>High efficiency, Low bandwidth, complex control scheme</td>
<td>[44]</td>
</tr>
<tr>
<td>Buck + charge pump</td>
<td>1.1 MHz</td>
<td>75%</td>
<td>Fewer magnetic components, Low efficiency</td>
<td>[58]</td>
</tr>
<tr>
<td>Buck-boost</td>
<td>300 kHz</td>
<td>90% (peak)</td>
<td>High efficiency over wide range of $P_O$, Low bandwidth</td>
<td>[55]</td>
</tr>
<tr>
<td>Boost</td>
<td>1 MHz</td>
<td>74% (peak)</td>
<td>Small supply voltage ($V_I \leq V_O$), Significant trade-off betw. $BW$ &amp; $\eta$</td>
<td>[57]</td>
</tr>
<tr>
<td>Synchronous buck +</td>
<td>23 MHz</td>
<td>69%</td>
<td>Large bandwidth, Low efficiency</td>
<td>[65]</td>
</tr>
<tr>
<td>Class AB amp</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Multilevel converter +</td>
<td>10 MHz</td>
<td>90%</td>
<td>Large bandwidth, high efficiency, High $P_O$ only; non-trivial 2-bit switching req'd</td>
<td>[53]</td>
</tr>
<tr>
<td>linear amp</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Multilevel converter +</td>
<td>2 MHz</td>
<td>71%</td>
<td>Switched-cap converter (no inductor), High $P_O$ only; low efficiency</td>
<td>[41]</td>
</tr>
<tr>
<td>linear regulator</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Class D converter +</td>
<td>285 MHz</td>
<td>88% (peak)</td>
<td>Large bandwidth, good linearity, Efficiency varies greatly with $P_O$</td>
<td>[46]</td>
</tr>
<tr>
<td>linear amp</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Class E</td>
<td>7 MHz</td>
<td>95% (peak)</td>
<td>High $\eta$ at medium $P_O$; large $BW$, $\eta$ varies with $P_O$; fixed-frequency</td>
<td>[68]</td>
</tr>
<tr>
<td>Class E$^2$ (amp + rectifier)</td>
<td>186 MHz</td>
<td>60%</td>
<td>Large bandwidth, Low efficiency; discrete output levels</td>
<td>[69]</td>
</tr>
<tr>
<td>Single-Ended Primary Inductance Converter (SEPIC)</td>
<td>1.25 MHz</td>
<td>80%</td>
<td>High efficiency, Nonlinear; complex control scheme req'd</td>
<td>[47]</td>
</tr>
</tbody>
</table>

The most common dynamic supply topology is the hybrid approach, namely a switching converter (for high-efficiency operation) in parallel with a linear amplifier (for high bandwidth). Nonetheless, most of the documented designs exhibit some
degree of trade-off between efficiency and linearity; the efficiency of the supply itself often varies widely over the full range of output.

1.4 Research Focus and Rationale

This work opts to focus exclusively upon the pulse-width modulated (PWM) buck converter as a dynamic supply. It is the circuit most frequently utilized for envelope tracking in the literature, whether the approach is a stand-alone converter or a hybrid converter-with-linear stage. This type of dc-dc converter is highly versatile, efficient, and can provide for direct-proportion control of the output [66]. However, no literature reviewed as of this writing provides comprehensive circuit-level analysis or design procedures for a PWM buck converter operating as a dynamic supply.

1.4.1 Buck Converter as Dynamic Supply

The asynchronous buck converter shown in Fig. 3 uses a low-voltage pulse waveform $v_{GS}$ with duty cycle $D$ to drive a power MOSFET operated as a switch. Diode $D_1$ acts as a rectifier. As switch $S_1$ turns on and off over period $T$, the voltage at the source of the FET alternates between diode forward voltage $-V_F$ and converter dc input voltage $V_I$. At $t = 0$, $v_{GS}$ exceeds the FET threshold voltage, the switch closes, and the voltage at the cathode of the diode is $V_I$; at $t = DT$, $v_{GS}$ is zero, the switch opens, and voltage at the cathode is $-V_F$. This effectively “chops” $V_I$, generating a large-signal equivalent of the original $v_{GS}$ pulse sequence across $D_1$. The large-signal pulse waveform is then averaged and smoothed by the 2nd-order $L$-$C$ network, delivering dc output current $I_O$ to the load in direct proportion to $D$. In standard operation, $V_O$ is fixed and $D$ is varied to control $I_O$, thus compensating for fluctuations in $V_I$ and/or $R_L$. However, if $V_I$ and $R_L$ are fixed, varying $D$ will vary both $I_O$ and $V_O$, and the converter functions as a dynamic power supply. Operation of the transistor is purely switch-mode, minimizing the power dissipated by $S_1$ and maximizing efficiency.
of the circuit. The combination of high efficiency, $D^1$ direct-proportion control, and topological simplicity make the buck converter a promising candidate for dynamic supply applications.

![PWM buck converter with diode rectifier.](image)

**Figure 3:** PWM buck converter with diode rectifier.

### 1.4.2 Rationale Behind This Work

**Analysis and Design** The literature search reveals that none of the sources utilizing a buck converter present a detailed circuit analysis or design procedure. One source describes use of a dynamic PWM boost converter and does provide a modicum of discussion to this end [3]. However, in terms of analysis and design, boost is a distinct topology and the aforementioned work cannot be directly applied to buck. PWM buck converters have been thoroughly documented for “static” operation as regulated power supplies, i.e. where $V_O$ is kept constant despite variations in $V_I$ and load $R_L$ [66, 71]. The principle of operation for a dynamic power supply is roughly the opposite though, in that $V_O$ varies while $V_I$ and $R_L$ are nominally constant. The rationale that follows is that existing analyses and design procedures may not be applicable in the form presented. It is therefore relevant to the body of knowledge to

1. Determine what, if any, differences exist in dc and large-signal ac analyses of a dynamic PWM buck converter, as opposed to the standard mode of operation.
2. Determine differences in design considerations resulting from any new analysis.

3. Verify new analysis and design through experimental measurement.

**Practical Implementation**  The existing literature also leaves a relatively wide gap of knowledge with regard to the supporting circuitry required to implement a dynamic buck converter. All buck converters require non-trivial gate driver schemes, in order to provide a high-frequency pulse waveform to two “hot” points, i.e. the gate and source of the MOSFET. An examination of specific driver configurations, within the context of dynamic supply operation, is therefore useful to the body of knowledge.

### 1.5 Research Objectives

The purpose of this work is to provide comprehensive examination of a PWM buck converter used as a dynamic supply, whether for the purpose of envelope tracking or amplitude modulation. In order to accomplish this, it is necessary to:

- Perform a thorough dc analysis of a buck converter operated as a dynamic power supply.

- Derive a practical design procedure for a variable-output voltage buck converter, based on dc analysis.

- Identify suitable power transistors for use as a high-speed switch.

- Identify a suitable means of driving the switch at frequencies $\geq 1$ MHz.

- Experimentally verify the dc analysis and proposed design procedure.

- Evaluate large-signal ac characteristics of the dynamic buck converter via simulation and experimental measurements.

- Experimentally determine maximum modulation efficiency of the dynamic buck converter design, based on available technology.
• Experimentally determine maximum modulation bandwidth for the dynamic buck converter.

1.6 Anticipated Contributions

• To provide previously-unpublished circuit analysis of a buck converter used as a dynamic power supply.

• To provide a practical, component-level design procedure for a dynamic buck converter, comparable to existing procedures for static buck converters.

• To provide experimental verification of the analysis and design procedure.

• To characterize the state-of-the-art, in terms of performance limitations of a dynamic buck converter using commercially-available parts.
2 DC Analysis and Design

2.1 CCM Operation Requirement

Directly-proportional control of the output is beneficial to dynamic power applications, since both envelope tracking and amplitude modulation require the dynamic supply to follow or reproduce an existing waveform [34, 37, 49, 52]. As explained in the literature, an asynchronous buck converter can be controlled in this manner when operated in continuous conduction mode (CCM) [66]. The schematic for an asynchronous diode-rectified PWM buck converter is shown in Fig. 4.

![Figure 4: Standard diode-rectified buck converter.](image)

The converter is said to be operating in CCM when inductor current $i_L$ is greater than zero for the entire switching period $T$. Since the $R-L-C$ output filter prevents dc current from flowing to ground, dc inductor current $I_L$ and output current $I_O$ are equal, i.e.,

$$I_L = I_O. \quad (2)$$

Therefore, if $i_L$ maintains a value greater than zero, the horizontal symmetry of the
If $i_L$ is zero over some finite portion of $T$ for any duration greater than instantaneous $t = (0, T, 2T, \ldots, nT)$, then the waveform is no longer symmetrical and its dc average $I_L = I_O$ is a nonlinear function of $D$. This is referred to as discontinuous conduction mode (DCM). While DCM operation can be useful in certain supply applications, its highly nonlinear control characteristics are undesirable from the perspective of a dynamic supply where the main purpose is to track an existing voltage signal or accurately reproduce an envelope. It therefore follows that a dynamic buck converter must operate in CCM at all times if directly-proportional output is to be preserved without the assistance of complex control circuitry or external signal processing. Fig. 5 depicts the basic difference between the two conduction modes.

Figure 5: CCM versus DCM converter operation.
2.2 Effect of Total Converter Efficiency

The traditional dc analysis of fixed-output buck converters typically assumes the converter is lossless (i.e., $\eta = 1$) when characterizing conduction mode boundaries, dc transfer functions, etc. Total device losses $P_{LS} > 0$ and total converter efficiency $\eta < 1$ are factored into portions of the analysis and design after the fact. This approach works well for fixed-output supply applications because

- Variability in dc input voltage $V_I$ and load $R_L$ is assumed to fall within a limited range.
- Range of duty cycle is typically narrow, i.e., $(D_{\text{max}} - D_{\text{min}}) \ll 1$.
- Duty cycle is usually centered around 50%, i.e., $0 \ll D_{\text{min}} < 0.5$ and $0.5 < D_{\text{max}} \ll 1$.

As demonstrated in the existing literature [66, 71], a narrow operating range for $D$ allows the design of fixed-output buck converters that operate with constant high efficiency, usually greater than 90%. Invoking the principles of a lossless converter into the dc analysis is therefore practical, and greatly simplifies the resulting design procedure.

However, by definition, dynamic power supplies often require a wide range of output; ideally, $0 \leq V_O \leq V_I$, which implies a similarly wide duty cycle range approaching $0 \leq D \leq 1$. The ratio of total device losses $P_{LS}$ to output power $P_O$ for an asynchronous buck converter is described in the existing literature as

$$\frac{P_{LS}}{P_O} = \frac{D_{\text{DS}}}{R_L} + \frac{f_s C_O V_I^2 R_L}{V_O^2} + (1 - D) \left( \frac{V_F}{V_O} + \frac{R_F}{R_L} \right) + \frac{r_L}{R_L} + \frac{r_C R_L (1 - D)^2}{12 f_s^2 L^2} \quad (3)$$

and reveals the dominance of coefficients $\frac{1}{V_O}$, $\frac{1}{V_O^2}$, $(1 - D)$, and $(1 - D)^2$. These quantities are, in turn, dependent upon the aforementioned variable output. If (3) is applied to the operating conditions of a dynamic-output buck converter, assuming
nominally fixed $V_I$ and $R_L$, then $D$ and $V_O$ are the only significant variables in the loss-to-output power ratio. Since

$$\eta = \frac{1}{1 + \frac{P_{LS}}{P_O}} \quad (4)$$

then total efficiency $\eta$ will also vary with $V_O$ and $D$, decreasing substantially as the output approaches zero. For this reason, $\eta$ must be taken into account as a continuous function of $(D, V_O)$ in the new dc analysis and design of the variable-output buck converter.

### 2.3 Inductor Current and CCM-DCM Boundary of Variable-Output Buck Converter

The following assumptions are made for the new dc analysis of an asynchronous buck converter operated as a dynamic power supply:

1. Principal of circuit operation is the same as a fixed-output CCM buck converter, i.e., $I_I = D I_O$ and $V_O = \eta D V_I$.

2. MOSFET $S_1$, diode $D_1$, inductor $L$, and capacitor $C$ are real components and dissipate power, i.e., $\eta < 1$.

3. Total converter efficiency $\eta$ varies with $(D, V_O)$, i.e., $\eta_{\text{min}} \leq \eta \leq \eta_{\text{max}} < 1$.

4. $V_I$ is fixed.

5. $R_L$ is fixed.

Since the voltage $v_L$ across the inductor is

$$v_L(t) = \begin{cases} V_I - V_O, & \text{for } 0 < t \leq DT \\ -V_D - V_O, & \text{for } DT < t \leq T \end{cases} \quad (5)$$
the current \( i_L \) through the inductor is

\[
i_L(t) = \int_{\tau=0}^{t} \frac{V_L}{L} d\tau + i_L(0)
\]

\[
= \begin{cases} 
\frac{V_I - V_O}{L} t + i_L(0), & \text{for } 0 < t \leq DT \\
-\frac{V_D - V_O}{L} (t - DT) + \frac{V_I - V_O}{L} DT + i_L(0), & \text{for } DT < t \leq T 
\end{cases}
\]

(6)

where \( V_D \) is the total forward-biased voltage across the rectifier diode \( D_1 \). An asynchronous diode-rectified buck converter operates in either CCM, DCM, or at the boundary between CCM and DCM, depending on the shape of \( i_L \) as depicted in Fig. 6.

![Diagram of CCM-DCM boundary of inductor current](image)

Figure 6: CCM-DCM boundary of inductor current.

The converter must operate in CCM or at the CCM-DCM boundary for assumption 1) to be valid. CCM operation depends upon maintaining a minimum value of \( I_L \) and a maximum value of peak-to-peak inductor current \( \Delta i_L \) at this \( I_L \). If \( I_L \) falls below a certain boundary dc level \( I_{OB} \), and \( \Delta i_L \) is simultaneously too large, the converter will enter DCM. Therefore, in the worst-case scenario, the converter operates at CCM-DCM boundary when its output is minimum; that is, \( I_{OB} \) is equal to the
The converter’s minimum specified dc output current $I_{O\text{min}}$. The dc inductor current for CCM or CCM-DCM boundary operation is

$$I_L = i_L(0) + \frac{\Delta i_L}{2}$$

where

$$\Delta i_L = i_L(DT) - i_L(0) = \frac{(V_I - V_O) DT}{L}. \quad (8)$$

Therefore,

$$I_L = i_L(0) + \frac{(V_I - V_O) DT}{2L}. \quad (9)$$

Assumption 2) implies the converter is lossy. The existing literature defines the lossy dc voltage transfer function as

$$M_{VDC} = \frac{V_O}{V_I} = \eta D \quad (10)$$

where $\eta$ is the total converter efficiency, or

$$\eta = \frac{P_O}{P_I} = \frac{I_OV_O}{I_IV_I}. \quad (11)$$

From (10),

$$D = \frac{V_O}{\eta V_I}. \quad (12)$$

A more specific way of expressing $\Delta i_L$ is therefore

$$\Delta i_L = \frac{V_IV_O - V_O^2}{f_LV_I\eta}. \quad (13)$$

Figure 7 compares the behavior of $\Delta i_L$ with respect to duty cycle (and therefore, $V_O$) in both a fixed-output buck converter and dynamic buck converter operating in CCM.
If assumptions 3) and 4) are valid and $\eta$ varies with output while $V_I$ remains fixed, then (10) and assumption 1) both imply that the minimum converter output $(I_{O_{min}}, V_{O_{min}})$ corresponds to some minimum duty cycle $D_{min}$ and minimum efficiency $\eta_{min}$, i.e.,

$$\frac{V_{O_{min}}}{V_I} = \eta_{min} D_{min}. \tag{14}$$
For CCM-DCM boundary operation, \( i_L(0, T, 2T, \ldots, nT) = 0 \). Therefore, in the worst-case operating scenario, the CCM-DCM boundary of a variable-output converter can be characterized by rewriting (9) as

\[
I_{OB} = I_{Omin} = I_{L(min)} = 0 + \frac{(V_I - V_{Omin}) D_{min} T}{2L}.
\]  

(15)

Substituting for \( D_{min} \) via (14) and expressing \( T \) in terms of \( f_s \) gives

\[
I_{OB} = \frac{(V_I - V_{Omin}) (V_{Omin} \eta_{min})}{2f_s L}.
\]  

(16)

If assumption 5) is taken into account and the load \( R_L \) is fixed, \( I_L \) and \( I_O \) can be defined as

\[
I_L = I_O = \frac{V_O}{R_L}
\]  

(17)

for any output level or conduction mode; hence the minimum dc output current is

\[
I_{Omin} = \frac{V_{Omin}}{R_L}.
\]  

(18)

Combining (18) and (16) allows the worst-case CCM-DCM boundary operating condition to be expressed as

\[
\frac{V_{Omin}}{R_L} = \frac{(V_I - V_{Omin}) (V_{Omin} \eta_{min})}{2f_s L}
\]  

(19)

or as a normalized ratio

\[
1 = \frac{R_L (V_I - V_{Omin}) \left( \frac{1}{V_{Omin} \eta_{min}} \right)}{2f_s L}.
\]  

(20)

The dynamic converter will therefore operate at CCM-DCM boundary when output
is minimum, and CCM at greater output, if

\[ 1 = \frac{R_L \left(1 - \frac{V_{O\text{min}}}{V_I}\right)}{2f_s L \eta_{\text{min}}}. \]  

(21)

Alternately, the inductor value that ensures operation at the CCM-DCM boundary is

\[ L \bigg|_{\text{CCM-DCM}} = \frac{R_L (V_I - V_{\text{Omin}})}{2f_s V_I \eta_{\text{min}}}. \]  

(22)

All other conduction modes can be described in a similar fashion. For “full” CCM, operation is above the boundary at all times and minimum dc output current \( I_{O\text{CCM}} \) is greater than \( I_O \), i.e.,

\[ I_{O\text{CCM}} > I_O. \]  

(23)

In this mode, by definition,

\[ I_{O\text{CCM}} = I_{O\text{min}} = \frac{V_{O\text{min}}}{R_L}. \]  

(24)

Therefore, (23) expands to

\[ \frac{V_{O\text{min}}}{R_L} > \frac{(V_I - V_{O\text{min}})(V_{O\text{min}}/V_I \eta_{\text{min}})}{2f_s L} \]  

(25)

and the dynamic converter always operates in CCM if

\[ 1 > \frac{R_L \left(1 - \frac{V_{O\text{min}}}{V_I}\right)}{2f_s L \eta_{\text{min}}}. \]  

(26)

For DCM operation, minimum dc output current \( I_{O\text{DCM}} \) is less than \( I_O \), i.e.,

\[ I_{O\text{DCM}} < I_O \]  

(27)
due to the instantaneous inductor current being zero over a greater portion of the switching cycle. In this mode, by definition,

\[ I_{ODCM} = I_{Omin} = \frac{V_{Omin}}{R_L}. \]  

Expanding (27) therefore yields

\[ \frac{V_{Omin}}{R_L} < \frac{(V_I - V_{Omin}) \left( \frac{V_{Omin}}{V_I \eta_{min}} \right)}{2f_s L} \]  

which implies the dynamic converter enters DCM at low output if

\[ 1 < \frac{R_L \left( 1 - \frac{V_{Omin}}{V_I} \right)}{2f_s L \eta_{min}}. \]  

2.4 Output Ripple Voltage

All buck converters exhibit output ripple voltage \( v_o(t) \) due to the filter’s suppression of triangular peak-to-peak inductor current \( \Delta i_L \). The degree to which this ripple propagates at the output depends upon the size of capacitor \( C \) and its equivalent series resistance (ESR) \( r_C \). Figure 8 shows a model of the converter’s output stage with dc and ac currents and voltages present.
If the output ripple current $i_o$ is assumed to be very small, then the ac current through $C$ and $r_C$ is

$$i_C \cong i_L - I_O = i_L - I_L. \quad (31)$$

Hence, from (6), (7), and (8),

$$i_C(t) = \begin{cases} \frac{\Delta i_L}{DT} t - \frac{\Delta i_L}{2}, & \text{for } 0 < t \leq DT \\ V_D + V_O (DT - t) + \frac{\Delta i_L}{2}, & \text{for } DT < t \leq T. \end{cases} \quad (32)$$

From the circuit in Fig. 8,

$$v_o = v_c + v_{rc} \quad (33)$$

where $v_c$ is the ac voltage across the capacitor and $v_{rc}$ is the ac voltage across $r_C$. Therefore,

$$v_c = \int_{\tau=0}^{t} \frac{i_C}{C} d\tau + v_c(0), \quad (34)$$

$$v_{rc} = i_C r_C, \quad (35)$$
\[ v_o(t) = i_C r_C + \int_{\tau=0}^{t} \frac{i_C}{C} d\tau + v_c(0). \] (36)

When characterizing output ripple over a full switching period, it is often more practical to quantify the ripple in terms of its peak-to-peak magnitude \( V_r \) rather than instantaneous value \( v_o(t) \). Total peak-to-peak output ripple can therefore be expressed in terms of individual peak-to-peak ripple voltages \( V_{C(pp)} \) and \( V_{rc(pp)} \) across \( C \) and \( r_C \) respectively, i.e.,

\[ V_r = V_{C(pp)} + V_{rc(pp)}. \] (37)

From (32) the peak-to-peak capacitor current \( i_{C(pp)} \) is

\[ i_{C(pp)} = \Delta i_L. \] (38)

Therefore, since \( r_C \) is nominally fixed, (35) can be rewritten in terms of peak-to-peak values as

\[ V_{rc(pp)} = i_{C(pp)} r_C = \Delta i_L r_C. \] (39)

The peak-to-peak capacitor ripple voltage is similarly derived in [66] as

\[ V_{C(pp)} = \frac{\Delta i_L T}{8C} = \frac{\Delta i_L}{8f_s C}. \] (40)

Therefore,

\[ V_r = \Delta i_L \left( r_C + \frac{1}{8f_s C} \right). \] (41)

and substitution of (13) into (41) gives

\[ V_r = \frac{V_I V_O - V_O^2}{f_s L V_I \eta} \left( r_C + \frac{1}{8f_s C} \right). \] (42)

It may be necessary to quantify output ripple without knowing the value of inductor
L. An approximation can therefore be made if it is assumed the dynamic converter will operate at the CCM-DCM boundary, i.e., utilizing the smallest inductor possible. Hence, substituting \( L \simeq L \bigg|_{CCM-DCM} \) from (16) gives

\[
V_r \simeq \frac{V_I V_O - V_O^2}{f_s V_I \eta} \left( r_C + \frac{1}{8f_s C} \right) \left[ \frac{2f_s V_I \eta_{min}}{R_L (V_I - V_{O_{min}})} \right]
\]

\[
\simeq \frac{2 (V_I V_O - V_O^2)}{R_L (V_I - V_{O_{min}})} \left( r_C + \frac{1}{8f_s C} \right) \left( \frac{\eta_{min}}{\eta} \right).
\]

(43)

The maximum output ripple \( V_{r_{(max)}} \) can be determined by differentiating \( V_r \) with respect to \( V_O \), setting equal to zero, solving for \( V_O \), and substituting into \( V_r \). The presence of \( \eta \) as a nonlinear function of both \( V_O \) and \( D \) complicates this method considerably; even if (4) is simplified considerably through practical approximation, differentiation results in a quartic polynomial. However, from a practical standpoint, the need to determine \( V_r \) stems from the necessity of simply keeping the output ripple below some specified level. Therefore, an estimate of \( V_r \) that takes into account the “worst-case” scenario - or maximum possible ripple - is useful. Since it is apparent that

\[
0 < \frac{\eta_{min}}{\eta} \leq 1
\]

(44)

it follows that

\[
V_r \leq \frac{2 (V_I V_O - V_O^2)}{R_L (V_I - V_{O_{min}})} \left( r_C + \frac{1}{8f_s C} \right)
\]

(45)

for any value of \( V_O, \eta_{min}, \) or \( \eta \). The worst-case ripple \( V_r' \) is therefore defined as

\[
V_r' = \frac{2 (V_I V_O - V_O^2)}{R_L (V_I - V_{O_{min}})} \left( r_C + \frac{1}{8f_s C} \right)
\]

(46)

and the maximum worst-case ripple is

\[
V_{r'_{(max)}} = \left\{ \frac{2 (V_I V_O - V_O^2)}{R_L (V_I - V_{O_{min}})} \left( r_C + \frac{1}{8f_s C} \right) \right\}_{max}.
\]

(47)
A generalized solution can be obtained from

\[
\frac{dV_r'}{dV_O} = \frac{2(V_I - 2V_O)}{R_L(V_I - V_{O_{\text{min}}})} \left( r_C + \frac{1}{8f_sC} \right) = 0
\]  

(48)

and

\[
V_O\bigg|_{V_{r_{\text{max}}}} = V_{Or} = \frac{V_I}{2}
\]  

(49)

which is the output voltage at which maximum worst-case ripple occurs. Therefore,

\[
V_{r_{\text{max}}} = V_r\bigg|_{V_{Or}} = \frac{V_I^2}{2R_L(V_I - V_{O_{\text{min}}})} \left( r_C + \frac{1}{8f_sC} \right)
\]  

(50)

and

\[
V_{r_{\text{max}}} \leq V_{r'_{\text{max}}}.
\]  

(51)

The same approach may be used to obtain a more precise assessment of output ripple if \( L \) is known and \( \eta \) can be calculated for a given output \( V_O \). Substituting (49) into (42) therefore yields

\[
V_{r_{\text{max}}} = V_r\bigg|_{V_{Or}} = \frac{V_I}{4f_sL\eta_r} \left( r_C + \frac{1}{8f_sC} \right)
\]  

(52)

where \( \eta_r \) is the total converter efficiency when \( V_O = \frac{V_I}{2} \).

## 2.5 Device Stresses

### 2.5.1 Switch

The maximum instantaneous voltage \( V_{SM_{\text{max}}} \) across the switching transistor is equal to the drain-to-source voltage when the switch is off and the diode is conducting, i.e.,

\[
V_{SM_{\text{max}}} = V_{DS(\text{off})} = V_I + V_D.
\]  

(53)
From the piecewise linear model of a p-n junction diode in Fig. 9, the effective forward voltage of the diode is

\[ V_D = V_F + I_D R_F \]  \hspace{1cm} (54)

where \( V_F \) is the nominal forward voltage, \( I_D \) is the dc component of the forward current, and \( R_F \) is the nominal forward resistance of the diode.

![Figure 9: Piecewise linear model of p-n junction diode in forward-biased mode.](image)

When the diode is forward-biased and conducting,

\[ I_D \approx I_L = I_O = \frac{V_O}{R_L} \]  \hspace{1cm} (55)

and (53) is therefore

\[ V_{SM_{max}} = V_I + V_F + \frac{V_{O_{max}} R_F}{R_L}. \]  \hspace{1cm} (56)

The maximum instantaneous current \( I_{SM_{max}} \) through the switch is equal to the maximum instantaneous input current of the dynamic converter for all output levels. As established in the literature, the input current is

\[ i_S(t) \equiv \begin{cases}  
i_L, & \text{for } 0 < t \leq DT \\ 0, & \text{for } DT < t \leq T. \end{cases} \]  \hspace{1cm} (57)
if leakage current in the switch and diode are neglected. The maximum value of $i_S(t)$ at any given output level is $I_{SM}$, which always occurs at $t = DT$ and is equivalent to the peak instantaneous inductor current per switching cycle. Hence,

$$I_{SM} = i_S(DT) = i_L(DT) = I_L + \frac{\Delta i_L}{2}. \quad (58)$$

From (17), (13), and (49) it is apparent that $I_L$ and $\Delta i_L$ are inversely proportional when $\frac{V_I}{2} < V_O \leq V_{O_{max}}$. It therefore cannot be assumed that the maximum value of $I_{SM}$ will always occur at maximum output, i.e., $(D_{max}, I_{O_{max}}, V_{O_{max}}, \eta_{max})$, although this is the case for most designs. Such a scenario is illustrated by Fig. 10.

![Figure 10: Possible waveforms of switch current $i_S$ where $I_{SM_{max}}$ does not occur at maximum output.](image)

Substituting (17) and (13) into (58) gives

$$I_{SM} = \frac{V_O}{R_L} + \frac{V_I V_O - V_O^2}{2 f_s L V_I \eta}. \quad (59)$$
As with ripple voltage, $I_{SM}$ may need to be determined without specific knowledge of the value of inductor $L$. The same approximation method is therefore used, i.e., substituting $L \approx L|_{CCM-DCM}$ to obtain

$$I_{SM} \approx \frac{V_O}{R_L} + \frac{V_I V_O - V_O^2}{2f_s V_I \eta} \left[ \frac{2f_s V_I \eta_{\min}}{R_L (V_I - V_{O\min})} \right]$$

$$= \frac{V_O}{R_L} + \frac{V_I V_O - V_O^2}{R_L (V_I - V_{O\min})} \left( \frac{\eta_{\min}}{\eta} \right). \quad (60)$$

Likewise, to determine $I_{SMmax}$, the same principles are applied as in (44)-(51), and

$$I_{SM} \leq \frac{V_O}{R_L} + \frac{V_I V_O - V_O^2}{R_L (V_I - V_{O\min})} \quad (61)$$

for any value of $V_O$, $\eta_{\min}$, or $\eta$. The worst-case switch current $I'_{SM}$ is therefore defined as

$$I'_{SM} = \frac{V_O}{R_L} + \frac{V_I V_O - V_O^2}{R_L (V_I - V_{O\min})} \quad (62)$$

and the maximum worst-case switch current is

$$I'_{SMmax} = \left\{ \frac{V_O}{R_L} + \frac{V_I V_O - V_O^2}{R_L (V_I - V_{O\min})} \right\}_{max}. \quad (63)$$

The generalized solution is obtained from

$$\frac{dI'_{SM}}{dV_O} = \frac{1}{R_L} + \frac{V_I - 2V_O}{R_L (V_I - V_{O\min})} = 0 \quad (64)$$

and

$$V_O \bigg|_{I'_{SMmax}} = V_{OSM} = V_I - \frac{V_{O\min}}{2}. \quad (65)$$

It should however be noted that, often,

$$V_{Omax} \leq V_I - \frac{V_{O\min}}{2} \quad (66)$$
and in such a case

\[ V_O \bigg|_{I'_{SM\max}} = V_{O\max}. \]  

(67)

Therefore, two distinct scenarios are derived

\[
I'_{SM\max} = \begin{cases} 
I'_{SM \bigg| V_{OSM}} = \frac{(V_I - \frac{V_{O\min}}{2})^2}{R_L(V_I - V_{O\min})}, & \text{for } V_{O\max} > V_I - \frac{V_{O\min}}{2} \\
I'_{SM \bigg| V_{O\max}} = \frac{V_{O\max}(2V_I - V_{O\min} - V_{O\max})}{R_L(V_I - V_{O\min})}, & \text{for } V_{O\max} \leq V_I - \frac{V_{O\min}}{2} 
\end{cases} 
\]  

(68)

which describe the maximum switch current in terms of the worst-case stress, i.e.,

\[ I_{SM\max} \leq I'_{SM\max}. \]  

(69)

2.5.2 Diode

The maximum instantaneous voltage \( V_{DM\max} \) across the diode rectifier occurs when the switch is on and the diode is off. If the switch’s on-resistance \( r_{DS} \) is small and the dc voltage drop \( V_{rDS} \) across \( r_{DS} \) is similarly small, i.e.,

\[ V_{rDS} \ll V_I \]  

(70)

then

\[ V_{DM\max} \approx V_I. \]  

(71)

The maximum instantaneous current \( I_{DM\max} \) through the diode is equal to the maximum instantaneous inductor current of the dynamic converter for all output levels. Therefore,

\[ I_{DM\max} = \left\{ I_L + \frac{\Delta i_L}{2} \right\}_{max} = I_{SM\max}. \]  

(72)
2.5.3 Inductor

The maximum instantaneous current through the inductor is

\[ I_{LM_{\text{max}}} = \left\{ I_L + \frac{\Delta i_L}{2} \right\}_{\text{max}} = I_{SM_{\text{max}}}. \]  \hspace{1cm} (73)

2.5.4 Capacitor

The maximum instantaneous voltage \( V_{CM_{\text{max}}} \) across the capacitor must take into account the upper half of the peak-to-peak output ripple voltage \( V_r \). Therefore, from (42),

\[ V_{CM_{\text{max}}} = \left\{ V_O + \frac{V_r}{2} \right\}_{\text{max}} = \left\{ V_O + \frac{V_i V_O - V_O^2}{2 f_s L V_I \eta} \left( r_C + \frac{1}{8 f_s C} \right) \right\}_{\text{max}}. \]  \hspace{1cm} (74)

As with current stresses \( I_{SM_{\text{max}}}, I_{DM_{\text{max}}}, \) and \( I_{LM_{\text{max}}} \), capacitor voltage stress \( V_{CM_{\text{max}}} \) is a function of \( V_O \) and \( \eta \) over the full range of output. Likewise, \( V_O \) and \( V_r \) are analogous to \( I_L \) and \( \Delta i_L \), which implies \( V_{CM_{\text{max}}} \) may not necessarily occur at maximum output \( (D_{\text{max}}, V_{O_{\text{max}}}) \). However, unlike the relationship between \( I_L \) and \( \Delta i_L \), it generally holds true that \( V_O \gg V_r \) since most practical switching converters are designed to suppress output ripple as much as possible. As demonstrated by the behavior of inductor current, shown in Fig. 7, \( \Delta i_L \), and hence \( V_r \), is at a relative minimum when output is maximum. Therefore, if ripple voltage is very small compared to maximum dc output, then \( V_{CM_{\text{max}}} \) occurs at this maximum output, i.e.,

\[ V_{CM_{\text{max}}} = V_{O_{\text{max}}} + \frac{V_i V_{O_{\text{max}}} - V_{O_{\text{max}}}^2}{2 f_s L V_I \eta_{\text{max}}} \left( r_C + \frac{1}{8 f_s C} \right) \]  \hspace{1cm} (75)

and

\[ V_{CM_{\text{max}}} \approx V_{O_{\text{max}}}. \]  \hspace{1cm} (76)
2.6 Variable Switching Loss

The switching power loss of any asynchronous buck converter, as established in the literature, is

\[ P_{SW} = f_s C_O V_I^2. \]  \hspace{1cm} (77)

If the switch’s output capacitance \( C_O \) is assumed to be constant, then \( P_{SW} \) is also constant. Under this model, switching losses will typically dominate at low output power, while having much less effect at high output. However, in practice, \( C_O \) is nonlinear and inversely proportional to the drain-to-source voltage \( V_{DS} \) of the switch, as shown in Fig. 11.

![Figure 11: Nominal output capacitance \( C_{oss} \), nominal reverse transfer capacitance \( C_{rss} \), and output capacitance \( C_O = C_{oss} - C_{rss} \) of Si power MOSFET (plot courtesy of Microsemi Corporation).](image)

For a dynamic buck converter, the average value of \( V_{DS} \) varies with \( D \) over a wide range as shown in Fig. 12; it follows that \( C_O \) also varies with \( D \). Depending upon individual MOSFET characteristics, \( C_O \) may exhibit significant nonlinearity across the range of dynamic output. This implies \( P_{SW} \) is also a nonlinear function of output, rendering constant or linear approximations in the literature unsuitable if the buck
converter is used as a dynamic power supply. Since $P_{SW}$ significantly affects efficiency under certain conditions, dynamic MOSFET output capacitance should be taken into account when analyzing total losses and efficiency as a function of $V_O$.

![Diagram showing $V_{DS}$ as a function of $D$.](image)

**Figure 12:** Change in $V_{DS}$ as a function of $D$.

The literature [66] provides an expression for $C_O$ as a function of time-variable drain-to-source voltage $v_{DS}$,

$$C_O = C_{ds(V_{ds}')} \sqrt{\frac{V_{DS}'' + V_B}{V_I + V_B}} \cdot \sqrt{\frac{V_I + V_B}{v_{DS} + V_B}}$$  \hfill (78)
where $V_B$ is the potential barrier of the body diode and $C_{ds(V_{ds'})}$ is the rated output capacitance of the MOSFET at fixed drain-to-source voltage $V'_{DS}$ when $V_{GS} = 0$ and $f = 1$MHz. Rated output capacitance $C_{ds(V_{ds'})}$ is typically derived from the manufacturer’s device data as

$$C_{ds(V_{ds'})} = (C_{oss} - C_{rss}) \bigg|_{V_{DS}=V'_{DS}, V_{GS}=0}$$

(79)

where $C_{oss}$ is the nominal output capacitance and $C_{rss}$ is the nominal reverse transfer capacitance. For a CCM buck converter, $v_{DS}$ is

$$v_{DS}(t) = \begin{cases} 0, & \text{for } 0 < t \leq DT \\ V_I + V_F, & \text{for } DT < t \leq T. \end{cases}$$

(80)

Since $v_{DS}$ is essentially a binary signal with fixed frequency and variable pulse width, it can also be expressed as the average drain-to-source voltage over one switching cycle, i.e.,

$$v_{DS}(t) \equiv V_{DS} \bigg|_{nT < t \leq (n+1)T} = (V_I + V_F) \left(1 - D\right)$$

$$= (V_I + V_F) \left(1 - \frac{V_O}{\eta V_I}\right) = V_I - \frac{V_O}{\eta} + V_F - \frac{V_O V_F}{\eta V_I}.$$  

(81)

Therefore,

$$C_O = (C_{oss} - C_{rss}) \bigg|_{V'_{DS}} \sqrt{\frac{V_I V_{DS} + V_B (V_I + V_{DS}) + V^2_B}{V_I \left(\frac{V_O}{\eta} + V_F - \frac{V_O V_F}{\eta V_I}\right) + V_B \left(2 V_I - \frac{V_O}{\eta} + V_F - \frac{V_O V_F}{\eta V_I}\right) + V^2_B}}$$

(82)

and the switching loss for a dynamic buck converter is

$$P_{SW} = f_s V_I^2 (C_{oss} - C_{rss}) \bigg|_{V'_{DS}} \sqrt{\frac{V_I V_{DS} + V_B (V_I + V_{DS}) + V^2_B}{V_I \left(\frac{V_O}{\eta} + V_F - \frac{V_O V_F}{\eta V_I}\right) + V_B \left(2 V_I - \frac{V_O}{\eta} + V_F - \frac{V_O V_F}{\eta V_I}\right) + V^2_B}}$$

(83)

Silicon power MOSFETs are available with $V_B \leq 0.9$ V. Hence, in the case of low-
to medium-power converters where $V_I \geq 9\,V$, the quantities associated with $V_B$ and $V_B^2$ are very small compared to $V_I V'_DS$ and $V_I \left( V_I - \frac{V_O}{\eta} + V_F - \frac{V_O V_F}{\eta V_I} \right)$. Additionally, if $V_I \gg V_F$, the collective effects of $V_F$ and $V_B$ on dynamic output capacitance are negligible and (82) can be simplified to

$$C'_O = C_O \bigg|_{V_I \gg V_B, V_F} \approx (C_{oss} - C_{rss}) \bigg|_{V'_D} \sqrt{\frac{V'_DS}{V_I - \frac{V_O}{\eta}}}.$$  \hfill (84)

The approximate nonlinear switching loss $P'_{SW}$ of a dynamic buck converter, where $V_B \ll V_I$ and $V_F \ll V_I$, is therefore

$$P'_{SW} = P_{SW} \bigg|_{V_I \gg V_B, V_F} \approx f_s V_I^2 \left( C_{oss} - C_{rss} \right) \sqrt{\frac{V'_DS}{V_I - \frac{V_O}{\eta}}}.$$  \hfill (85)

Figure 13 shows the effect of $C_O$ on the normalized switching loss in low- to medium-power dynamic converters with a Si MOSFET switch and low-$V_F$ diode. Figure 14 compares the approximate nonlinear switching loss in (85) to the exact loss in (83), if $V_B = V_F = 0.9\,V$. This approximation can be seen to diverge as $V_I$ decreases and $V_O$ increases, but is nonetheless a good estimate.
Figure 13: Normalized effect of nonlinear $C_O$ on switching loss in low- to medium-power dynamic buck converters with Si MOSFET switch ($V'_{DS} = 25\,\text{V}$, $V_B \leq 0.9\,\text{V}$) and $V_F \leq 0.9\,\text{V}$. 
Figure 14: Normalized comparison of exact value and approximation of dynamic switching loss $P_{SW}$ for $V_B = V_F = 0.9$V.

2.7 Total Converter Efficiency

Total converter power loss $P_{LS}$ depends on the power dissipated by each device in the circuit. This can be expressed as the sum of MOSFET switching losses $P_{SW}$, diode loss $P_{VF}$ associated with the forward voltage, capacitor power loss $P_{rC}$, MOSFET conduction loss $P_{rDS}$, diode loss $P_{rRF}$ associated with the forward resistance, and inductor power loss $P_{rL}$. The circuit of a buck converter with device parasitics contributing to the total power loss is shown in Fig. 15.
Figure 15: Asynchronous buck converter with device parastics and equivalent device models.

As established by (4), efficiency is determined from the loss-to-output power ratio \( \frac{P_{LS}}{P_O} \) which is provided in the existing literature as

\[
\frac{P_{LS}}{P_O} = \frac{P_{SW} + P_{VF} + P_{rC} + P_{rDS} + P_{RF} + P_{rL}}{P_O}.
\]  

(86)

This can be expanded to

\[
\frac{P_{LS}}{P_O} = \frac{f_s C_O V_I^2}{P_O} + \frac{(1 - D) V_F I_O}{P_O} + \frac{r_C I_{Crms}^2}{P_O} + \frac{r_{DS} I_{Srms}^2}{P_O} + \frac{R_F I_{Drms}^2}{P_O} + \frac{r_L I_{Lrms}^2}{P_O}
\]  

(87)

where \( C_O \) and \( r_{DS} \) are the MOSFET output capacitance and on-resistance, respectively; \( V_F \) and \( R_F \) are the respective forward voltage and forward resistance of the diode; \( r_L \) and \( r_C \) are the respective parasitic resistances of the inductor and capacitor; \( I_{Crms}, I_{Srms}, I_{Drms}, \) and \( I_{Lrms} \) are the respective RMS currents through the capacitor, switch, diode, and inductor. Expanding the RMS terms, defined per the existing
analysis, yields

\[
\frac{P_{LS}}{P_O} = \frac{f_s C_O V_I^2 R_L}{V_O^2} + \frac{V_F}{V_O} \left(1 - \frac{V_O}{V_I} \right) + \frac{r_C R_L (1 - D)^2}{12 f_s^2 L^2}
\]
\[
+ \left[ \frac{r_{DS} D}{R_L} + \frac{R_F (1 - D)}{R_L} + \frac{r_L}{R_L} \right] \left[ 1 + \frac{1}{12} \left( \frac{\Delta i_L}{I_O} \right)^2 \right]
\] (88)

where, from (8),

\[
\frac{\Delta i_L}{I_O} = \left( \frac{V_I - V_O}{f_s L} \right) = \frac{R_L \left(1 - \frac{V_O}{V_I} \right)}{f_s L \eta}.
\] (89)

The loss-to-output ratio for a dynamic buck converter is therefore

\[
\frac{P_{LS}}{P_O} = \frac{f_s C_O V_I^2 R_L}{V_O^2} + \frac{V_F}{V_O} \left(1 - \frac{V_O}{\eta V_I} \right) + \frac{r_C R_L (1 - D)^2}{12 f_s^2 L^2} \left(1 - \frac{V_O}{\eta V_I} \right)^2
\]
\[
+ \left[ \frac{r_{DS} D}{R_L \eta V_I} + \frac{R_F}{R_L} \left(1 - \frac{V_O}{\eta V_I} \right) + \frac{r_L}{R_L} \right] \left[ 1 + \frac{R_L^2 \left(1 - \frac{V_O}{\eta V_I} \right)^2}{12 f_s^2 L^2 \eta^2} \right]
\] (90)

and total converter efficiency may be defined as

\[
\eta = \left\{ 1 + \frac{f_s C_O V_I^2 R_L}{V_O^2} + \frac{V_F}{V_O} \left(1 - \frac{V_O}{\eta V_I} \right) + \frac{r_C R_L (1 - D)^2}{12 f_s^2 L^2} \left(1 - \frac{V_O}{\eta V_I} \right)^2
\]
\[
+ \left[ \frac{r_{DS} V_O}{R_L \eta V_I} + \frac{R_F}{R_L} \left(1 - \frac{V_O}{\eta V_I} \right) + \frac{r_L}{R_L} \right] \left[ 1 + \frac{R_L^2 \left(1 - \frac{V_O}{\eta V_I} \right)^2}{12 f_s^2 L^2 \eta^2} \right] \right\}^{-1}.
\] (91)

If the nonlinear behavior of \(C_O\) is considered, total converter efficiency is

\[
\eta = \left\{ 1 + \frac{f_s V_I^2 R_L (C_{oss} - C_{rss})}{V_O^2} \sqrt{\frac{V_{DS}}{V_I - \frac{V_O}{\eta}}} + \frac{V_F}{V_O} \left(1 - \frac{V_O}{\eta V_I} \right) + \frac{r_C R_L (1 - D)^2}{12 f_s^2 L^2} \left(1 - \frac{V_O}{\eta V_I} \right)^2
\]
\[
+ \left[ \frac{r_{DS} V_O}{R_L \eta V_I} + \frac{R_F}{R_L} \left(1 - \frac{V_O}{\eta V_I} \right) + \frac{r_L}{R_L} \right] \left[ 1 + \frac{R_L^2 \left(1 - \frac{V_O}{\eta V_I} \right)^2}{12 f_s^2 L^2 \eta^2} \right] \right\}^{-1}.
\] (92)
Note that $\eta$ itself must be considered wherever $D$ is present; this effectively reintroduces $\eta^{\pm 1}, \eta, \eta^2,$ and $\eta^3$ into the expression for total efficiency. A closed-form solution is therefore difficult to obtain strictly in terms of $V_O.$ However, a suitable approximation can be derived via software-assisted iteration and/or simplification of (91) based on practical design considerations.

If software such as MATLAB is utilized, a single iteration of $\eta$ is usually sufficient for convergence, i.e,

$$\eta = \left\{ 1 + \frac{f_s V_I^2 R_L (C_{oss} - C_{rss})}{V_O^2} \sqrt{\frac{V'_{DS}}{V_I - \frac{V_O}{\eta}}} + \frac{V_F}{V_O} \left( 1 - \frac{V_O}{\eta V_I} \right) + \frac{r_C R_L}{12 f_s^2 L^2} \left( 1 - \frac{V_O}{\eta V_I} \right)^2 \right\}^{-1}$$

(93)

where

$$\eta_1 = \left\{ 1 + \frac{f_s V_I^2 R_L (C_{oss} - C_{rss})}{V_O^2} \sqrt{\frac{V'_{DS}}{V_I - \frac{V_O}{\eta_0}}} + \frac{V_F}{V_O} \left( 1 - \frac{V_O}{\eta_0 V_I} \right) + \frac{r_C R_L}{12 f_s^2 L^2} \left( 1 - \frac{V_O}{\eta_0 V_I} \right)^2 \right\}^{-1}$$

(94)

and

$$\eta_0 = 1.$$  

(95)

However, it is often necessary to have some knowledge of $\eta$ prior to identifying individual circuit elements such as $L, r_L,$ and $r_C.$ It may also be desirable to estimate total efficiency based upon a single function of $V_O,$ rather than performing multiple iterations of (91) or (92). In such a case, the following assumptions are made:

1. $r_L, r_C \ll R_L$

2. $L \cong L_{CCM-DCM}$
If the first assumption holds true, $P_{r,L}$ and $P_{r,C}$ are very small compared to all other losses, and may be neglected. If the second assumption is accurate, then

$$\frac{R_L^2 \left(1 - \frac{V_O}{V_I}\right)^2}{12 f_s^2 L^2 \eta^2} \approx \frac{1}{3} \left(\frac{V_I - V_O}{V_I - V_{O_{\text{min}}}}\right)^2 \left(\frac{\eta_{\text{min}}}{\eta}\right)^2$$

and providing for the worst-case scenario where $\frac{\eta_{\text{min}}}{\eta} \approx 1$,

$$\frac{R_L^2 \left(1 - \frac{V_O}{V_I}\right)^2}{12 f_s^2 L^2 \eta^2} \approx \frac{1}{3} \left(\frac{V_I - V_O}{V_I - V_{O_{\text{min}}}}\right)^2.$$ 

Similarly, the remaining instances of $\eta$ within the equation for total efficiency are set to $\eta = 1$ to model the worst-case efficiency at any $V_O$. This allows (92) to be simplified to

$$\eta \approx \eta' = \left\{ 1 + \frac{f_s V_I^2 R_L (C_{\text{oss}} - C_{\text{rss}})}{V_O^2} \sqrt{\frac{V_{D_S}'}{V_I - V_O}} + \frac{V_F}{V_O} \left(1 - \frac{V_O}{V_I}\right) \right. 
+ \left[ \frac{r_{DS} V_O}{R_L V_I} + \frac{R_F}{R_L} \left(1 - \frac{V_O}{V_I}\right) \right] \left[1 + \frac{1}{3} \left(\frac{V_I - V_O}{V_I - V_{O_{\text{min}}}}\right)^2\right]\right\}^{-1} \quad (97)$$

and the approximate total efficiency of the dynamic buck converter, expressed solely as a function of $V_O$, is

$$\eta' = \left\{ 1 + \frac{f_s V_I^2 R_L (C_{\text{oss}} - C_{\text{rss}})}{V_O^2} \sqrt{\frac{V_{D_S}'}{V_I - V_O}} + \frac{V_F}{V_O} - \frac{V_F}{V_I} 
+ \frac{R_F}{R_L} \frac{V_O (r_{DS} - R_F)}{R_L V_I} \left[1 + \frac{1}{3} \left(\frac{V_I - V_O}{V_I - V_{O_{\text{min}}}}\right)^2\right]\right\}^{-1}. \quad (98)$$

This expression converges well with the iterative method, as demonstrated by Fig. 16. Furthermore, this solution only requires basic design specifications and knowledge of switch and diode parasitics in order to calculate a good estimate of efficiency for any output.
2.8 Design of a Dynamic Buck Converter Operating in CCM

2.8.1 Equations

It is necessary to determine the following specifications in order to select the four basic components of the dynamic buck converter:

- **Switch** – maximum drain-to-source voltage $V_{DSS_{\text{max}}}$, maximum drain current $I_{D_{\text{max}}}$.  

- **Diode** – maximum forward voltage $V_{R_{\text{max}}}$, maximum average forward current $I_{F(\text{AV})_{\text{max}}}$.  

- **Inductor** – minimum inductance $L_{\text{min}}$ required to keep converter in CCM at all times, maximum inductor current $I_{\text{dc}}$.  

- **Capacitor** – minimum capacitance $C_{\text{min}}$ required to keep output ripple voltage at or below specified ripple at all times, maximum capacitor voltage $V_{\text{dc}}$.  

Figure 16: Comparison of iterative ($\eta$) and simplified ($\eta'$) calculated efficiency characteristic of dynamic buck converter.
The switch must have $V_{DSS_{\text{max}}}$ sufficient to accommodate the maximum voltage stress $V_{SM_{\text{max}}}$; therefore, from (56),

\[ V_{DSS_{\text{max}}} > V_I + V_F + \frac{V_{O_{\text{max}}} R_F}{R_L}. \]  \hspace{1cm} (99)

Similarly, if $I_{D_{\text{max}}}$ must be large enough to handle the maximum current stress $I_{SM_{\text{max}}}$, then $I_{D_{\text{max}}}$ must accommodate the worst-case switch current stress $I'_{SM_{\text{max}}}$. Therefore, from (69) and (68),

\[ I_{D_{\text{max}}} > I'_{SM_{\text{max}}} \geq I_{SM_{\text{max}}} \]  \hspace{1cm} (100)

and

\[ I_{D_{\text{max}}} > I'_{SM_{\text{max}}} = \begin{cases} \frac{(V_I - V_{O_{\text{min}}})^2}{R_L(V_I - V_{O_{\text{min}}})}, & \text{for } V_{O_{\text{max}}} > V_I - \frac{V_{O_{\text{min}}}}{2} \\ \frac{V_{O_{\text{max}}}(2V_I - V_{O_{\text{min}}})}{R_L(V_I - V_{O_{\text{min}}})}, & \text{for } V_{O_{\text{max}}} \leq V_I - \frac{V_{O_{\text{min}}}}{2}. \end{cases} \]  \hspace{1cm} (101)

The diode must have a rated $V_{R_{\text{max}}}$ that can accommodate the maximum voltage stress $V_{DM_{\text{max}}}$, so from (71),

\[ V_{R_{\text{max}}} > V_I. \]  \hspace{1cm} (102)

As with the switch, the diode’s maximum-rated current $I_{F(AV)_{\text{max}}}$ must accommodate $I_{DM_{\text{max}}}$ and therefore $I_{SM_{\text{max}}}$. Hence,

\[ I_{F(AV)_{\text{max}}} > I'_{SM_{\text{max}}}. \]  \hspace{1cm} (103)

The value of inductance $L$ that causes the dynamic converter to operate precisely at the CCM-DCM boundary is given by (22); $L \big|_{CCM-DCM}$ therefore also describes the minimum inductance $L_{\text{min}}$ that will keep the converter in CCM at all output
levels, and

$$L_{\min} = \frac{R_L (V_I - V_{O\min})}{2f_s V_I \eta_{\min}}$$  \hspace{1cm} (104)$$

where

$$\eta_{\min} \cong \eta'_{\min} = \eta'_{\min} \bigg|_{V_o = V_{O\min}}$$

$$= \left[ 1 + \frac{f_s V_I^2 R_L (C_{oss} - C_{rss})}{V_{O\min}} \sqrt{\frac{V_{I'S}}{V_I - V_{O\min}} + \frac{4V_{O\min} (r_{DS}-R_F)}{3R_L V_I} + \frac{4R_F}{3R_L} + \frac{V_F}{V_{O\min}} - \frac{V_F}{V_I}} \right]^{-1}$$  \hspace{1cm} (105)$$

The inductor’s maximum rated current $I_{dc}$ must be large enough to handle the inductor current stress $I_{LM\text{max}}$ which, like the diode, is equal to $I_{SM\text{max}}$. Therefore,

$$I_{dc} > I'_{SM\text{max}}. \hspace{1cm} (106)$$

The minimum value of capacitance $C$ that will suppress the output ripple to $V_{r(max)}$ or less, for all output, can be determined from (52). Since $C$ is inversely proportional to $V_{r(max)}$, (52) is rewritten as

$$V_{r(max)} = \frac{V_I}{4f_s L \eta_r} \left( r_C + \frac{1}{8f_s C_{\min}} \right) \hspace{1cm} (107)$$

and

$$C_{\min} = \frac{V_I}{32f_s^2 L \eta_r V_{r(max)} - 8f_s r_C V_I} \hspace{1cm} (108)$$
where

\[
\eta_r \approx \eta'_r = \eta' \bigg|_{V_O=0.5V_I}
\]

\[
= \left\{1 + 4f_s R_L (C_{oss} - C_{rss}) \sqrt{\frac{2V'_DS}{V_I} + \frac{V_F}{V_I} + \frac{R_F}{R_L}} + \frac{r_{DS} - R_F}{2R_L} \left[1 + \frac{1}{12} \left(\frac{V_I}{V_I - V_{Omin}}\right)^2\right]\right\}^{-1}
\]  

(109)

An additional constraint on the value \( C \) is due to the capacitor’s parasitic ESR \( r_C \). This parasitic resistance must remain smaller than some maximum threshold, such that

\[
r_C < \frac{4f_s L \eta_r V_r(\max)}{V_I}.
\]  

(110)

The maximum rated voltage across the capacitor \( V_{dc} \) must be sufficient for the stresses \( V_{CM\max} \); therefore, from (76),

\[
V_{dc} > V_{O\max}.
\]  

(111)

### 2.8.2 Procedure

Certain operating characteristics of the dynamic buck converter are typically established beforehand as desired specifications and/or available constraints. For the procedure described herein, it is assumed \( V_I, V_{O\min}, V_{O\max}, R_L, V_{r(\max)} \), and \( f_s \) have already been selected. The four discrete components of the converter are chosen as follows:

1. The worst-case maximum instantaneous switch/diode/inductor current \( I'_{SM\max} \) given by (68) and (101) is calculated, based on \( V_I, V_{O\min}, V_{O\max}, \) and \( R_L \).

2. The diode is selected such that (a) \( V_{R\max} > V_I \), (b) \( I_{F(AV)\max} > I'_{SM\max} \), (c) \( V_F \leq 0.9 \text{ V} \), and (d) \( (t_{rr}, t_{fr}) \ll \frac{1}{f_s} \).

42
3. The switch is selected such that (a) \( V_{DSS_{\text{max}}} > V_I + V_F + \frac{V_{O_{\text{max}}}}{R_L} \) from the nominal forward voltage and resistance of the diode, (b) rated \( I_{D_{\text{max}}} > I'_{S_{\text{M_{max}}}} \), (c) rated \( P_{D_{\text{max}}} > \frac{V_{O_{\text{max}}}}{R_L} \), (d) rated operating frequency is greater than \( f_s \), and (e) rated output capacitance \( C_{\text{oss}} \) and on-resistance \( r_{DS} \) are as small as possible.

4. The estimated total efficiency \( \eta' \) is calculated for \( V_O = V_{O_{\text{min}}} \) and \( V_O = \frac{V_I}{2} \), per (105) and (109), to obtain \( \eta_{\text{min}} \) and \( \eta_r \), respectively.

5. The inductor is selected such that (a) \( L \geq L_{\text{min}} \), (b) rated \( I_{dc} > I'_{S_{\text{M_{max}}}} \), and (c) rated self-resonant frequency (SRF) is greater than \( f_s \).

6. The capacitor is selected such that (a) rated \( V_{dc} > V_{O_{\text{max}}} \), (b) available rated \( r_C \) is sufficiently small, per (110), and (c) \( C \geq C_{\text{min}} \).

2.8.3 Design Example

An asynchronous buck converter is designed as a dynamic power supply with the selected specifications \( V_I = 28 \text{ V} \), \( V_{O_{\text{min}}} = 3 \text{ V} \), \( V_{O_{\text{max}}} = 23 \text{ V} \), \( R_L = 75 \Omega \), \( V_{r(max)} = 140 \text{ mV} \), and \( f_s = 1 \text{ MHz} \).

Since

\[
V_I - \frac{V_{O_{\text{min}}}}{2} = 28 - \frac{3}{2} = 26.5 \text{ V}
\] (112)

\[
> V_{O_{\text{max}}} = 23 \text{ V}
\] (113)

the worst-case maximum instantaneous switch current is

\[
I'_{S_{\text{M_{max}}}} = \frac{V_{O_{\text{max}}} (2V_I - V_{O_{\text{min}}} - V_{O_{\text{max}}})}{R_L (V_I - V_{O_{\text{min}}})} = \frac{23 (2 \times 28 - 3 - 23)}{75 (28 - 3)} = 0.368 \text{ A.}
\] (114)
A MURS120T3 high-speed power rectifier diode is selected, with rated parameters

\[ V_{R_{\text{max}}} = 200 \text{ V} > V_I = 28 \text{ V} \quad (115) \]

\[ I_{F(\text{AV})_{\text{max}}} = 1 \text{ A} > I'_{S_{\text{M}_{\text{max}}}} = 0.368 \text{ A} \quad (116) \]

\[ V_F = 0.875 \text{ V} < 0.9 \text{ V} \quad (117) \]

\[ R_F = 1.3 \Omega \quad (118) \]

\[ (t_{rr}, t_{fr}) = (35 \text{ ns}, 25 \text{ ns}) \ll \frac{1}{f_s} = \frac{1}{1 \text{ MHz}} = 1000 \text{ ns}. \quad (119) \]

A VRF148A Si RF power MOSFET is chosen as the switch, with rated parameters

\[ V_{DSS_{\text{max}}} = 170 \text{ V} > V_I + V_F + \frac{V_{O_{\text{max}}} R_F}{R_L} = 28 + 0.875 + \frac{23 \times 1.3}{75} = 29.27 \text{ V} \quad (120) \]

\[ I_{D_{\text{max}}} = 6 \text{ A} > I'_{S_{\text{M}_{\text{max}}}} = 0.368 \text{ A} \quad (121) \]

\[ P_{D_{\text{max}}} = 115 \text{ W} > \frac{V_{O_{\text{max}}}^2}{R_L} = \frac{23^2}{75} = 7.053 \text{ W} \quad (122) \]

\[ f_1 = 30 \text{ MHz} > f_s = 1 \text{ MHz} \quad (123) \]

\[ C_{oss} = 40 \text{ pF} \quad (124) \]

\[ C_{rss} = 2.6 \text{ pF} \quad (125) \]

\[ V'_{DS} = 50 \text{ V} \quad (126) \]

\[ r_{DS} = 4 \Omega. \quad (127) \]
The minimum total efficiency of the dynamic buck converter is

$$\eta_{\text{min}} \approx \left[ 1 + \frac{f_s V^2 R_L (C_{\text{oss}} - C_{\text{res}})}{V_O^{\text{min}}} \sqrt{\frac{V_{DS}'}{V_I - V_O^{\text{min}}} + \frac{4V_O^{\text{min}} (r_{DS} - R_F)}{3R_L V_I} + \frac{4R_F}{3R_L} + \frac{V_F}{V_O^{\text{min}} - V_I}} \right]^{-1}$$

$$= \left[ 1 + \frac{1 \times 10^6 \times 28^2 \times 75 (40 - 2.6) \times 10^{-12}}{3^2} \sqrt{\frac{50}{28 - 3} + \frac{4 \times 3 (4 - 1.3)}{3 \times 75 \times 28} + \frac{4 \times 1.3}{3 \times 75} + \frac{0.875}{3} - \frac{0.875}{28}} \right]^{-1}$$

$$= 0.6119. \quad (128)$$

The minimum inductance that will keep the converter in CCM at all times is

$$L_{\text{min}} = \frac{R_L (V_I - V_O^{\text{min}})}{2f_s V_I \eta_{\text{min}}}$$

$$= \frac{75 (28 - 3)}{2 \times 10^6 \times 28 \times 0.6119}$$

$$= 54.72 \, \mu\text{H}. \quad (129)$$

Therefore, an inductor is chosen with

$$L = 56 \, \mu\text{H} \quad (130)$$

$$I_{dc} = 0.93 \, \text{A} > I_{SM_{\text{max}}} = 0.368 \, \text{A} \quad (131)$$

and rated parasitic dc resistance

$$r_L = 0.19 \, \Omega. \quad (132)$$
When output ripple is maximum, the total converter efficiency is

\[ \eta_r \simeq \left\{ 1 + 4f_s R_L (C_{oss} - C_{rss}) \sqrt{\frac{2V_{DS}}{V_I}} + \frac{V_F}{V_I} + \frac{R_F}{R_L} + \frac{r_{DS}-R_F}{2R_L} \left[ 1 + \frac{1}{12} \left( \frac{V_I}{V_I-V_{Omin}} \right)^2 \right] \right\}^{-1} \]

\[ = \left\{ 1 + \left[ 4 \times 10^6 \times 75 (40 - 2.6) \times 10^{-12} \sqrt{\frac{2 \times 50}{28}} + \frac{0.875}{75} + \frac{1.3}{2 \times 75} \left[ 1 + \frac{1}{12} \left( \frac{28}{28-3} \right)^2 \right] \right] \right\}^{-1} \]

\[ = 0.9177. \quad (133) \]

The capacitor’s maximum dc voltage rating must be greater than \( V_{Omax} \), and its parasitic resistance must be

\[ r_C < \frac{4f_sL}{V_I} \eta_r V_{r(max)} \]

\[ < \frac{4 (1 \times 10^6) (56 \times 10^{-6}) (0.9117) (0.140)}{28} \]

\[ < 1.0211 \Omega. \quad (134) \]

Therefore, a series of low-ESR tantalum capacitors are chosen where

\[ V_{dc} = 50 \text{ V} > V_{Omax} = 23 \text{ V} \quad (135) \]

\[ r_C = 0.8 \Omega < 1.0211 \Omega. \quad (136) \]

The minimum capacitance that may be utilized for the design is

\[ C_{min} = \frac{V_I}{32f_s^2 L \eta_r V_{r(max)} - 8f_s r_C V_I} \]

\[ = \frac{28}{32 (1 \times 10^6)^2 (56 \times 10^{-6}) (0.9117) (0.140) - 8 (1 \times 10^6) (0.8) (28)} \]

\[ = 0.5653 \mu F. \quad (137) \]
The smallest available capacitor in the aforementioned 50-V, 0.8-Ω ESR series is

\[ C = 2.2 \, \mu F \]  \hspace{1cm} (138)

and this value is selected for the design.

The circuit of the dynamic buck converter design with VRF148A power switch, MURS120T3 diode, 56-μH / 0.93-A / 0.19-Ω inductor, and 2.2-μF / 50 V / 0.8-Ω capacitor is shown in Fig. 17.

![Circuit Diagram](image_url)

Figure 17: Dynamic buck converter power stage design for \(3 \, V \leq V_O \leq 23 \, V\), \(V_r \leq 140 \, mV\).
3 Experimental Verification of DC Analysis and Design

3.1 Test Setup

The design completed in Section 2.8.3 is utilized to test the validity of both the dc analysis and design procedure. A prototype of the dynamic buck converter power stage circuit is built in order to measure all operating characteristics. The test hardware, seen in Fig. 67, is mounted on a custom PCB and contains the discrete components of the power stage along with an LTC4440-5 integrated high-side gate driver to control the switch. A schematic of the power stage with driver is shown in Fig. 18.

![Schematic of Dynamic Buck Converter Power Stage with Driver](image)

Figure 18: Dynamic buck converter power stage design with high-side gate driver.
The test bench is shown in Fig. 19 and consists of an Agilent E3631A dc power supply and Agilent 33220A 20-MHz waveform generator providing $V_I$ and $v_{PWM}$, respectively. A Tektronix TDS2004C 70-MHz (20 MHz bandwidth-limited) digital oscilloscope is used to view and measure waveforms $v_{PWM}(t)$, $v_{GS}(t)$, and $i_L(t)$. The floating gate drive signal $v_{GS}$ is captured via a Probe Master 4231 differential probe, while inductor current $i_L$ is obtained with a Tektronix AM503 amplified current probe. The dc ammeter is a Velleman DVM850BL (1.6-Ω series resistance); the voltmeter is a Fluke 77 DMM. A diagram indicating all current and voltage signals measured is shown in Fig. 20.
Figure 20: Currents and voltages measured for dc characterization of variable-output buck converter design.

The measurement procedure consists of manually varying duty cycle $D$ of the gate drive signal via the waveform generator, in minimal increments of 1%, while monitoring the converter output $V_O$ on the dc voltmeter. Circuit measurements are then taken for each value of $V_O$ in evenly-spaced intervals, across the full range of output from $V_{Omin} = 3\, \text{V}$ to $V_{Omax} = 23\, \text{V}$.

### 3.2 Comparison of Theoretical and Measured DC Characteristics

The theoretical dc operation of the dynamic buck converter can be assessed by plotting the expressions derived in Sections 2.3 - 2.7, using specifications, component values, and parasitics obtained from the design procedure. This section compares theoretical plots with measured performance data, captured from the actual circuit, for key parameters $\eta(V_O)$, $V_O(D)$, $\Delta i_L(V_O)$, $i_L(t)$, $P_O(V_O)$, and $V_r(V_O)$. 
3.2.1 Efficiency

The theoretical total efficiency of the dynamic buck converter can be plotted as a function of $V_O$ via the approximation $\eta \approx \eta'$ given in (98), and is shown in Fig. 21.

The measured total efficiency of the converter is obtained by measuring the dc input and output current and voltage, respectively, for a given measured value of $V_O$ and then time-averaging the product over one switching period $T_s$. The ratio

$$\eta_{\text{Measured}} = \frac{[I_O(\text{measured})V_O(\text{measured})]_{AV}}{[I_I(\text{measured})V_I(\text{measured})]_{AV}}$$

(139)

can then be calculated for each $V_O$. The measured total efficiency is shown in Fig. 22.

![Theoretical total efficiency of dynamic buck converter design over 20-V operating range.](image)

Figure 21: Theoretical total efficiency of dynamic buck converter design over 20-V operating range.
Figure 22: Comparison of measured and theoretical total efficiency of dynamic buck converter over 20-V operating range.

While it may initially appear as though the measured and theoretical results exhibit significant disparity, it should be noted that theoretical efficiency depends heavily upon device parasitics that must be gleaned from manufacturer data and not measured or calculated directly. The plot in Fig. 23 demonstrates how the curves fit extremely well if the theoretical $R_F$ and $C_{oss}$ are increased by less than an order of magnitude and $r_{DS}$ is decreased. It is not unreasonable to assume that, in practice, the actual parasitics of the Si semiconductors may vary similarly. This is especially true for $C_{oss}$, which increases on a logarithmic scale as $V_{DS}$ decreases, per Fig. 11.
3.2.2 DC Transfer Characteristic

The theoretical lossy dc transfer function $M_{V_{DC}}$ can be evaluated by plotting $V_O$ as a function of $D$ as shown in (10) and (12), i.e.,

$$V_O = \eta DV_I. \quad (140)$$

The expression for $\eta$ derived in (98) is substituted into (12) and plotted in Fig. 24.
Figure 24: Theoretical dc transfer characteristic of variable-output voltage buck converter design.

The measured transfer characteristic is obtained by setting the duty cycle on the pulse generator and measuring both $V_O$ and $D$ on the oscilloscope. The actual duty cycle $D_{GS}$ of gate-drive signal $v_{GS}$ is measured directly by the oscilloscope, since it may vary from the reference value of $D$ set on the pulse generator. This can be seen in Fig. 25; if $D$ is set to 51% on the waveform generator, the actual duty cycle delivered to the gate of the switch is instead 49.3%. The measured and theoretical (calculated) dc duty-cycle-to-output-voltage transfer characteristics are compared in Fig. 26.
Figure 25: Comparison of driver input $v_{PWM}$ (top) and gate drive $v_{GS}$ (bottom) signals, showing delay and duty cycle loss of over 1%.

Figure 26: Comparison of measured and theoretical dc transfer characteristics of variable-output voltage buck converter.

The slope of the measured transfer characteristic begins to decrease as $D$ is reduced and the output approaches $V_{Omin}$. The switching voltage waveforms in Fig. 27 illustrate, in a functional sense, why this is the case. Ideally the switch is ON for
approximately the same duration that \( v_{GS} \) is high, i.e.,

\[
D \equiv 1 - D_{DS}
\]

(141)

where \( D_{DS} \) is duty cycle of the drain-to-source voltage \( v_{DS} \). This relationship generally holds true in the measured circuit at larger values of \( D \). At smaller \( D \), however, the rise time of \( v_{DS} \) increases, causing the switch to remain ON for longer than desired. In this case, \( D < (1 - D_{DS}) \) and results in output \( V_O \) that is proportionally larger than expected for the given value of \( D \). This phenomenon can also be observed in the calculated transfer characteristic; Fig. 28 shows an expanded view for \( 0 \leq V_O \leq V_I \), demonstrating the same trend, albeit at much lower values of \( V_O \).

Figure 27: Experimental disparity between \( D \) and \( 1 - D_{DS} \) contributing to nonlinearity in measured \( V_O(D) \) transfer characteristic, \( V_O \approx V_{min} \).
Figure 28: DC transfer characteristic of variable-output buck converter, $0 \leq V_O \leq V_I$.

### 3.2.3 Peak-to-Peak Inductor Current

It is useful to plot the theoretical peak-to-peak inductor current $\Delta i_L$ per (13) as a function of $V_O$ or $D$ since this quantity affects all aspects of dynamic converter performance. It also allows for the maximum peak-to-peak $\Delta i_{L_{\text{max}}}$ to be gauged and its corresponding value of $V_O$ or $D$ to be determined. This plot is shown as a function of $V_O$ in Fig. 29. The theoretical maximum value of $\Delta i_L$ is therefore

$$\Delta i_{L_{\text{max}}} = 0.1366 \text{ A}$$  \hspace{1cm} (142)

and occurs at

$$V_O = V_{O(\Delta_{\text{max}})} = 13.4 \text{ V}.$$  \hspace{1cm} (143)
The measured peak-to-peak inductor current is shown in Fig. 30. The measured maximum value of $\Delta i_L$ is

$$\Delta i_{L\text{max(measured)}} = 0.128 \text{ A}$$  \hspace{1cm} (144)

and occurs at

$$V_O = V_O(\Delta_{\text{max,measured}}) = 13.42 \text{ V}.$$  \hspace{1cm} (145)

Figure 29: Theoretical peak-to-peak inductor current over operating range of variable-output buck converter design.
Experimental and theoretical curves are reasonably well-fit, and as the calculated values predict, $\Delta i_{L_{\text{max}}(\text{measured})}$ occurs when $V_{O(\text{measured})} \approx 13.4$ V. It should be noted that the measured peak-to-peak trend is shifted lower for all output levels. However this is easily accounted for by the fact that the actual value of $L$ used for the test circuit may be larger than the labeled value; indeed, the manufacturer data lists a tolerance of $\pm 15\%$ for the 56-$\mu$H inductor selected. As shown in Fig. 31, the nominal calculated inductance need only be increased by 7% for the curves to match within a reasonable margin of measurement accuracy.
3.2.4 Inductor Current Waveforms

The theoretical inductor current $i_L(t)$ can be plotted for any given value of $V_O$ by substituting (9), (12), (17), and (54) into (6), i.e.,

$$i_L(t) = \begin{cases} 
\frac{V_I - V_O t}{L} + \frac{V_O}{R_L} - \frac{V_I V_O - V_O^2}{2 f_s L V_I \eta}, & \text{for } 0 < t \leq \frac{V_O}{f_s V_I \eta} \\
\left(-\frac{V_I R_L - V_O (R_F + R_L)}{R_L L}\right) \left(1 - \frac{V_O}{f_s V_I \eta}\right) + \frac{V_O}{R_L} + \frac{V_I V_O - V_O^2}{2 f_s L V_I \eta}, & \text{for } \frac{V_O}{f_s V_I \eta} < t \leq \frac{1}{f_s}
\end{cases} \quad (146)$$

and is shown for three critical output levels of $V_O = 3$ V, 13.4 V, and 23 V in Fig. 32.

From (17), the dc value of inductor current at these output levels is

$$I_{L(min)} = \frac{V_{O_{min}}}{R_L} = \frac{3}{75} = 0.040 \text{ A} \quad (147)$$

$$I_{L(max)} = \frac{V_{O_{max}}}{R_L} = \frac{13.4}{75} = 0.179 \text{ A} \quad (148)$$
\[ I_{L(max)} = \frac{V_{O_{\text{max}}}}{R_L} = \frac{23}{75} = 0.307 \text{ A}. \] (149)

The measured inductor current waveforms are shown in Fig. 33 for the same three critical output levels. The measured dc inductor current is

\[ I_{L(min, \text{measured})} = 0.040 \text{ A} \] (150)

\[ I_{L(\Delta_{\text{max}}, \text{measured})} = 0.1798 \text{ A} \] (151)

\[ I_{L(max, \text{measured})} = 0.310 \text{ A}. \] (152)

Despite visible high-frequency switching transients, the measured and theoretical inductor current waveforms are in good agreement. The experimental discrepancy of the dc inductor current level is less than 3 mA. More importantly, these waveforms demonstrate that the dynamic converter operates in CCM at all times.

![Figure 32: Theoretical inductor current waveforms of dynamic buck converter design, for \( V_O = 3 \text{ V}, \) \( V_O = 13.4 \text{ V}, \) and \( V_O = 23 \text{ V}. \)](image-url)
Figure 33: Measured inductor current waveforms of dynamic buck converter for (a) $V_O = 23$ V, (b) $V_O = 13.4$ V, and (c) $V_O = 3$ V.
3.2.5 Output Power

The theoretical output power is

\[ P_O = \frac{V_O^2}{R_L} \]  \hspace{1cm} (153)

and is plotted as a function of \( V_O \) in Fig. 34. The minimum and maximum calculated output power is therefore

\[ P_{O_{\text{min}}} = \frac{3^2}{15} = 0.120 \text{ W} \]  \hspace{1cm} (154)

\[ P_{O_{\text{max}}} = \frac{23^2}{15} = 7.053 \text{ W}. \]  \hspace{1cm} (155)

The measured output power is

\[ P_{O(\text{measured})} = I_{O(\text{measured})} V_{O(\text{measured})} \]  \hspace{1cm} (156)

and is shown in Fig. 35. The minimum and maximum measured power output of the dynamic converter is

\[ P_{O_{\text{min}}(\text{measured})} = I_{O_{\text{min}}(\text{measured})} V_{O_{\text{min}}(\text{measured})} = 0.040 \times 3.01 = 0.1204 \text{ W} \]  \hspace{1cm} (157)

\[ P_{O_{\text{max}}(\text{measured})} = I_{O_{\text{max}}(\text{measured})} V_{O_{\text{max}}(\text{measured})} = 0.310 \times 22.9 = 7.099 \text{ W}. \]  \hspace{1cm} (158)

The measured and theoretical output power are in very close agreement across the entire 20-V operating range of the converter.
Figure 34: Theoretical output power of dynamic buck converter design.

Figure 35: Comparison of measured and theoretical output power of dynamic buck converter design.
3.2.6 Output Ripple Voltage

As shown in (41) the output ripple voltage $V_r$ is directly proportional to $\Delta i_L$, and varies with $V_O$ and $D$. The ripple may therefore be plotted as a function of $V_O$ to determine the theoretical maximum ripple $V_{r(max)}$ of the dynamic converter design. This plot is shown in Fig. 36. From both the plot and (41),

$$V_{r(max)} = \Delta i_{Lmax} \left( r_C + \frac{1}{8fsC} \right) = 0.1366 \left( 0.8 + \frac{1}{8 \times 10^6 \times 2.2 \times 10^{-6}} \right) = 0.117 \text{ V}$$

(159)

which occurs at $V_O = V_{O(\Delta max)} = 13.4 \text{ V}$. The measured output ripple is shown in Fig. 37. The measured maximum value of $V_r$ is

$$V_{r(max, measured)} = 0.120 \text{ V}$$

(160)

and occurs at

$$V_O = V_{O(\Delta max, measured)} = 13.41 \text{ V}.$$ 

(161)

The measured output ripple closely follows the trend of the theoretical values, and remains well under the specified $V_{r(max)} \leq 140 \text{ mV}$. As expected from the plot of $\Delta i_{Lmax(measured)}$, $V_{r(max, measured)}$ occurs at approximately $V_O = 13.4 \text{ V}$. 

65
Figure 36: Measured output ripple voltage of dynamic buck converter design over full range of output.

Figure 37: Measured output ripple voltage compared to theoretical ripple for full operating range of dynamic buck converter.
3.2.7 Device Stresses

The theoretical maximum current stresses $I_{SMmax}$, $I_{DMmax}$, $I_{LMmax}$ of the switch, diode, and inductor are, from (114),

$$I_{SMmax} = I_{DMmax} = I_{LMmax} \approx I'_{SMmax}$$

$$= 0.368 \text{ A.} \quad (162)$$

The actual stresses can be measured by capturing waveforms of the current through the switch, diode, and inductor when $V_O = V_{Omax}$. As shown in Fig. 38, the respective maximum current stresses are

$$I_{SMmax(\text{measured})} = 0.360 \text{ A} \quad (163)$$

$$I_{DMmax(\text{measured})} = 0.368 \text{ A} \quad (164)$$

$$I_{LMmax(\text{measured})} = 0.320 \text{ A.} \quad (165)$$

if transients of $f \gg f_s$ are neglected.

The theoretical maximum voltage stresses $V_{SMmax}$, $V_{DMmax}$, $V_{CMmax}$ of the switch, diode, and capacitor are, from (56), (71), and (76),

$$V_{SMmax} = V_I + V_F + \frac{V_{Omax} R_F}{R_L} = 28 + 0.875 + \frac{23 \times 1.3}{75} = 29.27 \text{ V} \quad (166)$$

$$V_{DMmax} = V_I = 28 \text{ V} \quad (167)$$

$$V_{CMmax} \approx V_{Omax} = 23 \text{ V.} \quad (168)$$

As with current, the actual voltage stresses can be measured by capturing waveforms of the voltage across the switch, diode, and capacitor when $V_O = V_{Omax}$. Neglecting
high-frequency transients and ringing, the measured maximum voltage stresses are shown in Fig. 39 to be

\[
V_{SM_{\text{max (measured)}}} = 30.8 \text{ V} \tag{169}
\]

\[
V_{DM_{\text{max (measured)}}} = 28.8 \text{ V} \tag{170}
\]

\[
V_{CM_{\text{max (measured)}}} = 23.2 \text{ V}. \tag{171}
\]

The measurements indicate slightly larger switch and diode voltage stresses than those calculated via dc analysis. Discrepancies on the order of 5% or less are typically not significant from a design standpoint, since standard engineering practice dictates a reasonable margin should be added when selecting devices for rated maximum safe operation. However, from an analytical perspective, this error is likely due to diode forward resistance \(R_F\) being larger than the nominal value, as implied by the plot of measured total efficiency in Section 3.2.1. If it is assumed that actual forward resistance \(R'_F\) is 5 times larger per Fig. 23, i.e.,

\[
R'_F = 5R_F = 5 \times 1.3 = 6.5 \Omega \tag{172}
\]

then from (56) the theoretical maximum voltage stress of the switch becomes

\[
V_{SM_{\text{max}}} = V_I + V_F + \frac{V_{O_{\text{max}}}R'_F}{R_L} = 28 + 0.875 + \frac{23 \times 6.5}{75} = 30.87 \text{ V} \tag{173}
\]

which is in very close agreement with the measured stress.
Figure 38: Measured maximum current stresses of (a) switch $I_{SM_{max}}$, (b) diode $I_{DM_{max}}$, and (c) inductor $I_{LM_{max}}$, $V_O = 23\,\text{V}$. 
Figure 39: Measured maximum voltage stresses of (a) switch $V_{SM_{\text{max}}}$, (b) diode $V_{DM_{\text{max}}}$, and (c) capacitor $V_{CM_{\text{max}}}$. 
### 3.3 Results

The measured data demonstrates the validity of both the dc analysis and design methodology of the dynamic buck converter, accounting for vagaries in semiconductor parasitics and the rated tolerance of the inductor value. Table 2 shows the maximum discrepancy encountered in each set of measurements, while Table 3 shows that all critical design specifications and operating parameters have been met.

**Table 2**

**Experimental Error in Measurements of DC Operating Characteristics**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Maximum $\Delta$ $(Experimental - Theoretical)$</th>
<th>Error $(\frac{Experimental - Theoretical}{Theoretical} \times 100%)$</th>
<th>Operating point $V_O$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\eta$</td>
<td>-0.1341</td>
<td>-22.1%</td>
<td>3 V</td>
</tr>
<tr>
<td>$D$</td>
<td>-0.0722</td>
<td>-47.7%</td>
<td>3 V</td>
</tr>
<tr>
<td>$\Delta i_L$</td>
<td>-16.2 mA</td>
<td>-20.7%</td>
<td>3 V</td>
</tr>
<tr>
<td>$I_L$</td>
<td>6.7 mA</td>
<td>2.6%</td>
<td>19 V</td>
</tr>
<tr>
<td>$P_O$</td>
<td>0.153 W</td>
<td>3.2%</td>
<td>19 V</td>
</tr>
<tr>
<td>$V_r$</td>
<td>12.92 mV</td>
<td>19.3%</td>
<td>23 V</td>
</tr>
<tr>
<td>$I_{SMmax}$</td>
<td>-8 mA</td>
<td>-2.2%</td>
<td>23 V</td>
</tr>
<tr>
<td>$I_{DMmax}$</td>
<td>0 mA</td>
<td>0.0%</td>
<td>23 V</td>
</tr>
<tr>
<td>$I_{LMmax}$</td>
<td>-48 mA</td>
<td>-13.0%</td>
<td>23 V</td>
</tr>
<tr>
<td>$V_{SMmax}$</td>
<td>1.53 V</td>
<td>5.2%</td>
<td>23 V</td>
</tr>
<tr>
<td>$V_{DMmax}$</td>
<td>0.8 V</td>
<td>2.9%</td>
<td>23 V</td>
</tr>
<tr>
<td>$V_{CMmax}$</td>
<td>0.2 V</td>
<td>0.7%</td>
<td>23 V</td>
</tr>
</tbody>
</table>
# Table 3

## Critical Specifications of Variable-Output Buck Converter Design

<table>
<thead>
<tr>
<th>Parameter</th>
<th>(Rated) Value</th>
<th>Measured</th>
<th>Within spec?</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{Omin}$</td>
<td>3 V</td>
<td>3.00 V</td>
<td>Yes</td>
</tr>
<tr>
<td>$V_{Omax}$</td>
<td>23 V</td>
<td>23.00 V</td>
<td>Yes</td>
</tr>
<tr>
<td>$V_{r(max)}$</td>
<td>140 mV</td>
<td>124 mV</td>
<td>Yes</td>
</tr>
<tr>
<td>Conduction mode</td>
<td>CCM, for all $V_O$</td>
<td>CCM</td>
<td>Yes</td>
</tr>
<tr>
<td>$I_{Dmax}$, $I_{SMmax}$</td>
<td>(6 A)</td>
<td>0.360 A</td>
<td>Yes</td>
</tr>
<tr>
<td>$V_{DSSmax}$, $V_{SMmax}$</td>
<td>(170 V)</td>
<td>30.8 V</td>
<td>Yes</td>
</tr>
<tr>
<td>$I_{F(AV)max}$, $I_{DMmax}$</td>
<td>(1 A)</td>
<td>0.368 A</td>
<td>Yes</td>
</tr>
<tr>
<td>$V_{R(max)}$, $V_{DMmax}$</td>
<td>(200 V)</td>
<td>28.8 V</td>
<td>Yes</td>
</tr>
<tr>
<td>$I_{dc}$, $I_{LMmax}$</td>
<td>(0.93 A)</td>
<td>0.320 A</td>
<td>Yes</td>
</tr>
<tr>
<td>$V_{dc}$, $V_{CMmax}$</td>
<td>(50 V)</td>
<td>23.2 V</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Experimental discrepancy greater than 20% is seen in parameters $\eta$, $D$, and $\Delta i_L$. The error in $\eta$ and $\Delta i_L$ can be explained by the tolerances inherent in nominal component values and device parasitics. The error in the dc transfer characteristic $V_O(D)$ is less attributable to either of these factors; in this case, adjusting theoretical component values and parasitics does not reduce discrepancy between the measured and calculated curves. However, from observation of the switching waveforms, it is known that switch takes longer to turn on when controlled by a narrow duty cycle pulse. This points to some inherent limitation of the switch itself, or driver IC used, or both, rather than the variable-output buck converter topology itself. While a solution to this problem is beyond the scope of this particular work, it forms a critical topic for future study.
4 Open-Loop AC Characteristics

The fundamental purpose of a dynamic power supply, whether used for envelope tracking or amplitude modulation, is to vary the dc output $V_O$ at some modulation frequency $f_m$. This results in a large-signal time-varying output $v_O(t)$. For a switching power supply used as a dynamic power source, $f_m$ is typically much less than $f_s$. The modulation frequency $f_m$ describes the rate at which $D$ is varied to prompt a corresponding change in instantaneous $V_O$, thereby generating $v_O(t)$. Thus, it is important to examine the behavior of the dynamic buck converter under conditions of continuously modulating output $v_O$, as opposed to several discrete fixed increments of $V_O$. This requires assessment of large-signal $v_O$ as a function of time; magnitude and phase as a function of $f_m$; and also the effect of modulation index on the output. Of similar key importance is the extent to which dynamic operation affects the efficiency of the power stage.

This chapter provides an overview of the theoretical ac characteristics of the PWM buck converter used as a dynamic power supply. Since dynamic power supplies are by definition modulated or controlled via an external source, this work focuses exclusively on open-loop response. A brief discussion is presented describing the applicability of existing ac theory and analysis to the proposed dynamic PWM buck converter. The suitability of simulation and experimental measurement to establishing ac characteristics for this work is also explained. The significant parameters of dynamic operation are described and the importance of the modulation reference signal is discussed. The simulation methodology for obtaining theoretical ac characteristics is described, and simulation results are presented. Finally, experimental results are presented, com-
pared to simulation, and key observations of ac performance are discussed.

4.1 Limits of Existing AC Theory and Use of Simulation and Measurement

PWM converters are nonlinear systems, and theoretical dynamic analysis has been derived only for very specialized (i.e., fixed-output) operating conditions [66]. The extant large-signal theory is grounded on assumptions of quasi-static operation; that is, it applies to relatively small shifts in instantaneous $D$ and therefore small shifts in instantaneous dc output current $I_L$. Small-signal dynamic modeling techniques are also used, but by definition these do not likely provide a full or accurate picture of large-signal operation. The extent to which small-signal techniques might be applied to theoretical analysis of a dynamic buck converter is itself a topic of further study.

Because existing theory applies distinctly to quasi-static and/or small signal operation of PWM buck converters, and because development of new theory for large-signal ac operation is beyond the scope of this work, simulation and measurement of the dynamic buck converter’s ac characteristics will instead be used to gain insight. Software-based circuit simulation of large-signal dynamic operating conditions will be undertaken as a baseline, and then compared against actual circuit performance to assess many of the same parameters provided for quasi-static operation in the literature. The design developed in Chapter 2, whose dc operation was verified both theoretically and experimentally, will be utilized for insight into ac operation.

4.2 Characteristics of Dynamic Operation

4.2.1 Modulation Reference Signal

Most practical applications of dynamic power supplies [34, 63] involve varying the supply output based on some time-dependent control voltage $v_{ref}(t)$ with frequency
In the case of a PWM converter operated as a dynamic supply, this implies $D$ will vary in proportion to the modulation control voltage. It is therefore useful, for the purposes of ac analysis, to consider the ac input of the dynamic buck converter in terms of the modulation reference signal $v_{ref}$, rather than instantaneous $D$ itself. The modulation reference voltage is then converted to a pulse waveform with proportionally time-dependent duty cycle $d(t)$. This approach allows for a clearer functional view of dynamic performance, and simplifies interpretation of the analysis.

As will be discussed further in this chapter, a relatively simple and effective means of generating a PWM signal with $d(t)$ is a ramp comparator circuit. This circuit, however, requires a dc offset $V_{REF}$ to be added to $v_{ref}$, proportional to the desired dc offset $V_{ODC\_nom}$ of the dynamic converter’s large-signal output. The resulting input used for the ac characterization in this work is therefore $v_{REF}(t)$. Assuming $v_{ref}$ is a pure sinusoid, the entire reference voltage input can be described in the frequency domain as

$$v_{REF}(\omega t) = V_{REF} + V_{Rm} \cos 2\pi f_m t.$$  \hspace{1cm} (174)

### 4.2.2 Large-signal Output

The proposed dynamic PWM buck converter can also be thought of as a low-frequency power amplifier with input $v_{ref}(t)$ and a dc offset $V_{ODC\_nom}$ at the output. From analysis provided in the existing literature, the large-signal output of the dynamic power supply is described as

$$v_O(\omega t) = V_{ODC\_nom} + V_{om}(f_m) \cos [2\pi f_m t + \phi(f_m)]$$  \hspace{1cm} (175)

where $V_{om}$ is the frequency-dependent peak value of the output’s large-signal ac component $v_o(\omega t)$. The coefficients in (175) can substituted in terms of the converter’s
respective dc and ac transfer characteristics $A_{VDC}$ and $A_{vac}(f_m)$, yielding

$$v_O(\omega t) = A_{VDC}V_{REF} + A_{vac}(f_m)V_{Rm}\cos[2\pi f_m t + \phi(f_m)]$$  \hspace{1cm} (176)

where $V_{REF}$ is a dc offset added to the input signal $v_{ref}$, and $V_{Rm}$ is the frequency-independent peak value of the output’s large-signal ac component.

### 4.2.3 Modulation Frequency Response

The open-loop transfer function of the dynamic converter based on modulated input-to-output is $A_{vm}$, given by

$$A_{vm} = \frac{v_O}{v_{REF}}.$$  \hspace{1cm} (177)

Hence, from (174) and (176),

$$A_{vm}(\omega t) = \frac{A_{VDC}V_{REF} + A_{vac}(f_m)V_{Rm}\cos[2\pi f_m t + \phi(f_m)]}{V_{REF} + V_{Rm}\cos 2\pi f_m t}.$$  \hspace{1cm} (178)

Because of the highly nonlinear nature of switch-mode power supplies, $A_{vac}$ and $\phi$ are difficult to quantify; existing theory is derived from small-signal modeling assumptions that cannot necessarily be made for operation of a PWM converter with a large-signal output swing. However, one assertion about the frequency response can be presented based on passive filter theory. The second-order $LC$ filter topology of the buck converter implies that a pole exists at

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$  \hspace{1cm} (179)

beyond which $v_O$ will attenuate at a rate of -20 dB per decade. Irrespective of any ac analysis that may be developed or applied to the dynamic buck converter, it can be stated that $f_o$ is the maximum possible bandwidth for the PWM buck converter operated as a dynamic supply. In the example of the power stage designed in Chapter

76
\[ f_0 = \frac{1}{2\pi \sqrt{(56 \times 10^{-6}) (2.2 \times 10^{-6})}} \]
\[ = 14.339 \text{ kHz.} \quad (180) \]

4.2.4 Modulation Index

The modulation index \( h \) describes how much signal swing the low-frequency ac output component \( v_{om}(t) \) exhibits with respect to the dc offset \( V_{ODC_{nom}} \), and is described as

\[ h = \frac{2V_{Rm}}{V_{Omax} - V_{Omin}} \quad (181) \]

where \( V_{Rm} \) is the peak value of \( v_{om} \). Modulation index is a useful means of characterizing dynamic power supply operation when the instantaneous output voltage does not actually reach either extreme of the full specified range \( (V_{Omin}, V_{Omax}) \) within a single cycle. It also allows the open-loop transfer function to be rewritten as

\[ A_{vm}(\omega t) = \frac{A_{VDC}V_{REF} + 0.5h (V_{Omax} - V_{Omin}) A_{vac}(f_m) \cos \left[2\pi f_m t + \phi(f_m)\right]}{V_{REF} + 0.5h (V_{Omax} - V_{Omin}) \cos 2\pi f_m t}. \quad (182) \]

4.2.5 Modulation Efficiency

The instantaneous efficiency of the dynamic converter under ac operation is \( \eta_m(t) \), which can be described in terms of the modulated input power \( P_i(t) \) and output power \( P_o(t) \) as

\[ \eta_m = \frac{P_o(t)}{P_i(t)} \quad (183) \]

Likewise,

\[ P_i(t) = i_I(t)v_I(t) \quad (184) \]

and

\[ P_o(t) = i_O(t)v_O(t) \quad (185) \]
where $i_I$, $i_O$, and $v_I$ are the large-signal time-varying input supply current, output current, and input supply voltage of the power stage. However, since $V_I$ and $R_L$ are fixed,

$$P_i(t) = V_I i_I(t) \quad (186)$$

$$P_o(t) = \frac{v_O^2(t)}{R_L} \quad (187)$$

and instantaneous modulation efficiency can expressed as a ratio of large-signal output voltage to input source current, i.e.,

$$\eta_m(t) = \frac{1}{V_I R_L} \times \frac{v_O^2(t)}{i_I(t)}. \quad (188)$$

The ratio in (188) implies that the instantaneous efficiency can be greater than one. It is therefore generally more informative to determine the average of $\eta_m(t)$ over some finite time, nominally $\frac{1}{f_m}$ or the modulation period $T_m$. This time-averaged, large-signal efficiency is the modulation efficiency $\eta_M$, defined as

$$\eta_M = \frac{f_m}{V_I R_L} \int_{t=0}^{T_m} \frac{v_O^2(t)}{i_I(t)} dt. \quad (189)$$

Alternately, if the practical restrictions of circuit simulation and experimental measurement make it difficult or impossible to divide waveforms prior to averaging, the following approximation can be used

$$\eta_M \simeq \frac{P_{o(AV)}}{P_{i(AV)}} \quad (190)$$

which represents the ratio of the time-averaged modulation input power $P_{o(AV)}$ to time-averaged output power $P_{i(AV)}$. This approximation can be expanded to

$$\eta_M \simeq \frac{1}{V_I R_L} \frac{\int_{t=0}^{T_m} v_O^2(t) dt}{\int_{t=0}^{T_m} i_I(t) dt} \quad (191)$$
4.3 AC Simulation Setup and Procedure

A baseline characterization of the magnitude, phase, efficiency, and step response of the dynamic buck converter is performed via simulation of the schematic in Fig. 40. This circuit modulates the output $v_O(t)$ of the dynamic buck converter power stage, based upon an external reference sinusoid $v_{REF}(t)$ with frequency $f_m$.

![Figure 40: Schematic of simulated dynamic buck converter with PWM generator.](image)

4.3.1 Subcircuits

The ac simulation circuit consists of three key sections; a PWM generator, a high-side gate driver, and the dynamic buck converter power stage. Since this work is only concerned with the characteristics of the power stage, the PWM generator and gate driver are modeled as ideal circuits. This is done in order to ensure the simulated results emphasize the dynamic performance of the power stage, which utilizes modeled non-ideal components.
**PWM Generator** The PWM generator consists of an ideal op-amp configured as a comparator, as shown in Fig. 41. This circuit compares the instantaneous value of the ideal ramp waveform $v_{ramp}$ to that of the modulating reference $v_{REF}$, modeled by a sinusoidal source with dc offset as shown. The frequency of $v_{ramp}$ is $f_s = 1$ MHz. Both waveforms are shown independently in Fig. 42.

![Figure 41: Simulated ideal op-amp ramp comparator.](image)

![Figure 42: Simulated ideal ramp comparator (a) non-inverting input $v_{REF}$ at $f_m = 100$ Hz and (b) inverting input $v_{ramp}$ at $f_s = 1$ MHz.](image)
As seen in Fig. 43, if the instantaneous value of the \( v_{REF} \) is higher than that of \( v_{ramp} \), the output of the comparator \( v_{PWM} \) clamps to the single-supply dc voltage \( V_{CC} = 3.75 \text{V} \). Otherwise, at every instance the value of \( v_{ramp} \) is greater than \( v_{REF} \), the comparator output is 0 V. If the ramp function has a linear rise and an instantaneous drop, and the op-amp has a slew rate large enough to track \( v_{ramp} \), the duty cycle of comparator output \( v_{PWM} \) is directly-proportional to the instantaneous magnitude of \( v_{REF} \), sampled at a rate of \( f_s \). The value of \( V_{CC} \) determines the magnitude of the pulse output, and is selected to be equal to the required gate drive signal peak voltage \( V_{GS} \). In the case of the VRF148A switch model used in simulation, \( V_{GS} \approx 3.75 \text{V} \).
Figure 43: Simulated PWM generation, via ideal ramp comparator, for (a) $D = 0.846$, (b) $D = 0.477$, and (c) $D = 0.127$. 
**Ideal Gate Driver**  An ideal gate driver, shown in Fig. 44 is utilized to convey $v_{PWM}$ to the floating gate and source terminals of the switch. This circuit is simply an ideal voltage-controlled-voltage-source with a gain of $k = 1$; its output is a floating or “high-side” voltage $v_{GS}$ - otherwise identical to $v_{PWM}$ - which turns the switch on and off.

![Diagram](image)

Figure 44: Simulated ideal gate driver.

**Power Stage**  The simulated power stage circuit, based on the design derived in Chapter 2, is shown in Fig. 45. Manufacturer-supplied models of both semiconductor devices are used, and both passive components are simulated with their respective nominal parasitic resistance and ESR. The converter supply voltage remains a fixed, ideal dc source, and the drive signal at the gate of the switch is likewise an ideal pulse train whose duty cycle is modulated by the magnitude of the sinusoidal reference $v_{REF}$. 

83
4.3.2 Procedure

The Synopsys Saber platform is used for capture and simulation, with waveforms viewed in Synopsys Cosmoscope. Key waveforms of interest are the input reference $v_{REF}(t)$, the power stage output $v_O(t)$, the output power $P_o(t)$ across the load, and the input power $P_i(t)$. Eight discrete values of $50 \text{ Hz} \leq f_m \leq 100 \text{ kHz}$ are selected as waveform capture points. For each value of $f_m$, the frequency of $v_{REF}$ is set, and a transient simulation of suitable length is run. The simulated waveforms of $v_{REF}, v_O, P_o,$ and $P_i$ are viewed in Cosmoscope over one modulation period $T_m$. The built-in measurement utility and cursors are used to measure $P_{o(AV)}, P_{i(AV)}, V_{om}, V_{Rm}$, and time delay, from which $\eta_M, A_{vm},$ and $\phi$ may be calculated and plotted in MATLAB as a function of $f_s$. The transient response of the power stage can also be simulated by simply replacing $v_{REF}$ with an ideal pulse source of the same peak-to-peak magnitude and a period of $\frac{1}{100 \text{ Hz}} = 10 \text{ ms}$. The rising and falling edge of the pulse may then be clearly viewed in comparison to $v_O$ using Cosmoscope, allowing rise time $t_r$ and fall time $t_f$ to be measured and the damping to be observed.
4.4 Simulated AC Characteristics

4.4.1 Large-Signal Output Response

The general shape of the simulated input and output waveforms at a very low modulation frequency can be seen in Fig. 46. The Cosmoscope waveform calculator is used to multiply simulated $v_{REF}$ by 2.64 in order to normalize the gain and simplify the visual comparison with $v_O$.

Figure 46: Simulated $P_i$, $P_o$, $v_{REF}$, and modulated output voltage $v_O$ of dynamic buck converter, $f_m = 50$ Hz, $h = 1$. 
The effect on simulated $v_O$ of increasing the modulation frequency is depicted in Fig. 47. It can be seen that, as modulation frequency increases beyond 500 Hz,

- the ac component of $v_O$ is attenuated.
- the dc component of $v_O$ increases.
- phase shift increases.
- significant harmonic distortion is introduced, first in the lower half of the sinu-
  soid.

Figure 47: Simulated input $v_{REF}$ and output $v_O$ of dynamic buck converter, $h = 1$, for (a) $f_m = 100$ Hz, (b) $f_m = 1$ kHz, (c) $f_m = 10$ kHz.
4.4.2 Transient Response

The simulated transient step response, with rise and fall times, is depicted in Fig. 48.

Figure 48: Simulated transient response of dynamic buck converter, demonstrating (a) rise time $t_r = 33.1 \mu s$ and (b) fall time $t_f = 272.3 \mu s$. 
4.4.3 Frequency Response

Fig. 49 shows the simulated magnitude and phase response, as well as the effect of modulation frequency on efficiency.

![Simulation plots showing frequency response](image)

Figure 49: Simulated frequency response of dynamic buck converter, $h = 1$.

4.4.4 Modulation Index $h < 1$

The simulated effect of reducing modulation index from $h = 1$ to $h = \frac{1}{2}$ is shown in Fig. 50. This reduces both attenuation and distortion, such that nonlinearities in $v_O$ which appear at $f_m$ when $h = 1$ do not appear until $2f_s$ when $h = \frac{1}{2}$. 
Figure 50: Simulated input $v_{R E F}$ and output $v_O$ of dynamic buck converter with reduced modulation index $h = 0.5$, for (a) $f_m = 100$ Hz, (b) $f_m = 2$ kHz, and (c) $f_m = 20$ kHz.
### 4.5 Experimental Measurement of AC Characteristics

The procedure for obtaining ac performance measurements from the actual circuit is largely identical to the simulated approach, and utilizes the same prototype hardware as with the dc test. However, instead of using a non-ideal ramp comparator to generate $v_{PWM}$, the external pulse modulation function on the Agilent 33220A waveform generator is utilized to supply $v_{PWM}$ to the gate driver IC. This allows the waveform generator to act as both $v_{ramp}$ and the comparator, while a 10-Vpp sinusoidal $v_{REF}$ of frequency $f_m$ is supplied externally from a Hewlett-Packard 33120A function generator. The internal-external PWM synthesis approach provides the best practical equivalent of the ideal PWM generator used in simulation. The modulation reference signal $v_{REF}$ can therefore simply be set to a 100-Hz square wave function in order to measure transient response. Otherwise, all test circuit connections remain similar to the dc test measurements. A diagram indicating signal connections and measurement points is shown in Fig. 51.

![Figure 51: Test and measurement setup for ac characterization of dynamic buck converter design.](image-url)
4.5.1 Measured Large-Signal Output Response

Figure 52: Measured input $v_{REF}$ (lower) and output $v_O$ (upper) waveforms of dynamic buck converter, $h = 1$, for (a) $f_m = 100$ Hz, (b) $f_m = 1$ kHz, (c) $f_m = 10$ kHz.
4.5.2 Measured Transient Response

Figure 53: Measured transient response of dynamic buck converter, demonstrating (a) rise time $t_r = 38 \mu s$ and (b) fall time $t_f = 290 \mu s$. 
4.5.3 Measured Frequency Response

Figure 54: Measured frequency response of dynamic buck converter, $h = 1$. 
4.5.4 Measured Large-Signal Response: Modulation Index $h < 1$

Figure 55: Measured input $v_{REF}$ (lower) and output $v_O$ (upper) waveforms with reduced modulation index $h = 0.5$, for (a) $f_m = 100$ Hz, (b) $f_m = 2$ kHz, and (c) $f_m = 20$ kHz.
Figure 56: Measured frequency response of dynamic buck converter, $h = 0.5$.

4.5.5 Measured Modulated Power and Average Modulated Efficiency

Coherent instantaneous input modulation power waveforms are not available in simulation due to the lack of a graphical waveform averaging function in the Cosmoscope viewer. However, the critical comparison of $P_o(t)$ and $P_i(t)$ is easily viewed experimentally using the scope’s channel multiplication function. Input and output power at $f_s = 50$ Hz is shown in Fig. 57.
Figure 57: Measured modulated (a) input power $P_i$ and (b) output power $P_o$ waveforms of dynamic buck converter, $f_m = 50$ Hz, $h = 1$.

The concept of power-on-demand is illustrated in Fig. 58 by superimposing both waveforms in Fig. 57. The input power follows the contour of the output power, demonstrating that the dynamic converter only performs work when needed. Modulation efficiency $\eta_M$ therefore remains high at all levels of dynamic output voltage, despite total efficiency $\eta$ being directly proportional to $V_O$ for dc operation. The area underneath the curve of $P_i$, but above $P_o$, represents the total power losses of the buck converter. The smaller this region is, the higher the average modulation efficiency.
Figure 58: Composite overlay of measured $P_i$ and $P_o$ waveforms for $f_m = 50$ Hz, $h = 1$, demonstrating $\eta_m = \frac{P_{o(\text{AV})}}{P_{i(\text{AV})}} = 0.912$.

The effect of increasing $f_m$ can be seen in Fig. 59. The area between the two waveforms also visibly increases with $f_m$, and efficiency is reduced. Note also that in Fig. 59c a portion of $P_o$ is greater than $P_i$; this represents the discrete times where $\eta_m(t) > 1$. This area is effectively subtracted from the larger “loss region” when determining total losses and time-averaged efficiency.
Figure 59: Measured $P_i$ and $P_o$ waveforms for (a) $f_m = 100$ Hz, (b) $f_m = 1$ kHz, and (c) $f_m = 10$ kHz.

However, modulation efficiency does not approach zero as $f_m$ continues to increase.
At frequencies well above $f_{0m}$, the output voltage $v_O$ and current $i_O$ trend toward purely dc values, and $P_i$ and $P_o$ also approach purely dc power as seen in Fig. 60. Although this effectively increases efficiency, it is somewhat of a moot point as the dynamic buck converter has effectively ceased modulating.

![Figure 60: Measured $P_i$ and $P_o$ waveforms for $f_m = 100$ kHz, showing modulated power approaching dc.](image)

Fig. 61 shows the effect of reduced modulation index on the modulated power waveforms and average efficiency. The trend is the same as with Figs. 59 and 60, although baseline $\eta_M$ is slightly lower.
Figure 61: Measured $P_i$ and $P_o$ waveforms with reduced modulation index $h = 0.5$, for (a) $f_m = 100$ Hz, (b) $f_m = 1$ kHz, and (c) $f_m = 10$ kHz.
4.6 Results

The measured results are in overall good agreement with the simulations, in that the same general trends are observed in all scenarios. The following insights about ac operation are therefore gained.

**Large Signal and Transient Response, \( h = 1 \)** At modulation frequency \( f_m \approx 750 \) Hz, distortion appears on the lower half of the output sine wave. As \( f_m \) is increased further, this harmonic distortion results in a nearly triangular waveform. At around the same point, the magnitude of \( v_O \) begins to decrease, although not evenly about \( V_{ODC_{nom}} = 13 \) V but, rather, in a truncated fashion from the bottom up. This indicates the converter cannot drive the output voltage low fast enough or far enough beyond a certain modulation frequency. This is confirmed by the falling edge step response in Figs. 48 and 53; \( t_f \approx 280 \) \( \mu \)s in both cases, indicating an approximate 3-dB bandwidth of

\[
BW \approx \frac{0.35}{t_f} = \frac{0.35}{280 \mu s} = 1.25 \text{kHz}.
\]  

(192)

Similar phenomena are observed, for example, when the slew rate of an op-amp is exceeded [ ] . This may point to limitations of the switch or inductor in providing sufficient instantaneous current to meet the demands of a faster, steeper shift in \( I_L \) and therefore \( v_O(t) \). The combined effects of lowpass filtering and slew rate would lend themselves to explaining the observed phenomenon that the dc component of \( v_O \) does not remain constant at 13 V, but rather increases, approaching \( V_{O_{max}} \) as \( f_m \) is increased. This stands to reason given that the buck converter topology does the most work when driving dc output \( V_O \) lower, i.e., away from the fixed supply level \( V_I \), as demonstrated by the dc analysis in Chapter 2.
**Frequency Response**  The variable-output buck converter exhibits magnitude characteristics similar to that of a lowpass filter, which is predicted by the cutoff frequency $f_0$ introduced by the $LC$ filter. However, the actual cutoff frequency $f_{0m}$ appears to be an order of magnitude lower, as shown in (180). Therefore

$$\frac{f_{0m}}{f_0} = \frac{1.25 \text{ kHz}}{14.339 \text{ kHz}} = 0.0872$$

(193)

i.e.,

$$f_{0m} : f_0 \cong 1 : 11.5.$$  \hspace{1cm} (194)

Similarly, with respect to switching frequency,

$$f_{0m} : f_s = 1 : 800$$  \hspace{1cm} (195)

which is revealing from a design perspective since $f_s$ must be chosen prior to dc design of the converter. It should be noted, however, that although the magnitude resembles a lowpass filter, significant harmonic distortion begins to appear at frequencies slightly lower than the cutoff.

Modulation efficiency is also observed to be dependent upon $f_m$; from Fig. 54 it can be seen that $\eta_M$ is highest, and relatively constant, within the passband. This efficiency is

$$\eta_M(BW) \cong \eta_{Mmax}$$

(196)

and is on the order of 91% for the actual circuit.

**Modulation Index**  No significant change in phase response is observed when modulation index $h$ is decreased; however, modulation frequency-dependent distortion and attenuation are effectively reduced. This is shown via both simulation and measurement. Figs. 50, 55, and 56 demonstrate that, when $h$ is reduced by half, the same
harmonic distortion and attenuation in $v_O$ previously seen at $f_m = (1 \text{ kHz}, 10 \text{ kHz})$ are now seen at $f_m = (2 \text{ kHz}, 20 \text{ kHz})$. The measured bode plot likewise shows that $f_{0m} \bigg|_{h=0.5}$ has increased to approximately 2 kHz. It can therefore be stated that

$$f_{0m} \propto \frac{1}{h} \quad (197)$$

and more specifically in this case

$$f_{0m} \approx \frac{1}{h} \left( f_{0m} \bigg|_{h=1} \right). \quad (198)$$

Fig. 56 also demonstrates that efficiency is slightly lower within the modulation passband when $h$ is reduced, implying

$$\eta_M \propto h \quad (199)$$

and, by extension,

$$f_{0m} \propto \frac{1}{\eta_M}. \quad (200)$$

**Modulation Power Waveforms** The experimental observations of instantaneous modulation power $P_i(t)$ and $P_o(t)$ demonstrate that, within the bandwidth $f_{0m}$, the circuit achieves its key goal of providing power on-demand in order to maximize efficiency. Within the passband, measured efficiency is on the order of 91%. The waveforms in Figs. 58, 59, and 61 illustrate not only the relationship of instantaneous output power to input power, but also the degradation of this ratio as modulation frequency increases.
5 Practical Design Considerations

The implementation of a dynamic buck converter power stage circuit presents a number of challenges at the practical level, despite topological simplicity. This chapter gives an overview of three key difficulties faced in fabricating a working test circuit from the design in Chapter 2. Such challenges include

- selection of a suitable power switch;
- devising a means of driving the gate of the switch;
- designing a printed circuit board upon which to mount discrete components.

Potential solutions to these problems are discussed within the context of the actual hardware constructed.

5.1 Power Switches for Dynamic Buck Converters

Multiple preliminary simulation attempts have shown that high switching frequencies are essential for modulation bandwidth and fidelity. Therefore, power transistors that operate well as a switch under high-speed, hard-switching conditions are the best candidates. These devices must also have low $C_{oss}$ and $r_{DS(ON)}$ to keep switching and conduction losses low. Of the four discrete components of the dynamic buck power stage, the switch is the most critical in terms of efficiency, speed, and overall modulation performance.
5.1.1 MOSFETs

Silicon and SiC RF power MOSFETs are desirable in that they are a robust, established technologies with a wide range of commercially-available specifications, packaging, and design tools. The majority of these are also enhancement-type devices, which are far easier to drive at floating $v_{GS}$ than depletion-type transistors. However, they generally also exhibit larger $C_{oss}$ which can limit efficiency and switching speed. Fig. 62 shows an example of this technology. For the purposes of this work, driving the switch proved to be a considerable challenge, and so ultimately a low-$C_{oss}$ Si RF power MOSFET was selected due to its enhancement-type properties.

![Figure 62: VRF148A Si RF power MOSFET, $r_{DS(on)} \approx 4 \Omega$, $C_{oss} = 40 \text{ pF}$, M113 direct-mount package.](image)

5.1.2 GaN HEMTs

The gallium nitride (GaN) high-electron-mobility transistor (HEMT) is an emergent technology which has demonstrated superior performance in RFPAs and other high-speed power applications [13, 19, 24, 72]. These devices are attractive for use in the proposed application due to their bandwidth ($> 10$ GHz capable) and low output capacitance ($C_{oss} \leq 5 \text{ pF}$). However, HEMTs are also depletion-type transistors; in order to take advantage of their capabilities in a buck converter, they must be driven...
at high-speed with a floating negative bias, which is a nontrivial undertaking.

A small product line of enhancement-type GaN-on-Si (“eGaN”) FETs are currently offered which boast some of the benefits of GaN HEMTs but with far easier driving requirements. According to the manufacturer, these devices have been produced specifically for high-speed, hard-switching applications, initially making them the most promising candidate for this work. An example of this type of device is seen in Fig. 63, and highlights a key drawback.

![Figure 63: EPC2012 GaN-on-Si “eGaN” FET, $r_{DS(on)} = 100 \, \text{m\Omega}$, $C_{oss} = 73 \, \text{pF}$, die-packaged.](image)

These transistors are currently available only in surface-mount die packaging, making prototype testing difficult, costly, and time-consuming. Beyond obvious mounting challenges, the complex issue of external heat-sinking is introduced. The EPC2012 eGaN FET was initially selected as the switching device for this work; and although technically beyond the scope of this work, several attempts at proper mounting and heat sinking were made with poor results. Furthermore, simulation ultimately showed no inherent speed benefits over a comparable, prepackaged RF power MOSFET, as can be seen in Fig. 64 when switching at a modest $f_s = 10 \, \text{MHz}$.
Figure 64: Comparison of $v_{DS}$ between EPC2012 GaN-on-Si and VRF148A Si power FETs, $f_s = 10$ MHz.

5.2 Driving the Switch

Switch-mode power converters must have a means of driving the gate-to-source voltage of the switch at a desired speed and with sufficient current. Additionally, the asynchronous buck converter topology requires this PWM voltage to be floating between two hot points; that is, not referenced to ground. This “high-side” driving configuration forms a nontrivial challenge from the perspective of fabricating a working test circuit for the dynamic power stage. Regardless of the speed capabilities of the switch, actual performance is limited by the ability to deliver a high-quality PWM signal between the floating gate and source. This renders the driver as critical as the switch itself, in terms of design and overall performance of the power stage. Two driver solutions, one discrete and one IC-based, are examined in the course of this work.
5.2.1 Transformer-coupled Charge Pump

A discrete component high-side driver may be implemented using a small signal transformer to isolate $v_{PWM}$ and a diode-capacitor charge pump to provide gate drive current. An example is shown in Fig. 65.

![Diagram of Transformer-coupled high-side driver with charge pump.](image)

Figure 65: Transformer-coupled high-side driver with charge pump.

The T-1062SCT coupling transformer is used due to high bandwidth, low output capacitance, and a small footprint. Using a waveform generator to provide $v_{PWM}$ at $f_s = 2$ MHz and $0.2 \leq D \leq 0.8$, the measured no-load output $v_{GS}$ is seen in Fig. 66; however, when connected to the power stage, drive current is insufficient and the switch fails to turn ON.
This approach was deemed insufficient for this work, and efforts are instead directed towards an IC driver solution.
5.2.2 Integrated Circuit Solutions

A number of dedicated ICs are commercially available for driving the gate of high-side switches in PWM converters. These are low-profile, monolithic devices that require a nominal dc supply voltage $+V_{CC}$ and two or three support components. Three ICs are examined for use in this work, and are presented in Table 4.

Table 4

<table>
<thead>
<tr>
<th>IC</th>
<th>$t_r$, $t_f$</th>
<th>$I_{\text{drive}}$ (peak)</th>
<th>$V_{CC}$</th>
<th>Additional components required</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM5113</td>
<td>7 ns</td>
<td>1.5 A</td>
<td>$+5,\text{V}$</td>
<td>bootstrap cap, 0.1-$\mu\text{F}$ bypass cap</td>
</tr>
<tr>
<td>EL7158</td>
<td>8 ns</td>
<td>12 A</td>
<td>$+5,\text{V}$</td>
<td>bypass cap</td>
</tr>
<tr>
<td>LTC4440-5</td>
<td>8 ns</td>
<td>1.1 A</td>
<td>$+5,\text{V}$</td>
<td>bootstrap diode &amp; cap, bypass cap</td>
</tr>
</tbody>
</table>

All ICs are comparable in terms of speed, and all possess sufficient peak drive current capability. The LTC4440-5 is therefore selected due to extensive application documentation and manufacturer-provided simulation tools. Having first confirmed operation in simulation, the IC is mounted to a prototype PCB as seen in Fig. 67.

Figure 67: Prototype mounting for LTC4440-5 high-side gate driver.
The complete driver subcircuit with external components is shown in Fig. 68. The floating output, loaded by the VRF148A switch, is then measured at \( f_s = 2 \, \text{MHz} \); Fig. 69 shows loaded performance of the LTC4440-5 to be superior to that of the unloaded transformer-coupled charge pump.

Figure 68: Schematic of driver subcircuit for power stage.
Figure 69: Loaded output $v_{GS}$ of LTC4440-5-based driver subcircuit, $f_s = 2$ MHz, for (a) $D = 0.8$, (b) $D = 0.5$, and (c) $D = 0.2$. 
5.3 PCB Layout

The printed circuit board shown in Fig. 70 is used to mount the power stage and driver components. Standard design practices for hard-switching PCBs are adopted, such as short-and-wide traces and a large ground plane on the reverse side of the board. However, as a test circuit, it is also necessary to incorporate test access points and extra component real estate into a single PCB design. These are incorporated as shown to allow for voltage and current probe access, and also for expansion of the original asynchronous design to a synchronous variant with two VRF148A switches.

![Prototype dynamic buck converter](image)

Figure 70: Prototype dynamic buck converter (a) layout and (b) completed test PCB.
6 Conclusions and Future Work

6.1 Summary

This work has presented previously-unpublished insight into the analysis, design, and performance of a PWM dc-dc buck converter operated as a dynamic power supply. New dc analysis has been provided for the buck converter operating under the conditions of fixed $V_I$, fixed $R_L$, and variable $(D, V_O)$. Theory is presented for mathematically determining key dc parameters such as the CCM-DCM operating boundary, $\Delta i_L$, $I_{SM \text{max}}$, $V_r$, $P_{SW}$, $\eta$, and device stresses for fixed-$V_I$, variable-$V_O$ operation. A new design procedure is derived for selecting components $L$, $C$, and switching devices $S_1$ and $D_1$. The new dc analysis and design procedure are demonstrated to be in good agreement with measured dc performance of a variable-output voltage buck converter built with discrete components.

Open-loop ac characteristics of the dynamic-output buck converter, such as large signal and transient response, gain, phase, modulation index, and $\eta_M$ have been obtained via simulation and experimental measurements. The simulation results and measurements have been demonstrated to be in good agreement. The ac characterization has shown that the dynamic buck converter exhibits an approximate lowpass response with cutoff frequency $f_{0m}$, and produces undistorted, highly-efficient modulated output $v_O$ within this bandwidth. It has also been demonstrated that the effective bandwidth can be increased by reducing the modulation index, albeit at the cost of efficiency. The ratio of $f_s : f_{0m}$ required for undistorted output is shown to be on the order of $10^3$. Measurement of modulated ac power demonstrates that the dynamic PWM buck converter can operate with over 91% efficiency by providing
power-on-demand.

Practical design considerations for the power stage have been discussed, namely the difficulties inherent with matching a high-speed switch to a suitable high-speed, high-side gate driver, in order to maximize $f_s$. An overview of different switches and drivers has been presented, along with a brief discussion of the PCB designed for testing a dynamic buck converter.

As a feasibility study and proof-of-concept, this work has shown the proposed circuit to be a good candidate for the power stage of a dynamic supply in terms of efficiency. However, in the absence of considerably faster switches and similarly-capable high-side gate driver ICs, modulation bandwidth remains limited.

6.2 Contributions

The specific contributions of this work are:

- New circuit analysis characterizing the dc operation of a PWM dc-dc buck converter operated with fixed $V_I$, fixed $R_L$, and variable $V_O$.

- New equations for peak-to-peak inductor current $\Delta i_L$, peak-to-peak ripple voltage $V_r$, peak switch current $I_{SM_{\text{max}}}$, switching loss $P_{SW}$, total efficiency $\eta$, and minimum inductor and capacitor design values $L_{\text{min}}$ and $C_{\text{min}}$.

- Step-by-step design procedure for selecting switch, diode, inductor, and capacitor of variable-output voltage buck converter.

- Simulated and measured quantification of ac characteristics of dynamic buck converter, including transient response, frequency response, and modulation efficiency.
6.3 Future Work

Further topics of study related to this work may include:

- Further investigation into the drain-to-source rise-time behavior of the switching device at low \( D \), with the aim of linearizing the dc transfer characteristic \( V_O(D) \).

- Simulated dc and ac characterization of dynamic buck converter design with switching devices not available for experimental measurement in this work, such as high-speed depletion-type GaN devices.

- Experimental comparison between Si, SiC, and eGaN enhancement-type devices used as a switch for the power stage.

- Experimental measurement of ac characteristics at much higher switching frequencies, when and if suitable switch and drivers are made available.

- DC analysis and/or ac characterization of variable-output voltage PWM buck converter utilizing the synchronous topology.

- Investigation into applicability of existing small-signal ac models to the large-signal characteristics of modulated-output dynamic buck converter.

6.4 Publications


References


[34] A. Bracke, L. Rathgeber, F. Siegert, S. Heck, and M. Berroth, “Power supply modulation for RF applications,” 15th International Power Electronics and Motion Control Conference (EPE/PEMC), 4-6 Sept. 2012, pp. LS8d.3-1 - LS8d.3-5.


