10-bit C2C DAC Design in 65nm CMOS Technology

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10-BIT C2C DAC DESIGN IN 65nm CMOS TECHNOLOGY

A Thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering

by

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B.TECH., Koneru Lakshmaiah University, GUNTUR, 2017

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ABSTRACT

Kommareddy, Jeevani. M.S.E.E., Department of Electrical Engineering, Wright State University, 2019. 10-bit C2C DAC design in 65nm CMOS technology.

Many wired and wireless communication systems require high-speed and high-performance data converters. These data converters act as bridge between digital signal processing blocks and power amplifiers. However, these data converters have been the bottleneck in the communication systems. This thesis presents the design of a 10-bit C2C digital to analog converter (DAC) for high resolution, wide bandwidth and low power consumption applications. The DAC is implemented in CMOS 65nm technology. The SFDR of this C2C DAC is 71.95dB at 500MHz input frequency and consumes 88.14\(\mu W\) of power with ENOB as 11.65 with 1.0GHz sample frequency with 0.31LSB of INL and 0.5LSB of DNL. A 10-bit SAR ADC is designed using this proposed C2C DAC with 427.4\(\mu W\) of power consumption at 1.0V voltage supply.
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1. Introduction

1.1 Motivation

Rising demand of bandwidth due to increasing on-chip processing speed and logic density have pushed serial input/output (I/O) data rates beyond 10Gbits/second (Gb/s). Analog-to-digital converter (ADC) based receivers with digital signal processing (DSP) have become popular [1]. Along with ADCs digital-to-analog converters (DAC) are also in high demand. DACs convert discrete digital signals into continuous analog signals. Among all the DAC architectures Capacitive DACs are preferred because of their reduced design complexity, optimized power and improved matching. Exclusively for medium to high resolution applications capacitive DACs are chosen over resistive and current steering DACs. Even though the Capacitive DAC based solution provides many benefits, it still faces a bottleneck in sizing the capacitors, capacitor mismatch and parasitic capacitance degrading the DAC performance. With technology scaling, digital solutions will also provide better portability between IC fabrication technologies and flexibility, and ultimately result in lower power and cost.
Therefore, this thesis will target the implementation of such a capacitive DAC using the optimized structure in 65nm CMOS technology. The target application here is using this capacitive DAC in implementing SAR ADC.

1.2 Objective of Thesis

The goal of this thesis is to design a low power 10-bit Capacitive DAC using less capacitance and high switching speed in CMOS 65nm technology. This DAC should be able to drive 10-bit SAR Logic in SAR ADC operating at high frequency.

To achieve this goal did research on 65nm CMOS Technology specifications and many reference DAC structures were studied and implemented and tested with the SAR ADC circuit.

1.3 Thesis Organization

Rest of the thesis is organised into four chapters. DAC overview and related architectures were stated in Chapter 2. Optimized C2C DAC design and SAR ADC designs are presented in the Chapter 3. Test setup and performance measurement results for both DAC and SAR ADC are given in Chapter 4. Conclusion and future scope are given in Chapter 5.
2. Background

2.1 DAC Overview

Signal processing is universally used in various fields, such as audio, controls, communication and medical systems. It deals with both analog signals and digital signals by using data converters. Data converters serves as interface between the analog and digital world [2].

As shown in the Figure 1 analog input signal is passed through low pass filter to remove the high frequency components in order to avoid aliasing. Then the signal is converted to discrete sampled data at sampling frequency $f_s$, and the sampled data is quantized using the analog-to-digital converter (ADC). Digital outputs from ADC are processed through the digital signal processor (DSP). Finally, it is converted to analog signal by using digital-
to-analog converter (DAC). Then the analog signal is passed through reconstruction filter to smoothen the signal.

This chapter focuses on the basic principles of DAC. Basic requirements to design DAC resolution and quantization errors are explained. Static and dynamic performance metrics of DAC are introduced. An overview of different DAC architectures is also presented. Based on speed, power resolution and area comparison between popular architectures is given at the end of this chapter.

### 2.2 Basic concepts of DAC

Figure shows the black box of N-bit resolution DAC. DAC converts digital binary word into analog signals. As shown in the Figure 2 Vref is the reference voltage of the DAC and b_{N-1} to b_0 are the digital input bits. For each binary word a corresponding analog voltage exists. That analog output voltage of the DAC is given by

\[
V_{out} = V_{ref} \left( \frac{D}{2^N} \right)
\]

Eq (2.1)
where N is the resolution of the DAC, D is the binary word input given to the DAC and it can be characterized as

\[ D = \sum_{n=0}^{N-1} 2^n(b_n) \]  

**Eq (2.2)**

Where \( n \) is the index of the binary word and \( b \) is the digital bit ‘1’ or ‘0’ value at the respective index.

### 2.2.1 Smallest output step size (\( V_{LSB} \))

Generally, least significant bit (LSB) is the zeroth bit (\( b_0 \)) in digital word. But in data converters, one LSB is referred as minimum step size of the analog output. LSB can be written as

\[ LSB = \frac{V_{FS}}{2^N} \]  

**Eq (2.3)**
Where \( N \) is the DAC resolution and \( V_{FS} \) is the full-scale range voltage. Full scale range is defined as the difference between maximum output voltage to the minimum output voltage. Where minimum output voltage is referred as digital word consisting of all ‘0’, the maximum analog output voltage is one LSB less than \( V_{ref} \). The full-scale voltage \( V_{FS} \) can be defined as

\[
V_{FS} = \left( \frac{2^N - 1}{2^N} \right) V_{ref} \quad \text{Eq (2.4)}
\]

### 2.3 DAC Architectures

Plenty of architectures are used to convert digital word bits to analog signals. Based on the application requirements of data converter DAC architecture is chosen. Requirements such as accuracy, power, area, bandwidth must be taken into consideration. Some DAC architectures are simple and are designed using few switches and resistors. But these DAC architectures have limitations in terms of speed, resolution and mismatch error. It’s hard to design a high-resolution DAC which is operating at high frequencies [2].

Data converters are categorized into Nyquist rate converters and over sampling converters based on bandwidth and sampling condition. The Nyquist rate DACs operates in between DC and Nyquist rate frequency. To make the converter operating at Nyquist rate frequency anti-aliasing filters must be used which is difficult to design. But Over sampling DACs operates at fraction of the sampling frequency. Hence building a reconstruction filter will be essay.
The main logic in every DAC architecture is dividing a reference voltage and generating corresponding analog output voltage. The reference voltage is divided into smaller currents or voltage levels by using resistor networks. Capacitor network store charge from the reference voltage and discharge it to the output. Transistor current sources can also be used to generate analog output voltages by creating output currents.

### 2.3.1 Resistor String DAC

An easy way of DAC architecture is the resistor string [3] as shown in *Figure 3*. Using $2^N$ resistors in series, resistor DAC can be designed, each resistor in the series corresponding to one LSB. To one end of the resister series, a voltage reference is connected and the other is connected to ground. Each resistor is followed by a switch. And the output of each switch is combined to obtain the DAC output. The switches in the resistor string can either be enabled or disabled using the output signal from the $2^N: N$ encoder. The voltage division of reference occurs when the switches were enabled and produces an analog output.
Advantages of this resistor string DAC are it is simple and guaranteed to be monotonic. Large number of resistors were required to obtain higher resolution which is the disadvantage of the resistor string DAC. Using the large number of resistors requires large amount in area and it is difficult to use identical resistors which leads to linearity errors. With increase in the resolution, large number of resistors were connected to output in parallel where parasitic capacitance restricts the speed of the converter.
2.3.2 Binary Weighted Resistor Ladder DAC

Using a resistor ladder network which contains $N$ resistors, the binary weighted resistor ladder DAC can be designed. The resistance value of each resistor in the resistor ladder is a multiple of 2 with each descending bit, which starts from the MSB resistor whose resistance $R$ which is shown in the below Figure 4[3].

![Figure 4 Binary Weighted Resistor Ladder DAC](image)

The reference voltage is divided into different voltage levels based on the binary weighted resistor network and are connected to switches. Based on digital input bits these switches control the voltage levels. An operational amplifier is connected to the output of the switches. Current flows through the resistors to the ground or to the virtual ground in the operational amplifier when a reference voltage is connected to the resistor ladder which forms the output at op amp. The disadvantage of this architecture is the difference in the
resistor value becomes large with the higher resolution designs. Matching of the resistors becomes difficult during process variation in fabrication.

\subsection{R-2R DAC}

The R-2R DAC is modification to the binary weighted resistor ladder DAC architecture where resistors are used with only two resistance values. The resister ladder in R-2R DAC is designed by connecting resistors in series with resistance value $R$, then rungs of resistors of value of $2R$ [3]. The R-2R can be described as in current mode or voltage mode depending on the reference voltage. Switches operated in between $V_{\text{ref}}$ and ground in voltage mode and the switches operate in between output and ground in current mode shown in below Figure 5 [3], where the ladder resister is connected to reference voltage.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure5.png}
\caption{R-2R DAC}
\end{figure}
The advantage of R-2R DAC is, it only requires resistors with only two resistance values and number of resistors are 2N. Due to the 2R equivalent resistance of the ladder rung on each side, the output impedance is always constant for this design. To increase the linearity of this design, current source transistors are used in conjunction with resistor ladder network. To switch the reference voltage in between ground and virtual ground, an operational amplifier must be used. With the use of op amp output buffer, it limits the bandwidth and linearity errors will be occurred. Switches operate in between ground and \( V_{\text{ref}} \) in voltage mode, which is difficult to design. Since the switches are directly connected to output node, glitches will occur in current mode.

2.3.4 Current Steering DACs

For the high bandwidth converters, current steering DAC is the suitable architecture which is shown in the Figure 6 [3]. The working of the current steering DAC is to add the currents which are produced by an array of current sources. Supply voltage is connected to one end and to the other end (output end) a load resistor is connected. Current flows through the load resistor when the current source is enabled. The current is converted into voltage, when the current is synced by the current source. The voltage division is formed in between the power supply connected to resistor and the voltage drop by the current from current sources. This forms the output voltage. High performance can be achieved because no op amp is used.
The disadvantage of this design is, it produces a large glitch at output when multiple current sources are being switched at same time. With increase in the number of bits, the requirement of current sources also increases, which leads to high power consumption. A large amount of parasitic capacitance is introduced, which limits the speed of the converter.

Figure 6 Current Steering DAC architecture
2.3.5 Charge Scaling DACs

Replace the resistors with capacitors in resistor-based architecture, it is charge scaling DAC. This charge scaling DAC can be designed using either C-2C network or binary weighted architecture as shown in Figure 7 [4]. In charge scaling DAC an additional reset switch is used to discharge all capacitors with every conversion.

Because of its fast, accurate and essay implementation in CMOS most of the SAR ADCs uses charge scaling converters [4]. The disadvantage of this architecture is it requires the op amp. Due to parasitic capacitance op amp is required to avoid the non-linearity in the output of the DAC. This design also suffers from charge feed through errors. But due to technology scaling charge scaling DAC are giving high performance compared to other DAC structures.
2.4 Comparison

All the popular DAC structures were discussed in the above section. Among all those structures best architecture is chosen based on application. In this thesis main objective is to design a low power consumption DAC which is suitable to design low power 10-bit SAR ADC. For some applications, almost all the architectures may work well; for others, there may be a better choice to achieve the best performance. For example, the problem in using the resistive DAC for SAR ADC implementation is the switching speed and the non-linearity. And the disadvantage with current steering DAC is it produces more glitches in the output if the multiple current sources are switched at the same time. The problem with DAC using capacitors is that leakage causes it to lose its accuracy within a few milliseconds of being set. This makes capacitive DACs unsuitable for general purpose of DAC applications, but for SAR ADCs it is not a problem. Because the conversion is completed in few us or less i.e; even before the leakage starts.

Also, the development in sub-micron CMOS technology made possible of very small, cost effective and very accurate switched capacitor DACs which makes the capacitor DACs superior to resistive DACs. The advantage of C2C architecture over binary weighted capacitive DAC is the total capacitance value of the entire circuit. C2C DAC will have only two capacitor values i.e; C and 2C for N bit resolution but binary weighted capacitive DAC capacitance values depends upon the resolution.
Hence in this thesis a 10-bit C2C DAC structure with optimized switch circuit is presented which can be used in implementing 10-bit SAR ADC in 65nm CMOS technology.

2.5 Performance Metrics

DAC performance can be measured in terms of static performance and dynamic performance. Dynamic performance of DAC is given higher priority to assess the performance and to check the reliability of DAC. It is measured by passing the digital inputs to DAC which were generated by an analog to digital converter whose input is sinusoidal wave form. Now FFT analysis is done on the reconstructed sinusoidal output waveform from the DAC to see how the designed digital to analog converter performs. However, the accuracy of converter output with respect to the expected output is analyzed by static performance metrics. Generally, the input is selected in such a way that it has the full range of binary codes so that the digital analog converter output looks like staircase plot. The accuracy is determined by measuring the voltage at each level of code. By measuring the performance using dynamic performance metrics we can have a good insight on how accurate the DAC is once the output gets settled.
2.5.1 Static Linearity

Differential nonlinearity (DNL), and the integral nonlinearity (INL) are two main static performance metrics. The difference between the output levels of two adjacent codes gives the differential nonlinearity of the DAC. The DNL is measured in terms of LSB, in ideal case the difference between two codes will be 1 LSB. In order to bail that the output is monotonically increasing, the DNL should never be greater than 1LSB [3]. If two adjacent codes step size is 1.25LSB instead of 1LSB, then the DNL is said to be 0.25LSB. The DNL must be between $\pm \frac{1}{2}$ LSB to maintain ample accuracy. The disturbance in accuracy occurs due to Non-monotonic behavior of the DAC. Few design methods were proposed to guarantee the monotonicity behavior of DAC.

Integral nonlinearity is the difference of the ideal output voltage level and the output voltage level. One way to measure is giving the input in such a way that it has the full range of binary codes so that the digital analog converter output looks like staircase plot. And the deviation from this staircase plot is the integral nonlinearity. Figure 8 shows an example of the DNL and INL errors of a non-ideal 3-bit ADC.
As shown in Figure 8 the code width is 0.5LSB longer than the ideal one at code 2 (010₂), so the corresponding DNL error is +1.5LSB. While at code 5 (101₂), the DNL error becomes -0.5LSB and INL is -0.5LSB.

Offset and gain errors also cause the linearity issues to digital to analog converters. Offset error is the difference between the first code transition point and the ideal one. Full-scale gain error is the difference between the last code transition point and the ideal one. Full-
scale gain error doesn’t cause any effect on the performance of the digital to analog converter but will cause distortions in the output waveform.

2.5.2 Dynamic Performance

The data converters performance is assessed better with dynamic performance metrics. Which will help the data converters, as best fit in the real-world applications. Dynamic performance is measured by giving the full-scale range sinusoidal with single set frequency as input to the data converters.

2.5.2.1 Signal to Noise Ratio

Signal to Noise Ratio (SNR) is defined as the ratio of spectral power of the input to the noise power. As shown in the Eq (2.6) SNR is determined by the ratio of a root mean square (RMS) of full-scale input to its RMS quantization error.

Where RMS quantization error can be given by Eq (2.5)

\[
Q_{RMS} = \frac{V_{LSB}}{\sqrt{12}} \quad \text{Eq (2.5)}
\]

\[
SNR_{dB} = \frac{2^N(V_{LSB})}{2^{N/2} V_{LSB}} \quad \text{Eq (2.6)}
\]

The input signal must be at full scale in order to measure the SNR. Smaller amplitude will reduce the SNR, which is intuitive since the signal to noise ratio is directly proportional to the input signal power. In the ideal case, the noise floor would only consist of the
quantization noise produced by the converter. In practical converters, errors from linearity, glitches, clock skew, and output settling time will increase the noise floor [3].

By simplifying Eq (2.6) ideal SNR for N-bit data converter is given as

\[ SNR = 6.02N + 1.76 \]  

Eq (2.7)

As shown in Eq (2.7) for each bit of resolution, SNR should provide a 6dB increment in SNR value.

### 2.5.2.2 Spurious Free Dynamic Range

Spurious Free Dynamic Range (SFDR) is considered as most important dynamic specification for data converters. It is measured by applying the dft to the output. It is the difference between the fundamental signal at input frequency to the second highest distorted component, which is known as spur. Figure 9 shows the SFDR measurement, fundamental signal and the noise floor.
2.5.2.3 Signal-to-Noise-and-Distortion Ratio (SINAD)

In an ideal ADC, Signal-to-noise-and-distortion ratio (SINAD) is the ratio of the input signal amplitude to the rms sum of all other spectral components (including not only random errors but also harmonic distortions). SINAD is represented as

\[ SINAD = 20 \log_{10} \left( \frac{A_{signal}}{A_{noise} + A_{Harmonic\,distortions}} \right) \]  

Eq (2.8)
2.5.2.4 Effective Number of bits

The Effective number of bits (ENOB) measures the reduced resolution of the DAC. Due to high frequencies the practical resolution of data converters degrades. As the DAC is non ideal the reduced resolution is caused due to the harmonics and distortion of the output signal. ENOB is calculated by replacing the SNR variable with SFDR value in the SNR equation. The real resolution of the output can be determined by Eq (2.9)

\[
\text{ENOB} = \frac{\text{SFDR(dB)} - 1.76\text{dB}}{6.02\text{dB}} \quad \text{Eq (2.9)}
\]
3. System Circuit and Design

This thesis mainly focusses on designing a low power and efficient DAC design which can be used as sub block in ADC. For DAC topology C2C architecture of 10bit resolution is chosen over binary-weighted architecture because of its remarkable speed and higher bandwidth, at a cost of distortions caused by parasitic capacitances.

3.1 Architecture of C2C DAC

Capacitor arrays are widely used for DAC design [1]. Among all the capacitive DAC architectures C2C DAC is preferred because of its small capacitance ratios, high conversion rate and low power consumption. The schematic of C2C DAC is shown in Figure 10. Digital inputs to DAC are controlled by 10-bit Successive Approximation Register (SAR). SAR digital bit outputs are fed to switches as shown in the Figure 10. DAC switches take the digital bits as inputs and switch the output voltage in between Vref and GND. Detailed explanation on DAC switch is given in section 3.1.1. Based on the digital bits output of DAC is calculated as

\[ V_{out}C_{total} = C_{effective} \times V_{ref} \times \left( \sum_{i=0}^{N-1} b_i 2^{-i} \right) \]

Eq (3.1)
Where $b_i$ is the digital input bits from SAR control logic. $C_{\text{total}}$ is the effective output capacitance of the entire C2C ladder network which is equal to $2C_u$ where $C_u$ is the unit capacitance. Total capacitance spread of the C2C 10-bit DAC is $29C_u$ which is drastically low compared to binary weighted capacitor array DAC which will have a total of $1024C_u$ capacitance. Now the novelty of the designed C2C DAC lies in selecting the unit capacitor value to achieve high performance with less parasitic capacitance effect.
Figure 10 C2C DAC architecture with DAC switches
The capacitance of unit capacitor (Cu) is chosen based on four aspects. They are capacitance mismatch, parasitic capacitances, thermal noise and input sampler band width. If input sampling switch and bandwidth were taken into consideration, then the unit capacitor should choose reasonably by keeping an upper bound on unit capacitance. But the linearity of DAC gets affected by capacitor mismatch. Mismatch gets worse if the unit capacitance gets smaller because capacitor mismatch is inversely proportional to square root of the capacitor area. Also, the ratio of parasitic capacitances to the real capacitance gets higher as the capacitance area gets decreased. Table 1 shows the parasitic capacitances for unit Metal insulator Metal (MIM) capacitors. And by choosing the lower capacitance value thermal noise gets increased. From thermal noise formula kT/C, it can be seen that thermal noise is inversely proportional to capacitance. Therefore, thermal noise, Capacitor mismatch, Parasitic capacitance ratio sets the lower bound for unit capacitance value.

Table 1: Parasitic capacitance for different MIM capacitance values

<table>
<thead>
<tr>
<th>Unit MIM Capacitor (fF)</th>
<th>20</th>
<th>40</th>
<th>80</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bottom plate parasitic capacitance (fF)</td>
<td>1.13</td>
<td>1.38</td>
<td>1.71</td>
</tr>
<tr>
<td>Top plate parasitic capacitance (fF)</td>
<td>0.48</td>
<td>0.64</td>
<td>0.93</td>
</tr>
</tbody>
</table>

Hence 40fF is chosen as unit capacitance Cu and 80fF as 2Cu to design C2C DAC architecture. From Table 1 it can be seen that bottom plate parasitic capacitance is almost 2 to 3 times to the top plate parasitic capacitance. Considering the effect of these parasitic
capacitances Cu is taken as 39.9771fF and 2Cu is taken as 80.0132fF in the schematic design. As the capacitor network works as voltage divider circuit. It converts the digital bit word to analog output voltages. This analog voltage is given as input to an operational amplifier to get stabilized output.

3.1.1 DAC Switch Design

As seen in Figure 10, digital inputs are the control terminals to the switches of a DAC. Switches are used to switch the output voltage in between Vdd and GND based on the digital bits. If the digital bit is ‘1’ then M1 and M2 transistors will be ON, transistors M3 and M4 will be OFF. This makes the switch output raise to Vdd. If the digital bit is ‘0’ then M3 and M4 transistors will be ON, transistors M1 and M2 will be OFF. This makes the switch output fall to ground voltage.

![Figure 11 Schematic of DAC_switch using 2 to 1 MUX](image)

Figure 11 Schematic of DAC_switch using 2 to 1 MUX
The logic of this switch is implemented using a 2 to 1 MUX as shown in the *Figure 11* with CMOS transmission gates. Due to switching activity nature, power consumed by switches takes a big portion of DAC power consumption. Optimized sizes are used to reduce the output current which is directly proportional to the power consumption. To implement a 2 to 1 MUX logic, digital bit is passed as select input and Vdd, GND as the actual inputs to the transmission gates. Optimized sizes were chosen for the CMOS transmission gates to get perfect Vdd and GND voltages as output without any distortion as shown in *Figure 12*. 
Figure 12 DAC switch output and control bit
3.1.2 Op Amp Design

Two stage op amp with miller compensation capacitor ($C_c$) and nulling resistor ($R_z$) is used in this DAC design to provide stability for the output DAC signal. NMOS differential pair is used for first stage followed by PMOS common source amplifier as shown in Figure 13 [7].

![Two stage Op-amp schematic](image-url)

*Figure 13 Two stage Op-amp schematic*
Design calculations of two stage op amp are described as per small signal analysis of the two-stage op amp:

Second stage output bias current can be determined by using relation between slew rate and load capacitor \( (C_L) \), which can be given as

\[
\text{slew rate} \leq \frac{I_7}{C_L} \quad \text{Eq}(3.1)
\]

\( I_7 \) is set to 7 µAmp to achieve 70V/µs with load of 100fF.

Similarly first stage output bias current is also estimated using Eq(3.1) with load capacitor as \( C_c \). Compensation capacitor can be calculated as

\[
C_c = 0.22 \times C_L \quad \text{Eq}(3.2)
\]

Transconductance for two stages can be determined using

\[
g_{m1} = GBW \times 2\pi \times C_c \quad \text{Eq}(3.3)
\]

\[
g_{m6} = 2.2GBW \times 2\pi \times C_L \quad \text{Eq}(3.4)
\]

The DC gain of two stage amplifier is calculated by multiplying individual stages DC gain. Individual stages DC gain is obtained by multiplying transconductance \( (g_m) \) and the output resistance \( (R_{out}) \). It can be given as

\[
A_{v0} = (g_{m1} \times R_{out1})(g_{m6} \times R_{out2}) \quad \text{Eq}(3.5)
\]

Output resistance of each stage is inversely proportional to output bias current and the channel length modulation \( (\lambda) \). Final equation for calculating DC gain is given in Eq(3.6)

\[
A_{v0} = \frac{g_{m1}g_{m6}}{2(\lambda_n+\lambda_p) \times I_7 \times I_5} \quad \text{Eq}(3.6)
\]
The sizes of M1, M6 transistors are determined by transconductance and current relation as shown in Eq(3.7).

\[ g_m = \sqrt{2\beta I} \quad \text{Eq}(3.7) \]

For calculating M1, \( I_1 \) is need which is equal to half of the \( I_5 \) bias current. Therefore width of M5 is double of M5. M6 size is also calculated with Eq(3.7) and \( I_6 \) is equal to \( I_7 \).

From current mirror circuit M4 and M6 transistors relation can be given as

\[ I_4 = (I_6) \left( \frac{w_4}{w_6} \right) \quad \text{Eq}(3.8) \]

\[ I_4 = I_6 \quad \text{Eq}(3.9) \]

M5 and M7 sizes are calculated by using current equations as we already know \( I_5 \) and \( I_7 \) current values. Table 2 shows the calculated sizes for all transistors in two-stage amplifier.

To eliminate the RHP zero nulling resistor is added in series to the miller compensation capacitor, which can be calculated using Eq (3.10)

\[ R_x = \frac{1}{g_{m6}} \quad \text{Eq} (3.10) \]

Table 2 Calculated Transistor sizes for two-stage amplifier

<table>
<thead>
<tr>
<th>Transistors</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>M5</th>
<th>M6</th>
<th>M7</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/L ((\mu)m/nm)</td>
<td>15.22/100</td>
<td>15.22/100</td>
<td>30.4/100</td>
<td>30.4/100</td>
<td>30.4/100</td>
<td>130.6/100</td>
<td>121.6/100</td>
</tr>
</tbody>
</table>
3.1.2.1 Simulation

The unity gain bandwidth (GBW) and low frequency gain (in dB) for operational amplifier is measured by performing ac analysis. Both inputs inn and inp are given as sinusoidal inputs with -0.5V and 0.5V of amplitude respectively. Using dB20 function in Cadence calculator Gain plot in dB is plotted. As shown in the Figure 14 designed two-stage op amp is having low frequency gain of 59.6295dB and unity gain bandwidth at 599.845MHz, f-3dB of 1MHz. Performance measurements for designed op amp are given in Table 3.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain(dB)</td>
<td>59.6295</td>
</tr>
<tr>
<td>Unity GBW</td>
<td>599.845MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>73.8°</td>
</tr>
<tr>
<td>f-3dB</td>
<td>1MHz</td>
</tr>
</tbody>
</table>
Figure 14 Unity GBW and DC measurement of two-stage operational amplifier
3.2 SAR ADC Design

As shown in the *Figure 15* Successive Approximation Register (SAR) ADC consist a sample hold circuit, a comparator circuit, a SAR circuit, a digital to analog converter. Binary search Algorithm is used to design SAR ADC. Input signal (Vin) is sampled using sample and hold and the sampled output is given as input to comparator. Now the SAR circuit sets the MSB bit value to ‘1’ and the rest of the bits to ‘0’. DAC converts the SAR digital bits to analog output voltage Vout (Half of the reference voltage). Analog output from DAC is given as reference input to the comparator. Comparator compares the sampled Vin with Vout of DAC. If Vin is greater than Vout of DAC then comparators result is ‘1’, or else the result will be ‘0’. Now based on the comparator result SAR will decide the MSB value and generates the next approximation bits. And the cycle continues until the LSB bit is decided. Hence, N-bit SAR ADC requires N clock cycles for converting one sample. *Figure 16* shows an algorithm for 3bit conversion using SAR logic.
Figure 15 SAR ADC Block Diagram

Figure 16 3-bit conversion of SAR logic
Because of its simple architecture SAR ADC consumes less area. And the only analog component in entire architecture is a comparator hence it consumes less power compared to rest of ADC architectures. Technology scaling also helps in achieving less power and less die size. All the sub circuit architectures of SAR ADC are stated in below sections.

3.3 Sub circuits of SAR ADC

3.3.1 Sample Hold circuit

A sampling switch is the front end of the ADC and requires careful attention during design. The implementation of switch depends on the required bandwidth and accuracy. Sample hold circuit contains CMOS switch and a capacitor. Switch can be implemented by using single NMOS or PMOS or more complicated bootstrapping switch or a complementary CMOS switch. The simplest and best way to implement this switch is using complementary CMOS transistors. Switch operates in two modes, first is tracking mode. In this mode when the sampling signal is high and the switch is connected, it tracks the analog input signal. Second one is hold mode; it holds the analog value when the sampling signal turns to low. Regardless of the type of architecture sample hold circuit shows great impact on the dynamic performance of ADC.
This thesis uses two complementary CMOS switch and a holding capacitor of 50fF to achieve full range input sampling. As the supply voltage is low for 65nm CMOS technology there will be voltage drop due to leakage currents. This degrades the sampling accuracy. One of effective solution to reduce this sub threshold leakage currents is increasing the channel length. Hence as shown in the Figure 17, stack of two CMOS switches are used.

### 3.3.1.1 Simulation

Sample hold circuit is simulated in Cadence Virtuoso. Figure 18 shows the output functionality of sample hold circuit having sinusoidal input of 10MHz frequency sampled using 1GS/s clock. In Figure 18 top waveform is 1.0GHz clock signal and the bottom waveform consists of both input signal and sampled output signal which exactly follows input signal with error less than 1mV.
Figure 18 Sample hold circuit output for given sinusoidal wave input
3.3.2 Comparator

In this thesis, a double tail latch comparator design is used instead of two stage op amp followed by a D flip flop. The advantage of using the double tail latch comparator is to achieve high resolution. Resolution of comparator is decided by how accurate it can measure the minimum deviation from the input signal. Designed double tail latched comparator detects a deviation of 0.3mV from the input signal, which can be used in implementing 10-bit SAR ADC. And this architecture is well suited for low supply voltage. The schematic of comparator circuit is shown in Figure 19 [1]. As shown in the figure the comparator consists of a pre-amplifier followed by a double tail latch. Using a preamplifier will reduces the effect of input offset and the thermal noise, which helps in achieving less power and high SNR.
The bottom tail is used as input stage and the upper stage is used for latching purpose. During reset phase clk is low and clkb is high which makes M5 and M16 off to disable both bottom and top tails. M8 and M9 charge the output to Vdd and M10 and M11 are turned on to discharge the output of the cross coupled pair to ground. In the latch phase clk is high and clkb is low, the output of bottom tail drops from vdd to ground. The cross
coupled inverters formed by M12, M13, M14, M15 transistors will regenerate the output of the top latch. This helps in achieving the same and less raise and fall times of the output.

3.3.2.1 Simulation

The double tail comparator circuit is simulated in Cadence Virtuoso. Figure 20 shows the functionality of comparator which can compare the sinusoidal input with full scale range of 1V having amplitude of 0.5V and offset as 0.5V with the reference input of 0.5V. The accuracy of comparator is estimated by the rise time and fall time of the output waveform. The double tail latched comparator given in this thesis is having rise time of 3.57ps and fall time of 3.64ps for the output waveform at 1GS/s clock frequency.
Figure 20 Comparator output waveform with raise and fall time.
Figure 21 Comparator output waveform when input sinusoidal wave is having amplitude of 0.5mV and offset as 0.5V.

Figure 21 shows input sine wave having amplitude of 0.5mV and offset as 0.5V with frequency of 100MHz and clock frequency of 1GHz. Figure 22 shows the duty cycle measurement of comparator output as 50.29%. with input having 0.3mV of amplitude with
offset as 0.5V. From Figure 22 it can be seen that the minimum amplitude deviation that can be detected by designed double tail latched comparator is 0.3mV.

Figure 22 Duty Cycle measurement for comparator output with input having amplitude of 0.3mV with offset of 0.5V.
3.3.3 SAR Register

As stated in section 3.3 successive approximation register ADC implements binary search algorithm by using control logic. There are two fundamental approaches to design SAR control logic. One is using ring counter and a shift register. This method is proposed by Anderson [2]. This approach requires at least of 2N flip flops. Another approach is using N flip flops and some combinational logic [2].

SAR operation is illustrated in Table 4. Based on the comparator result SAR control logic determines the value of digital bits sequentially. Conventional SAR logic takes N+2 clock cycles to complete entire conversion of one sampled input. As shown in the Table 3 first clock cycle is used as reset mode to set all the outputs of flip flops to ‘0’. In the next N clock cycles the data is converted and each bit is determined sequentially based on comparator output. Last clock cycle is used to sort the results of the complete conversion.

Table 4 Algorithm of flip flop states in SAR control logic

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Sample</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>comp</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>a9</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>a9</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>a8</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>a9</td>
<td>a8</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>a7</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>a9</td>
<td>a8</td>
<td>a7</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>a6</td>
</tr>
</tbody>
</table>
In this thesis second approach of using N flip flops and combinational logic is used to build the SAR control logic. Optimization is done by reducing the clock cycles to N+1 instead of N+2 at the cost of two more flip flops, by removing reset pin (step 0). The architecture of SAR control logic is shown in Figure 23.
Figure 23 SAR control Logic
As shown in Figure 23, SAR control logic consists of DFF_MUX and OR logic gates. As this architecture has only N flip flops, these flip flops must guess as well as store the converted result. As seen in the Table 3 flip flops have three operations to perform. They are

1. Shifting right
2. Taking the comparator results
3. Memorization mode.

All these three operations are performed by both DFF_MUX and OR gates combinedly. Shifting logic ‘1’ to right and loading the comparator result operations are taken care based
on previous flip flop output. But the memorization of previous state output depends on OR gate output. OR gate logical expression can be given as

\[ A_{kn} = (A_{k(n-1)} + D_n) \]

Where \( A_{k(n-1)} \) is previous state OR gate output and \( D_n \) is the present state flip flop value.

For LSB bit OR gate \( A_{k(n-1)} \) value is connected to ground to end the conversion.

To start the SAR operation first is the initialization state. In this state first flip flop must be set to 1 and the rest to ‘0’. To provide this condition two flip flops are used by taking the output of LSB flip flop as input. In the next steps each DFF_MUX has to take the output of the previous flip flop, or the result of comparator, or the OR gate value. As there are three inputs to be chosen by flip flop, a 3 to 1 multiplexer is required. As shown in Figure 18, 4 to 1 mux is used to select from three inputs. Based on the select inputs S0 and S1 three inputs were chosen as shown in Table 5.

Table 5 4 to 1 MUX operation

<table>
<thead>
<tr>
<th>S0</th>
<th>S1</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Shift ‘1’ to right</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Load Data</td>
</tr>
<tr>
<td>1</td>
<td>-</td>
<td>Memorization</td>
</tr>
</tbody>
</table>

D flip flop used in is designed using transmission gates. Thus, the SAR control logic performs the binary search algorithm and finals the digital bit word of the sampled input.
4. Implementation and Results

In this chapter the implementation of 10-bit DAC along with 10-bit SAR ADC in 65nm CMOS technology with supply voltage of 1V is addressed. Schematic of the designed DAC is shown in Figure 25. Using Cadence Virtuoso DAC functionality and dynamic performance is tested. SAR ADC functionality is also tested and presented.

![Diagram](image.png)

*Figure 25 Schematic implementation of C2C DAC in cadence virtuoso.*

4.1 DAC performance

The proposed C2C DAC architecture along with DAC switch is simulated by applying the digital input codes using pulse signals for 10 bits to cover the full output voltage range. Figure 26 shows the output ramp from zero to full scale with average power consumption of 88.14μW
Figure 26 Output wave form of 10-bit C2C DAC
4.1.1 DAC Test Bench

DAC test bench is created to test the dynamic and static performances of proposed 10-bit C2C DAC as shown in Figure 27. 10-bit ideal ADC is constructed using the ideal ADC component in Cadence ahdl Library. All ideal components in ahdl Library are built using Verilog-A code. Verilog-A code of ideal ADC is modified to 10-bit ideal ADC and used in the test bench. The ideal output bits of ADC are fed as input to proposed C2C DAC and ideal DAC which is also built using Verilog-A code component from ahdl Library. Functionality of designed C2C DAC is tested by applying input sine wave of 100MHz frequency to ideal ADC sampled at 1GS/s. As shown in the Figure 28 to Figure 31 that output of the DAC, sampled sine wave matches the input well.

Figure 27 DAC Test Bench
Figure 28 Designed C2C DAC output for the sinusoidal wave of 10MHz input frequency
Figure 29 Designed C2C DAC output for the sinusoidal wave of 15MHz input frequency
Figure 30 Designed C2C DAC output for the sinusoidal wave of 80MHz input frequency
Figure 31: Designed C2C DAC output for the sinusoidal wave of 100MHz input frequency
4.1.2 Static Performance

Static performance metrics INL and DNL for proposed C2C DAC were measured using the DAC test bench output waveforms. To measure worst INL and DNL values input to ideal ADC is given as piecewise linear function resulting a ramp wave from 0.3V to 0.7V and sampled with clock of 1GHz frequency. Then DNL functions in the Cadence calculator are applied to the proposed C2C DAC output. While simulating calculator will generate a text file containing DNL value for each code. This text file is exported to MATLAB to plot the DNL value in terms of LSB for each code as shown in Figure 32. And the worst case DNL for the proposed DAC is 0.5LSB. Similarly, for INL value Cadence calculator is used to get the output voltage difference values of ideal DAC output and the proposed C2C DAC. The text file generated with output voltage difference at each code is exported to MATLAB to plot the INL values in terms of LSB for each code. And the worst case INL value for proposed C2C DAC is 0.31LSB as shown in Figure 33.
Figure 32 DNL plot using MATLAB code for designed C2C DAC

Figure 33 INL plot using MATLAB code for designed C2C DAC
4.1.3 Dynamic Performance

The dynamic performance is one of the important factors in assessing the performance and accuracy of the DAC. Dynamic performance of the DAC is measured by applying 500MHz sinusoidal input signal to the ideal SAR ADC and sampled at 1GS/s. Using Cadence calculator FFT operation is performed on the output of C2C DAC. Table 6 gives the SFDR measurement values for designed C2C DAC at different input frequencies. Figure 34 shows the SFDR measurement of C2C DAC at low input frequency of 10MHz input is 66.56dB. Figure 35 shows the SFDR measurement of C2C DAC at frequency of 15MHz input is 67.18dB. Figure 36 shows the SFDR measurement of C2C DAC at frequency of 80MHz input is 64.313dB. Figure 37 shows the SFDR measurement of C2C DAC at frequency of 100MHz input is 66.93dB. Figure 38 shows the SFDR measurement of C2C DAC at frequency of 500MHz input is 71.95dB.

Table 6 SFDR measurement for different input frequencies

<table>
<thead>
<tr>
<th>Input frequency</th>
<th>SFDR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10MHz</td>
<td>66.56</td>
</tr>
<tr>
<td>15MHz</td>
<td>67.18</td>
</tr>
<tr>
<td>80MHz</td>
<td>64.313</td>
</tr>
<tr>
<td>100MHz</td>
<td>66.93</td>
</tr>
<tr>
<td>500MHz</td>
<td>71.95</td>
</tr>
</tbody>
</table>
Figure 34 SFDR measurement of C2C DAC with input frequency of 10MHz with SFDR as 66.56dB
Figure 35 SFDR measurement of C2C DAC with input frequency of 15MHz with SFDR as 67.185dB
Figure 36 SFDR measurement of C2C DAC with input frequency of 80MHz with SFDR as 64.313dB
Figure 37 SFDR measurement of C2C DAC with input frequency of 100MHz with SFDR as 66.936dB
Figure 38: SFDR measurement of C2C DAC with input frequency of 500MHz with SFDR as 71.952dB
4.2 SAR ADC

4.2.1 SAR Control Logic

Proposed architecture of SAR control logic is tested in Cadence Virtuoso. Functionality is verified based on Table 3. Figure 39 and Figure 40 show the digital output bits D9 to D0 of SAR control logic based on the given comparator input. As shown in Figure 39 comparator input is given logic ‘0’ for entire period of 800ns. So digital bits D0 to D9 are storing logic ‘0’ at 11\textsuperscript{th} clock cycle (N+1).
Figure 39 SAR Control Logic when comparator input is given as '0'
Figure 40 SAR Control Logic when the output from comparator is a “0101010101”

In Figure 40 the comparator input is given as “0101010101” for entire time period of 550ns. So now the digital bits D0 to D9 stores 0101010101 at 11th clock cycle.
4.3 SAR ADC Test bench

SAR ADC is implemented in Cadence Virtuoso using TSMC 65nm CMOS Technology. Test bench for SAR ADC is built by connecting all the circuits designed as shown in the Figure 15 architecture of SAR ADC. This test setup is simulated at 1V power supply and an input at 9MHz frequency to check the functionality purpose.

Using the digital bits sampled analog signal is calculated by using the binary weighted equation. This can be given as

\[
VT(\text{/out}) + VT(\text{/out1}) \times 2 + VT(\text{/out2}) \times 4 + \ldots + VT(\text{/out9}) \times 512)(0.4/1/1023) + 0.3
\]
Figure 41 SAR ADC output waveform using proposed C2C DAC structure.
4.4 Power Dissipation

The power dissipation of the ADC can be categorized into the digital sub-circuits, and the analog circuits. The analog power dissipation is based on the current drawn through the load resistor by the converter. In addition to this, the digital circuits will consume power. The average power dissipation for the comparator is 226.7µW, the SAR logic is 1.875µW, the C2C DAC is 88.14µW. Table 7 shows the overall power contribution of the digital circuits. From the Table 7, it can be seen that the comparator circuit consumes most of the power among all the circuit components. It is because of its preamplifier and latch stages. The total power consumed by 10-bit SAR ADC is measured to be 427.4µW at input frequency of 500M Hz.

Table 7 Power consumption by components used in SAR ADC

<table>
<thead>
<tr>
<th>Component</th>
<th>Power consumption (µW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAR Logic</td>
<td>1.875</td>
</tr>
<tr>
<td>Comparator</td>
<td>226.7</td>
</tr>
<tr>
<td>C2C DAC</td>
<td>88.14</td>
</tr>
<tr>
<td>SAR ADC</td>
<td>427.4</td>
</tr>
</tbody>
</table>
4.5 Performance Comparison

There are several data converter architectures of same resolution and technology exists in literature. A few of these different converters are compared with the designed C2C DAC without using operational amplifier. A summary of key performance measures comparison can be seen in Table 8. From the Table 8 it can be seen that the converter presented in this thesis has the lowest power consumption, consuming $88.14\mu W$. The INL of the designed C2C DAC is best of having 0.31LSB whereas the highest INL is from [13] having 2.0LSB.
Table 8 Performance Comparison of DAC Architectures

<table>
<thead>
<tr>
<th></th>
<th>[4]</th>
<th>[12]</th>
<th>[13]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS Technology</td>
<td>0.35μm</td>
<td>0.18μm</td>
<td>0.13 μm</td>
<td>65nm</td>
</tr>
<tr>
<td>Resolution</td>
<td>10</td>
<td>8</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>3.65mW</td>
<td>-</td>
<td>0.5mW</td>
<td>88µW</td>
</tr>
<tr>
<td>Power scaled to 65nm</td>
<td>1.106mW</td>
<td>-</td>
<td>0.3mW</td>
<td>0.088mW</td>
</tr>
<tr>
<td>SFDR (dB)</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>71.95</td>
</tr>
<tr>
<td>Conversion rate</td>
<td>1.75MS/s</td>
<td>5MS/s</td>
<td>2MS/s</td>
<td>1GS/s</td>
</tr>
<tr>
<td>INL</td>
<td>0.67LSB</td>
<td>1 LSB</td>
<td>2.0LSB</td>
<td>0.31LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>0.33LSB</td>
<td>0.6LSB</td>
<td>0.5LSB</td>
<td>0.5LSB</td>
</tr>
<tr>
<td>ENOB</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>11.65</td>
</tr>
<tr>
<td>FOM ( \left( \frac{10^4 \text{Hz}}{\text{mW}} \right) )</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>63.8</td>
</tr>
</tbody>
</table>
5. Conclusion and Future Work

5.1 Conclusion

This thesis presents a high bandwidth data converter. The design procedure of converter circuits is addressed to prove the functionality and accuracy. Each sub circuits which are used in designing the data converter are discussed. Contribution from this thesis are:

- A high bandwidth 10-bit C2C DAC is designed and implemented in TSMC 65nm CMOS technology. All the performance metrics were compared with other existing works. The converter can operate at 1GS/s with an input bandwidth of 500MHz without operational amplifier circuit. Designed converter has the least power consumption of 88.14 µW compared to all compared works. This converter has SFDR of 71.95dB and an ENOB of 11.65.

- A 10-bit SAR ADC is implemented using the proposed C2C DAC structure in TSMC 65nm CMOS technology. It was simulated with 1V power supply with input having 0.4 V_{PP} range at 9MHz frequency. Total power consumption of entire SAR ADC is 427.4 µW which is very less compared to many of compared DAC structures.
5.2 Future Work

Few techniques can be used to increase the performance of data converters potentially. Further optimization of operational amplifier will increase the bandwidth of input signal for entire ADC circuit. The digital sub circuits can be furthermore optimized to achieve less power and high accuracy. Sample and hold buffer can be used to achieve the better sampled signal with capability of driving high loads. Finally, time interleaved technique can be used to increase the sampling rate of the data converters.
6. References


