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Resonant Gate-Drive Circuits for High-Frequency Power Converters

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Resonant Gate-Drive Circuits for High-Frequency Power Converters

A dissertation submitted in partial fulfillment

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By

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Abstract

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The development trend of power converters motivates the pursuit with high density, high efficiency, and low cost. Increasing the frequency can improve the power density and lead to small passive elements and a fast dynamic response. Each one of these power converters must be driven by a gate-drive circuit to operate efficiently. Conventional gate-drivers are used up to frequencies of about 5 MHz and suffer from switching losses. Therefore, the development of switch-mode power supplies (SMPS) operating at high frequencies requires high-speed gate drivers. The presented research in this dissertation focuses on analysis, design, and development of new types of resonant gate-drive circuits to drive power transistors at high frequencies.

Three proposed topologies are presented in this dissertation. Two topologies are single-switch ZVS gate-drive circuits. The attractive features of the two circuits are : (a) suitable to drive a low-side power transistor, (b) capable of operating at high frequencies with quick turn-ON and turn-OFF transitions, (c) low power loss due to zero-voltage switching in the driving switch, (d) a significant increase in gate-source voltage of the driven switch with respect to the input voltage, (e) small energy storage components, and (f) designed to operate at switching frequency 20 MHz and a supply voltage of 4 V. The third presented topology is a class-D resonant gate-drive circuit. A series resonant circuit is formed by the resonant inductor and the input capacitance of the MOSFET to achieve the charge and discharge process of the transistor input capacitance. The proposed circuit can be used as a gate-drive circuit to drive low-side or high-side power switches operating at 6.78 MHz.

In each above topology, detailed steady-state operation and derived expressions for the steady-state waveforms are presented. The analysis includes predicted power loss expressions in circuit components to estimate the overall losses in the gate-drive circuits. A design procedure of the proposed gate drivers is developed. The simulations and experimental results are given to validate the theoretical analysis.

Finally, in the last chapter of the dissertation, the behavior of an air-core inductor operating at high frequencies is investigated. An appropriate model for the inductor is introduced to represent the effect of high frequencies on the inductor's winding resistance. The analysis includes an expression to estimate the power loss in the air-core inductor. A detailed design methodology is presented to predict the dc and ac characteristic of the air-core inductor. A design example of an air-core inductor is given for switch-mode power gate driver operating at high frequencies.

List of Symbols

Chapter 2

C_{gd}	Gate-drain capacitance
C_{gs}	Gate-source capacitance
C_{ds}	Drain-source capacitance
g_m	Transconductance of a MOSFET
A_v	Voltage gain
V_{TH}	Threshold voltage of a MOSFET
Q_g	Total gate charge
M_i	Power MOSFET, ($i = 1, 2$)
D	Duty cycle
v_{GS}	Gate-source voltage
V_G	DC supply voltage
R_g	Internal gate resistance of a MOSFET
Z	Characteristic impedance
E_s	Total energy supplied

Chapter 3

i_L	Instantaneous inductor current
$i_L(0)$	Initial inductor current
Δi_L	Peak-to-peak inductor current
D	Duty cycle of a switch
L	Resonant inductor
V_I	DC input voltage
f_s	Switching frequency
f_o	Resonant frequency
ω_s	Angular switching frequency
ω_o	Angular resonant frequency
M	Driving switch
M_D	Driven switch
C_{iss}	MOSFET parasitic input capacitance
C_{oss}	MOSFET parasitic output capacitance
C_{rss}	MOSFET parasitic reverse transfer capacitance
i_S	Switch current
C	Equivalent capacitance
Q	Quality factor
Z_o	Characteristic impedance
r_L	Inductor resistance
R	Total internal gate resistance
a	Frequency ratio
C_{in}	Equivalent input capacitance of a driven MOSFET
V_{bi}	Built-in potential

Chapter 4

V_I	DC input voltage
V_{GS-M}	Drive voltage of a MOSFET
L_r	Resonant inductor
C_r	Passive capacitor
T	Switching time period
ω_r	Angular second harmonic frequency
r_{DS}	MOSFET on resistance
i_R	Current of passive network circuit L_r-C_r
I_m	Amplitude of i_R current
ϕ	Phase shift of i_R current
Q_{gs}	Gate-source charge
Q_{gd}	Gate-drain charge
Q_g	Total gate charge
Z_o	Characteristic impedance
Z_g	Equivalent impedance network
P_M	MOSFET conduction power loss
P_{rL}	Inductor conduction loss
P_{Rg}	MOSFET gate conduction loss
P_F	Power loss in L_r-C_r circuit

Chapter 5

M_i	Half-bridge MOSFETs ($i = 1, 2$)
M	Driven transistor
L_r	Resonant inductor
t_r	Time rising
t_f	Time falling
r_{on}	MOSFET on resistance
R_L	Load resistance of the driven switch
I_m	Amplitude of gate current i_G
I_I	Average input current
I_{Gpk}	Peak value of gate current i_G
P_I	Input power
P_{gate}	Gate power loss of a MOSFET

Chapter 6

A	Relative winding inner diameter
A_c	Core cross-sectional area
C_{tt}	Turn-to-turn capacitance of single-layer inductor
C	Total parasitic capacitance
d_i	Inner wire diameter
d_o	Outer wire diameter
D_c	Diameter of the core
D_t	Effective coil diameter
ϵ_r	Relative permittivity of the insulator
ϵ_0	Absolute permittivity of free space (8.854×10^{-12} F/m)
f_s	Switching frequency
ω_s	Angular switching frequency
f_{sr}	Self-resonant frequency
ω_{sr}	Angular self-resonant frequency
L	Total equivalent inductance
l_w	Total length of the winding
l_c	Length of the core
l_T	Average length per turn of winding
N	Number of winding turns in the inductor
Q_{L0}	Quality factor of the resonant circuit
p	Winding pitch
R_{wdc}	DC winding resistance
R_w	AC winding resistance
R_s	Equivalent series resistance
s	Separation length
μ_0	Absolute free-space permittivity ($4\pi \times 10^{-7}$ H/m)
δ	Winding skin depth
μ_{rc}	Manufacturer-specified core relative permittivity
η_p	Porosity factor
ρ	Copper resistivity (1.724×10^{-8} Ω.m)
X_s	Equivalent series reactance
Z	Impedance of the inductor

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1 Introduction

The electronic technology in our life has broadly expanded. It is changing the way we live and it is becoming the basis for the information. Most people use electronic devices daily such as computers, cell phones, television, artificial lighting, and household appliances. All the above devices require power conversion. In the majority of cases power conversion is manged by switch-mode power supply (SMPS) where it is necessary to drive a switch into ON and OFF conditions. Several power conversion topologies utilized in SMPS require gate driver to work effectively and achieve an efficient power conversion [1].

1.1 Background

Gate driver is an integral part of a power-electronic converter. It forms an important interface between a power-electron converter stage and a control stage [2]. The existing gate-drive circuits are designed in many different forms. They are all used with a specific function to drive the switches, such as boost converter and class-E for pulse-width modulation (PWM) operation. Some gate drivers are designed to be resonant with the passive components [3]-[9] or recovered energy [10]-[12]. The most widely used in the industry is the conventional gate driver because it is simpler and more cost effective [13], [14]. Conventional gate driver, which consists of two complementary MOSFETs, can be used at frequencies up to about 5 MHz [15]. However, they suffer from high switching losses and gate losses. Tremendous improvements have been made during the past decade in the gate-driver circuits, but relatively little advancement has occurred in reducing switching losses at high frequencies. An essential requirement of switching devices at high frequencies is low switching losses.

A topology with a single switch has advantages, especially for operation at high switching frequencies [16], [17]. Among many zero-voltage switching (ZVS) inverters, the resonant inverter with a ground-ended transistor has the great advantage of operating at high-switching frequencies. However, the single-switch inverter has high stress of drain-source voltage. Thus, several techniques have been utilized to alleviate voltage stress in the switch. One common method is used to add a harmonic-tuned circuit as demonstrated in [18], [19]. Two-widely resonant topologies exist that achieve

low switching losses for operation at high frequencies are class-E and class-Φ_2 [20]. Class-E is a single-switch inverter that can operate at high switching frequencies with high efficiency [21], [22]. It has zero voltage, zero dv/dt switching conditions and it does not suffer from switching loss [1]. Several topologies are derived from class-E, such as class Φ_2 and resonant boost converter [23]-[25].

1.2 Current State-of-the-Art of Gate Drivers

Today's gate drivers, which are used in power converters, consist of at least two transistors and can be operated at frequencies up to about 5 MHz [15]. In conventional gate-drive circuits, such as two-transistor inverter, hard switching power MOSFETs suffer from switching losses and severely restrict the efficiency at high frequencies. This topology exhibits the following challenges: (a) difficulty to achieve control of dead-time up to a few nanoseconds (b) high-side (floating) transistor, and (c) synchronization issues between the low-side and high-side switches. For instance, in converters with more than one transistor, it is difficult to implement high-side gate driver and provide dead times on the order of a few nanoseconds [26], [27].

1.3 Motivation

The majority of electronic devices generally require SMPS, which is used in power conversion due to its high efficiency and high density. The size of SMPS depends on passive energy storing elements (inductors and capacitors). Therefore, increase in switching frequencies will achieve high efficiency, high power density, and reduced size. With increasing switching frequency, the converter's transient response can be accelerated, leading to improvement of the power converter performance [2], [28].

In conventional gate-drive circuits, hard switching power MOSFETs suffer from switching losses and severely restrict the efficiency associated with high frequency operation [10]. The resonant technique has proven to be a good choice for mitigating the power losses in gate-drive circuits [29]. Thus, soft-switching technique is one of the most efficient methods to reduce the switching loss and improve system efficiency under high-frequency operation [30], [31]. Moreover, the small values of output capacitance C_{oss} and the input capacitance C_{iss} of power MOSFETs play important roles to reduce the switching loss in the circuit [6], [32].

1.4 Objectives

Work on power converters operating at high frequencies has been going on for the last few decades. Since gate drivers are an integral part of power-electronic converters, the properties of these gate drivers are important as they offer substantial performance improvements for the power conversion systems. The objectives of this dissertation are as follows:

1. To investigate the existing state-of-the-art gate-drive circuits and identify their potential advantages and drawbacks.

2. To advance the gate-driver technology for power transistors for high switching frequencies.

3. To propose a single-switch gate-drive circuit with superior soft-switching performance for high-efficiency operation at high switching frequencies. It can be used in pulse-width modulated, inverters, and resonant dc-dc converters.

4. To present a half-bridge gate-drive circuit based on class-D for operation at high switching frequencies.

5. To derive the expressions for the steady-state waveforms and component values of the proposed gate-drive circuits.

6. To derive the expressions for the power losses in circuit components and to estimate the overall losses in the gate drivers.

7. To develop the design procedure of the proposed gate drivers.

8. To validate the theoretical analysis by simulations and experimental results.

9. To investigate the behavior of an air-core conductor and estimate the power loss in high frequency applications.

1.5 Structure and Contents

Chapter 1 covers an introduction to the dissertation with background, motivation, and the objectives of the research. The state-of-the-art is focused on description of the existing topologies of gate-drive circuits. Chapter 2 includes switch-mode power supply, gate charge profile, and single-switch topologies. Chapter 3 presents a single-switch gate-drive circuit. Chapter 4 proposes a high-frequency single-switch ZVS gate driver based on a class Φ_2 resonant inverter. Chapter 5 covers half-bridge resonant gate driver based on class-D inverter. The analytical expressions of the presented topologies are given. Furthermore, power-loss analysis, voltage and current stresses, and detailed design procedure are provided. The new topologies can be used to drive the power MOSFETs at high switching frequencies. Chapter 6 investigates the behavior of air-core inductor at high frequencies. An appropriate model for the air-core inductor is presented to estimate the power loss in the inductor. Moreover, a detailed design methodology is given to predict the dc and ac characteristic of the air-core inductor.

2 Switch-Mode Power Supplies and Topologies

A switch-mode power supply is a power converter that uses switching devices such as MOSFETs and energy storage components (inductors and capacitors) to provide the power at non-conduction state of the switching device [32]. The switches operate under specific frequency and they are not conducted continuously. Thus, the power loss in the circuit is reduced. The switching-mode power supply suffers from the ripples of both voltage and current at the output stage due to switching. These ripples can be suppressed by using low pass filter. Based on the structure of SMPS, it can be utilized for stepping up or down of DC input voltage. The switch-mode power supplies, which are used in different electronic equipment, have higher efficiencies of up to 97 %, flexible technology and high power density [26].

2.1 Miniaturization

The new technologies have focused for size reduction of electronic products. The miniaturization is based on the passive energy components and the transistors power semiconductors in power electronics. Increasing switching frequencies is an important factor towards miniaturization of power conversion [20]. Some of these are described in the following subsections.

2.1.1 Band Gap Energy of Semiconductors

The ability to increase the switching frequency and achieve the same efficiency depends on the power semiconductors [32]. These power semiconductors are based on the type of material. Now semiconductor companies develop the boundaries by increasing the band gap of power semiconductors. The important parameters of these materials are summarized in Table 2.1. In order to compare the different materials, different figures of merits (FOM) have been adopted to justify the best of one semiconductor material over the other. The most widely used are BFOM and JFOM. BFOM takes into account the conduction losses in power MOSFETs and JFOM depends on the high-frequency and high-power performance of transistors [1], [33].

Si MOSFET is the most widely used as a semiconductor material for power devices. It is proper in the circuits that require low voltage applications [34]. Si MOSFETs

Table 2.1: Material properties of Si, GaAs, SiC, and GaN at room temperature.

Property	Si	GaAs	SiC	GaN
Energy Band-Gap (eV)	1.12	1.42	3.26	3.39
Break Down Electric Field MV/cm	0.25	0.4	2.0-3.5	2-3.3
Electron Mobility μ ($cm^2/V.s$)	1300-1350	5000-8500	260-720	900-2000
Dielectric Constant $\in$ (cm^{-3})	12.8	12.5-13.1	10	9-9.5
Saturation Velocity (cm/s)	10^7	1.2×10^7	2.7×10^7	1.5×10^7
Thermal Conductivity W/m.K	150	500	450	130
JFOM	1	2.7	20	27.5
BFOM	1	2.7	20	27.5

technology is still dominating in the power electronics field [32]. In high-frequency applications, MOSFETs proved to be less efficient. For technologies, which used high frequencies and high voltages, gallium nitride (GaN) and silicon carbide (SiC) are more promising [35].

GaAs Gallium Arsenide has the highest mobility. It is excellent in the circuits that require high switching frequency [36]. Therefore, it is widely used in communication circuitry such as satellites, cellphones, and other radars applications. However, it is not suitable for applications that need more than few volts due to its low break down voltage.

SiC is semiconductor material, which has a wide-band gap energy 3.3 eV. It is fabricated in a way similar to that of Si and has several properties, such as operational capability at high temperatures and voltage due to the high break down field [32]. However, its electron mobility μ is less than of silicon, gallium arsenide, and gallium nitride. SiC has an advantage over Si, GaAs, and GaN because its critical field and thermal conductivity are high [37]. Thus, it is suited for high power applications.

GaN semiconductor, which is called high electron mobility transistor (HEMT), has superior performance. It can operate at high frequency due to the higher electron mobility formed by the two-dimensional electron gas (2DEG) between AlGaN and GaN layers [35]. GaN devices surpasses Si and SiC in terms of its ability in mobility and low energy consumption. Due to the higher break down field and thermal conductivity, it provides higher power and voltage levels than GaAs [2]. GaN devices can be used in many applications like RF, microwave, and digital circuits.

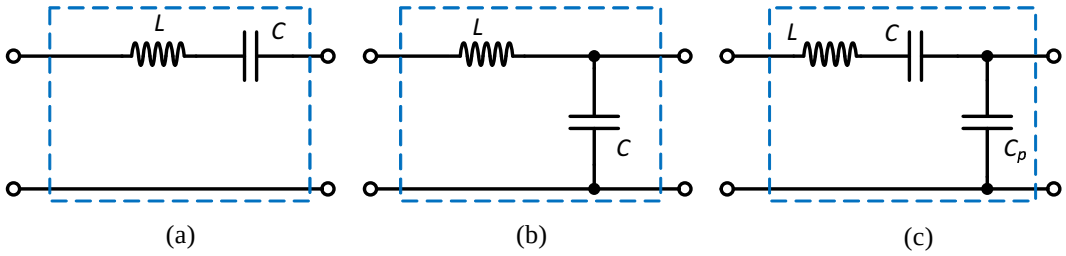

Figure 2.1: Resonant circuits. (a) Series resonant. (b) Parallel resonant. (c) Series-parallel resonant.

2.1.2 Resonant Circuits

Several types of resonant converters exist, but they can all be classified into three groups: series resonant, parallel resonant, and series-parallel resonant converters as shown in Fig 2.1. The series resonant converter has the lowest complexity and best efficiency; however, with light and no-load situations, it has a challenge with the output regulation [38]. Parallel resonant converter has good load regulation, but the output power is not scaled with the resonate current. Moreover, it has full load losses even at light loads, leading to low efficiencies [39]. To obtain the advantages and the drawbacks of both series and parallel resonant circuits, series-parallel resonant circuit has both the series and the parallel resonant elements [38]. By increasing the frequency, passive energy storage components in the resonant converters will be miniaturized.

2.1.3 Soft-Switching Operation

In the SMPS, the passive energy storing components are dominated. Increasing the frequency is the main way to reduce the size. However, switching losses will be significant, causing a reduction in efficiency [29], [40]. Conventional SMPS topologies such as buck and boost converters operate under hard switching. It means the transistor is still switching due to voltage or current running through the transistor causing to dissipate the energy in the transistor, i.e., switching losses as shown in Fig. 2.2. The switching loss gets larger when the switching frequency is increased, leading to a decrease in efficiency. In order to reduce the switching losses and increase the frequency, zero-voltage switching (ZVS) and/ or zero-current switching (ZCS) can be

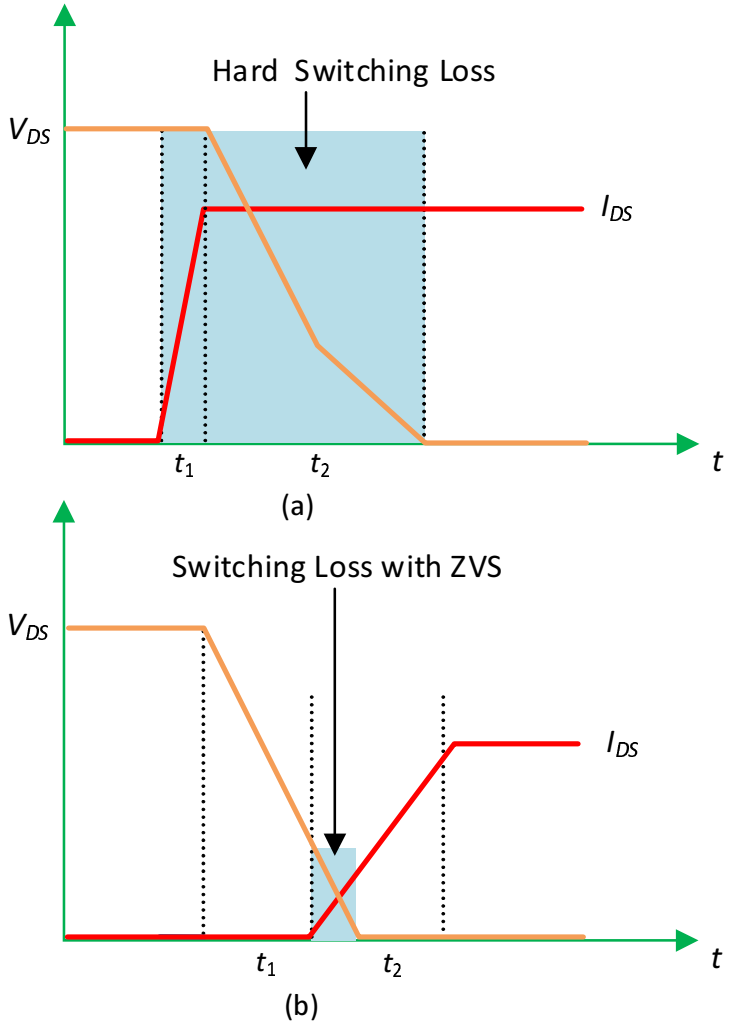

Figure 2.2: Switching waveform. (a) Hard switching. (b) Soft-switching technique.

employed [41]. The transistor turns ON when the voltage across the transistor is zero, or the current through the transistor is zero when it turns OFF. Theoretically, this should eliminate switching losses, but practically this is not applicable.

2.2 Gate-Charge Profile

During switching transient, the MOSFET is influenced by the parasitic capacitances, which are present in the structure of the device. The parasitic components and the body diode of the MOSFET play important roles in switching performance [37]. The parasitic capacitances in the gate-source C_{gs} and gate-drain C_{gd} correspond to the actual geometry for the MOSFET, while the drain-source capacitance C_{ds} is the

parasitic capacitance of the body diode. The switching performance is based on how quickly voltage changes across these capacitors. Thus, the most important parameters in high-switching applications are the parasitic capacitances [14]. The gate-drain capacitance C_{gd} is a function of the drain source voltage V_{ds} of the MOSFET, and it can be approximated by

$$C_{gd} = \frac{C_{gd(0)}}{\sqrt{1 + \frac{V_{ds}}{V_{TD}}}}, \tag{2.1}$$

where $C_{gd(0)}$ is the gate-drain zero-bias capacitance, and V_{TD} is the drain threshold voltage. The C_{ds} is non-linear junction capacitance of the body diode for the MOSFET. It depends on the voltage and can be described as

$$C_{ds} = \frac{C_{ds(0)}}{\left(1 + \frac{V_{ds}}{V_{bi}}\right)^m}, \tag{2.2}$$

where $C_{ds(0)}$ is the drain-source zero-bias capacitance, V_{bi} is the built-in potential, and m is the grading coefficient. The parasitic capacitance values of the MOSFETs devices are not mentioned directly in the datasheets of the transistors. Their values are obtained indirectly through the values of the input capacitance C_{iss}, reverse transfer capacitance C_{rss}, and the output capacitance C_{oss}. The gate-drain-capacitance C_{gd} can be determined as

$$C_{gd} = C_{rss}. \tag{2.3}$$

The gate-source capacitance C_{gs} is

$$C_{gs} = C_{iss} - C_{rss}, \tag{2.4}$$

and the drain-source capacitance C_{ds} is given by

$$C_{ds} = C_{oss} - C_{rss}. \tag{2.5}$$

In switching applications, the capacitance C_{gd} causes a further complication because of its place between the input and output of the device. Therefore, its influence depends on the drain-source voltage of the MOSFET. This phenomenon is called the "Miller's effect," and it can be expressed as

$$C_{gd(M)} = (1 + g_m R_L) C_{gd} = (1 - A_v) C_{gd}, \tag{2.6}$$

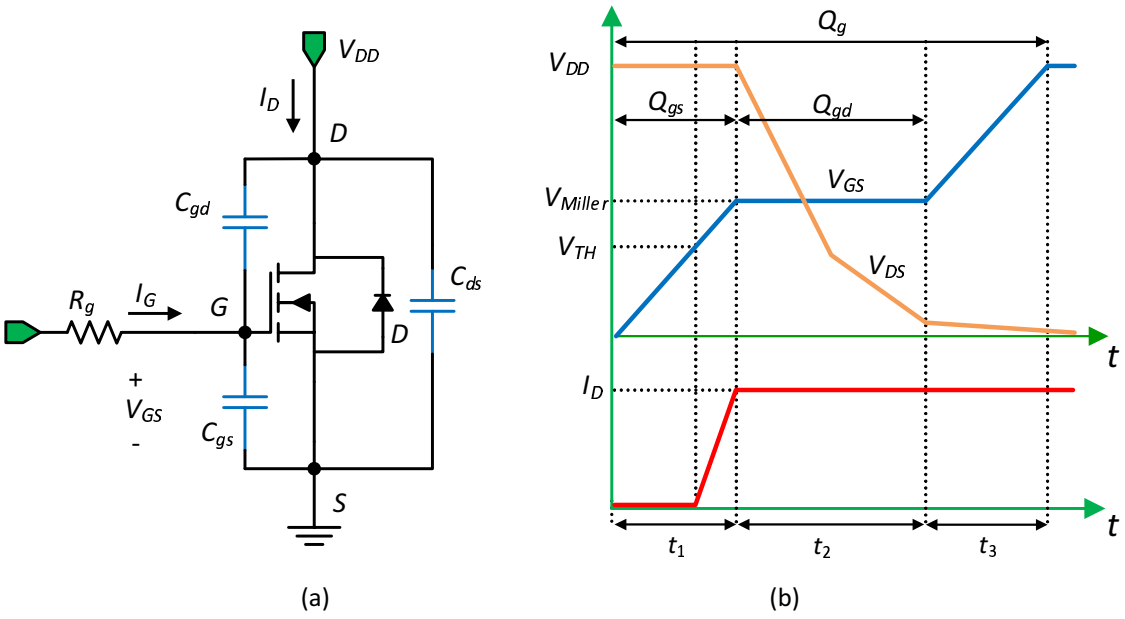

Figure 2.3: (a) Schematic of a MOSFET. (b) Qualitative gate charge waveforms.

where the voltage gain is

$$A_v = \Delta V_{ds}/\Delta V_{gs}, \tag{2.7}$$

and g_m is the transconductance of the MOSFET, which is a small signal gain in the linear region

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}. \tag{2.8}$$

The maximum current of the MOSFET in the linear region is

$$I_{DS} = (v_{GS} - V_{th})g_m. \tag{2.9}$$

The capacitance current $I_{C_{iss}}$, which is equal to the gate current I_G, is a function of the gate-source voltage v_{GS} and the input capacitance C_{iss}. The capacitance current $I_{C_{iss}}$ is

$$I_G = I_{C_{iss}} = C_{iss}\frac{\Delta v_{GS}}{\Delta t}. \tag{2.10}$$

The Q_g is the charge injected into the input capacitance C_{iss} of the MOSFET at time Δt. Thus, the gate current I_G can be expressed as

$$I_G = \frac{\Delta Q_g}{\Delta t}. \tag{2.11}$$

The behavior of switching transient of the MOSFET gives information on the description of gate charge as shown in Fig. 2.3. The total gate charge of the MOSFET can be estimated as

$$Q_g = C_{in} v_{GS}, \tag{2.12}$$

where C_{in} is the equivalent input capacitance. It can be expressed as

$$C_{in} = C_{gs} + (1 - A_v) C_{gd}. \tag{2.13}$$

2.3 Single Switch Topology

Single-switch topologies are the most common choice for high-frequency converters. These topologies have a switch, an inductor in series with the input voltage, and an LC resonant network [1]. In order to keep the volt-second balance across the inductor, the average switch voltage v_s of the MOSFET has to be equal to the input voltage V_I. To apply ZVS operation in these topologies, the quality factor should be high, the duty cycle is 50%, and the load of the inverter is optimum load resistance. For a duty cycle of 50%, the peak voltage across the switch is two times the input voltage V_I, but in reality, the peak voltage is greater than two times of the input voltage like Class-E inverter $v_S = 3.56 V_I$. This high voltage stress on the semiconductors is the biggest challenge with single-switch topologies. However, single-switch topologies are often chosen for high-frequency operations in several applications because of low losses and complexity. Moreover, they are connected with a low-side gate driver.

2.3.1 Class-E Topology

The class E inverter, the most commonly used in different applications, is the fundamental ZVS single-switch [18]. Several other topologies are derived from the class E inverter, such as the class EF_2 and class Φ_2 [20]. A schematic of class E that comprises of a single switch, two capacitors, and two inductors is shown in Fig. 2.4 [18]. The energy, which is stored at the output capacitance C_{oss}, is fully discharged before turning on the MOSFET. In this type of circuit, the class E has a disadvantage of a large inductor L_R. This result relatively increases the size of stored energy in the converter. In addition, the stress voltage at the switch is about 3.5 times of input voltage at duty cycle 50%. According to [1], the inverter can achieve both ZVS and

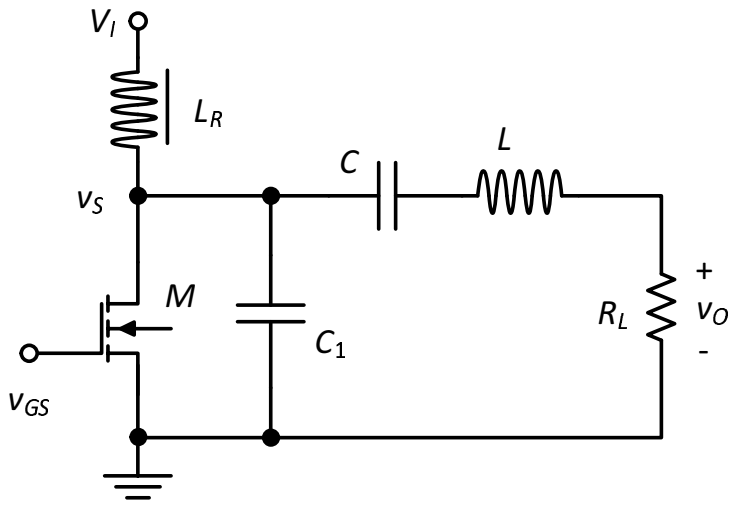

Figure 2.4: Class E inverter [18].

ZDS switching if the following apply:

$$R_L = \frac{8}{\pi^2 + 4}\frac{V_I^2}{P_O}, \tag{2.14}$$

$$C_1 = \frac{8}{\pi(\pi^2 + 4)}\frac{1}{\omega R_L}, \tag{2.15}$$

$$L = \frac{Q_L R_L}{\omega}, \tag{2.16}$$

$$C = \frac{1}{\omega R_L \left[Q_L - \frac{\pi(\pi^2-4)}{16}\right]}, \tag{2.17}$$

and

$$L_R = \frac{7f}{R_L}. \tag{2.18}$$

2.3.2 Class Φ_2 Topology

In single-switch topologies, the large voltage across the MOSFET is the major problem. The voltage stresses can be alleviated by using an LC resonant network connected in parallel with the MOSFET. The Φ_2 inverter, which is based on a resonant operation, provides lower switch voltage stress and faster settling time compared to other resonant inverters as shown in Fig. 2.5 [41]. The components of the $L_{MR}-C_{MR}$ resonant circuit are tuned to the second harmonic to alleviate the voltage across the switch with low peak amplitude. The voltage across the switch becomes a trapezoidal

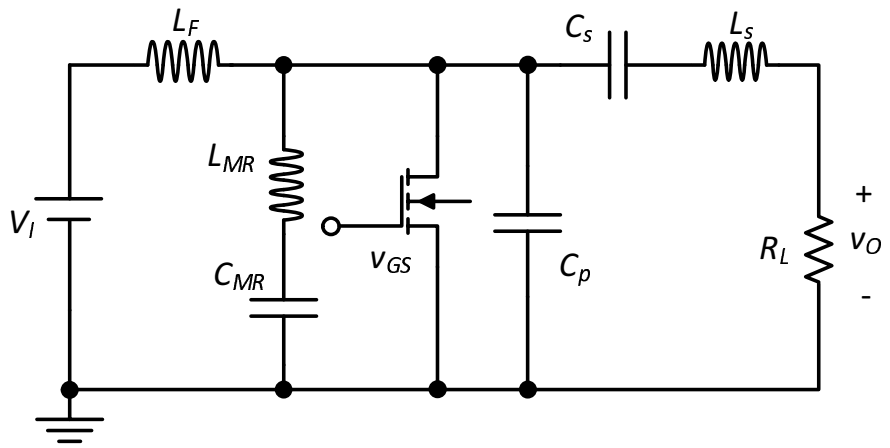

Figure 2.5: Class Φ_2 converter [41].

waveform, which is combined from first harmonic and third harmonic frequencies. As a result, the loss is reduced, and zero-voltage is applied at turn-ON and turn-OFF transitions [27]. In consideration of achieving ZVS, the duty cycle of the switching device is a constant 50% at fixed switching frequency. The key drawback of the inverter is that many stored energy components are presented, causing increases in the losses and power density. There are no exact equations of the added LC circuit and the input inductance for the calculations in the literature, but the following results are given by [18]

$$L_F = \frac{1}{9\pi^2 f_s^2 C_P}, \tag{2.19}$$

$$L_{MR} = \frac{1}{15\pi^2 f_s^2 C_P}, \tag{2.20}$$

and

$$C_{MR} = \frac{15}{16} C_P. \tag{2.21}$$

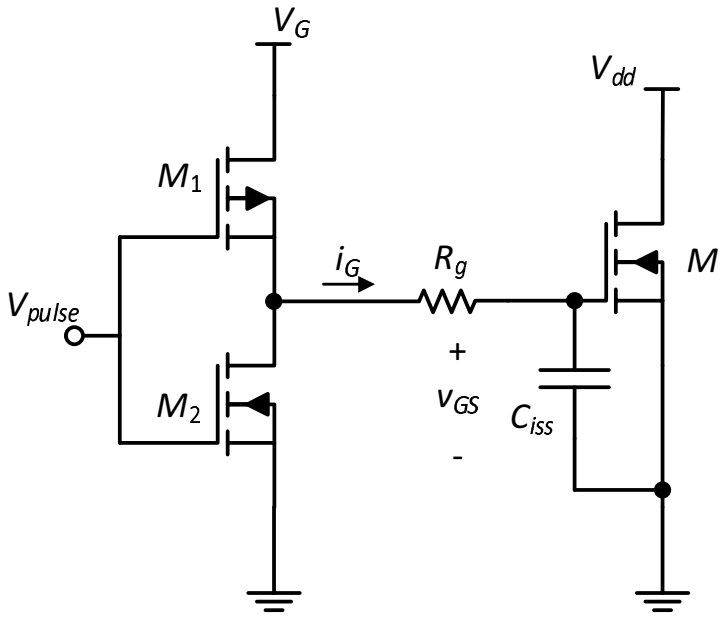

Figure 2.6: Conventional gate-drive circuit [42].

2.4 Half-Bridge Topology

2.4.1 Conventional Gate-Driver Circuit

The conventional gate driver, which consists of two complementary MOSFETs, is a totem-Pole structure as shown in Fig. 2.6 [42]. The drain terminals of the P-channel and the N-channel of the MOSFETs are connected in series. The resistor R_g includes the internal gate resistance of the driven MOSFET M_D and the on-resistance of the MOSFET M_1. The equivalent gate capacitance of the power MOSFET is represented as input capacitance C_{iss}. The conventional gate driver operates like the first order RC circuit. With a single triggering pulse, the MOSFETs M_1 and M_2 are alternatively turned ON and turned OFF. When M_1 is turned ON and M_2 is OFF, the equivalent circuit of the gate driver is shown in Fig. 2.7. The gate current supplies the charge to the input capacitance C_{iss} through the gate resistance R_g and the gate-source voltage v_{GS} is clamped to the V_G as shown in Fig. 2.8. During transient charging, the gate current i_G can be expressed as

$$i_G(t) = \frac{V_G}{R_g} e^{-t/R_g C_{iss}}. \tag{2.22}$$

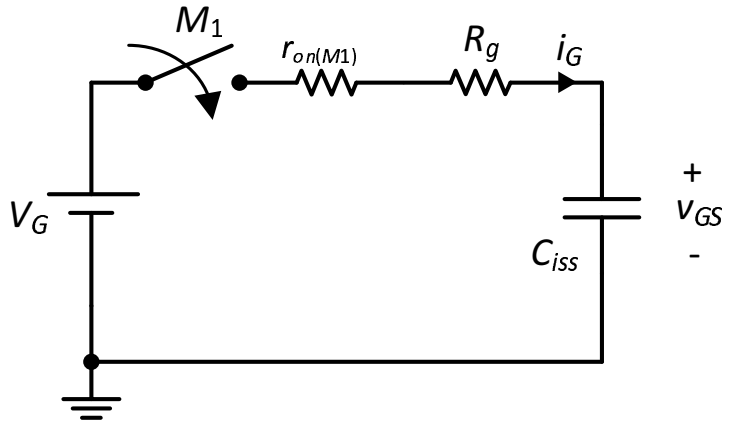

Figure 2.7: Equivalent circuit of conventional gate-drive circuit when M_1 is ON and M_2 is OFF.

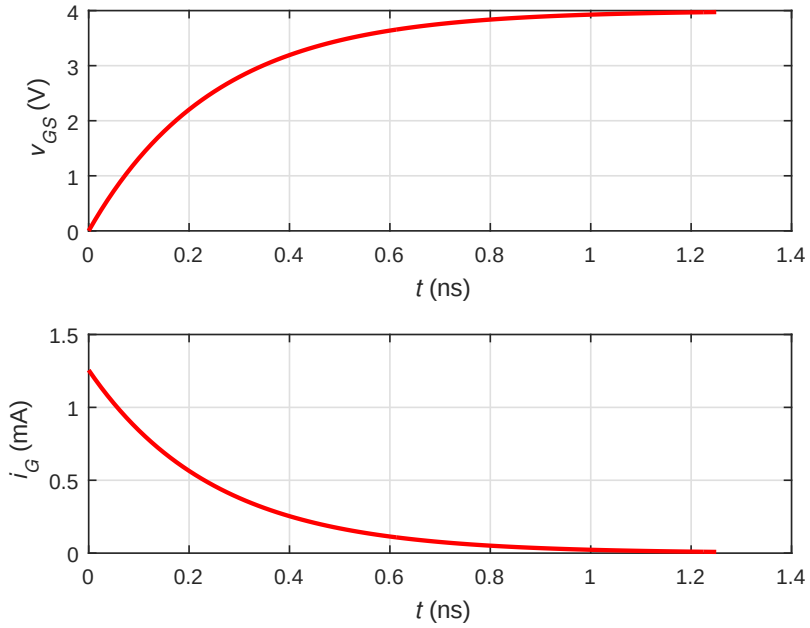

Figure 2.8: Gate-source voltage and gate current of the conventional gate-drive circuit when M_1 is ON and M_2 is OFF.

The characteristic impedance Z during the charging period is

$$Z = R_g + \frac{1}{\omega_s C_{iss}}. \tag{2.23}$$

The gate-source voltage v_{GS} across the input capacitance C_{iss} is

$$v_{GS}(t) = V_G \left(1 - e^{-t/R_g C_{iss}}\right). \tag{2.24}$$

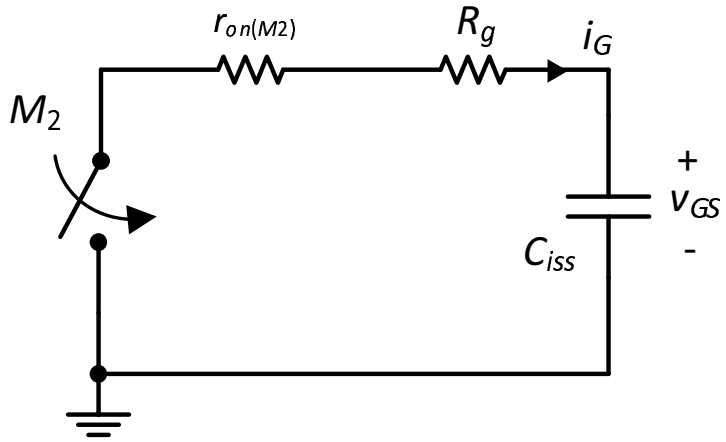

Figure 2.9: Equivalent circuit of conventional gate-drive circuit when M_1 is OFF and M_2 is ON.

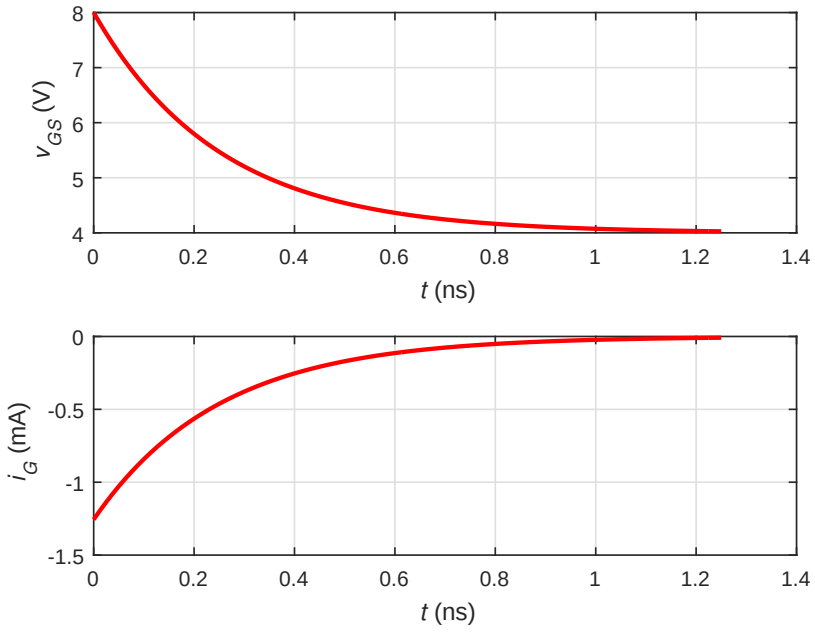

Figure 2.10: Gate-source voltage and gate current of the conventional gate-drive circuit when M_1 is OFF and M_2 is ON.

During the charging period, the gate-source voltage v_{GS} across the input capacitance C_{iss} rises exponentially, and the gate current i_G decreases exponentially with respect to time. The time constant of the RC circuit can be utilized to estimate the speed of the gate driver.

When M_1 is OFF and M_2 is turned ON, the equivalent circuit is shown in Fig. 2.9. The capacitance C_{iss} gets discharge and the gate-source voltage v_{GS} is clamped to the ground as shown in Fig. 2.10. Both the gate current i_G and the gate-source voltage v_{GS} decreases exponentially during the discharging period

$$i_G(t) = -\frac{V_G}{R_g} e^{-t/R_g C_{iss}}, \tag{2.25}$$

and

$$v_{GS}(t) = V_G e^{-t/R_g C_{iss}}. \tag{2.26}$$

During the charging and the discharging period, the total energy, which is supplied by the voltage source V_G, is given as

$$E_s = \int_0^\infty V_G i_G(t)\ dt = V_G \int_0^\infty i_G(t)\ dt = V_G Q_G = C_{iss} V_G^2. \tag{2.27}$$

The gate loss in the equivalent input capacitance C_{iss} can be determined by

$$P_G = \frac{E_c}{T} = f_s E_s = f_s V_G^2 C_{iss}. \tag{2.28}$$

2.5 Summary

The general trend in electronic power conversion systems is to push for higher operating frequencies in order to minimize the passive elements. This can be done through new circuit topologies and new components (materials). Technologies from the GaN could go very well with resonant high-frequency converters. SiC is generally better suited for higher power and voltage levels. Si and GaAs are still used for medium power and voltage levels. In order to make the power converters operate at high frequencies, soft-switching technique is used to eliminate switching losses in the switching devices. The switching performance is based on how quickly voltage changes across the parasitic capacitances of the device. Furthermore, parasitic capacitances play significant roles in high-switching frequency.

Single-Switch topologies, which have a ground-ended transistor, are suitable for implementing and operating at switching frequencies of several MHz. The class-E topology has low complexity compared to others topologies. The main drawback in the class-E is the voltage stress, but it is suited for applications that require low

input voltage. The class Φ_2 inverter has lower voltage stress than other topologies. Moreover, the class Φ_2 has resonate current because of the extra LC circuit, which is used to reduce the peak voltage switch.

The conventional gate driver is the only half bridge that has been used widely in different applications. There are many challenges in implementation, i.e., controlling dead time to a few nanoseconds, high-side (floating) gate driver due to multiple transistors, and synchronizing the low-and high-side signal switches of the gate driver. Thus, the single-referenced topology has a great feature of a simpler gate-drive circuit when it operates at switching frequencies of several megahertz.

3 High-Frequency Single-Switch Gate Driver

3.1 Introduction

This chapter introduces a new single-switch gate-driver circuit to drive a low-side power transistor, which is capable of operating at high frequencies with quick turn ON and turn OFF transitions. The presented topology increases the output voltage with respect to the input voltage. Thus, the new circuit can drive a power MOSFET even when a low voltage is available. The high-frequency operation of the gate driver increases the power losses; an accurate analysis to predict these losses is presented. The new design achieves small passive energy storage components, fast response, and a low design complexity. These advantages make the proposed gate-driver proper for applications that need high-frequency operation of single-switch power converter, such as RF power converters and telecom power supplies.

The objectives of this chapter are: (a) to propose a new topology of single-switch gate-driver circuit based on conventional half-bridge gate driver, suitable to drive power transistors at high frequencies with the capability to rapidly charge and discharge the input capacitance of the driven transistor, (b) to explain and analyze the operation of the proposed gate-driver circuit in detail, (c) to derive design equations for the circuit, (d) to analyze power losses for the gate driver, (e) to present its design procedure, (f) to validate the proposed gate driver through a class-E power inverter, and (g) to provide simulations and experimental results for the gate driver at switching frequency of 20 MHz.

3.2 Circuit Description

The proposed single-switch gate-drive circuit is shown in Fig. 3.1. It consists of a DC input voltage V_I, an inductor L and a switch M. The switch M is an N-channel enhancement-mode power MOSFET and its source is connected to the ground. It is desirable that the drain-source voltage waveform of the driver switch M satisfies ZVS and can be designed for any duty ratio. The inductor L operates as a current source to supply the charge to the input capacitance C_{iss} of the power transistor M_D. The voltage v_{GS} is the gate-source voltage across the input capacitance C_{iss}, which should be charged and discharged. The introduced gate-driver is appropriate

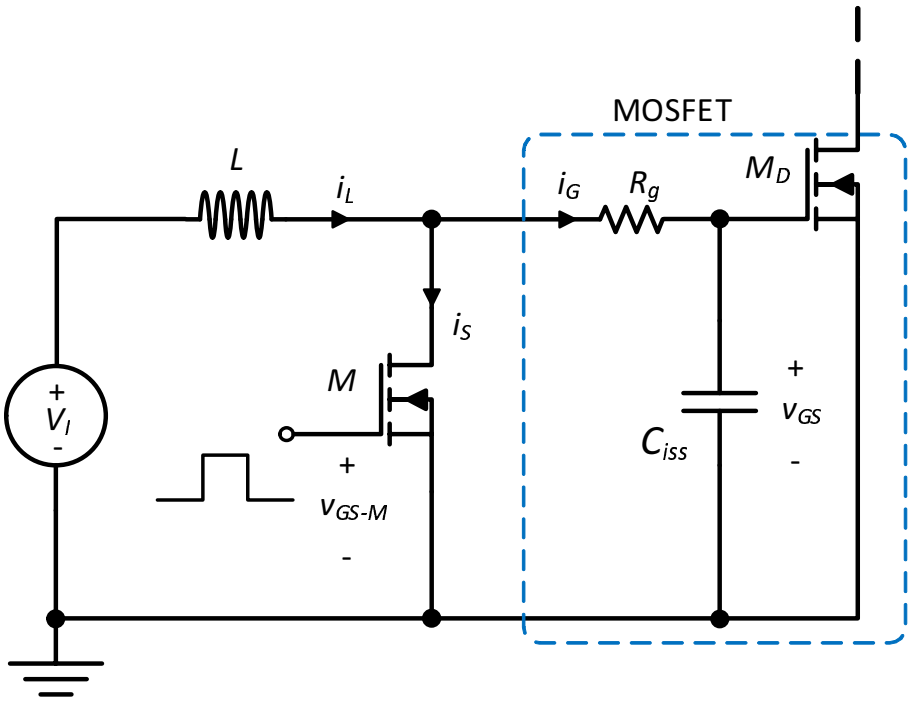

Figure 3.1: Proposed single-switch gate-drive circuit.

for many applications that require an essential gate-source voltage v_{GS} boosting. The proposed circuit charges the input capacitance C_{iss} at higher voltages than input voltage V_I. We focus on identifying characteristic network in the circuit and provide a flexible value of duty cycle to the driven power MOSFET M_D to achieve a rapid turn-ON and turn-OFF of drain-source voltage.

The driving transistor M is operating under ZVS condition to eliminate the switching loss. The switch M can be driven at any duty cycle D, which is determined as switch ON time t_{on} divided by the total period T. The ideal current and voltage waveforms of the proposed gate driver over one period are shown in Fig. 3.2. The analysis of the gate driver is based on the ON-state and the OFF-state of the switch M. For the ON interval, the transistor M exhibits as a switch with a resistance r_{DS}. It operates with an infinite resistance during the OFF interval. The current flowing through the capacitances C_{oss} and C_{iss} forms a soft-switching voltage at both transitions.

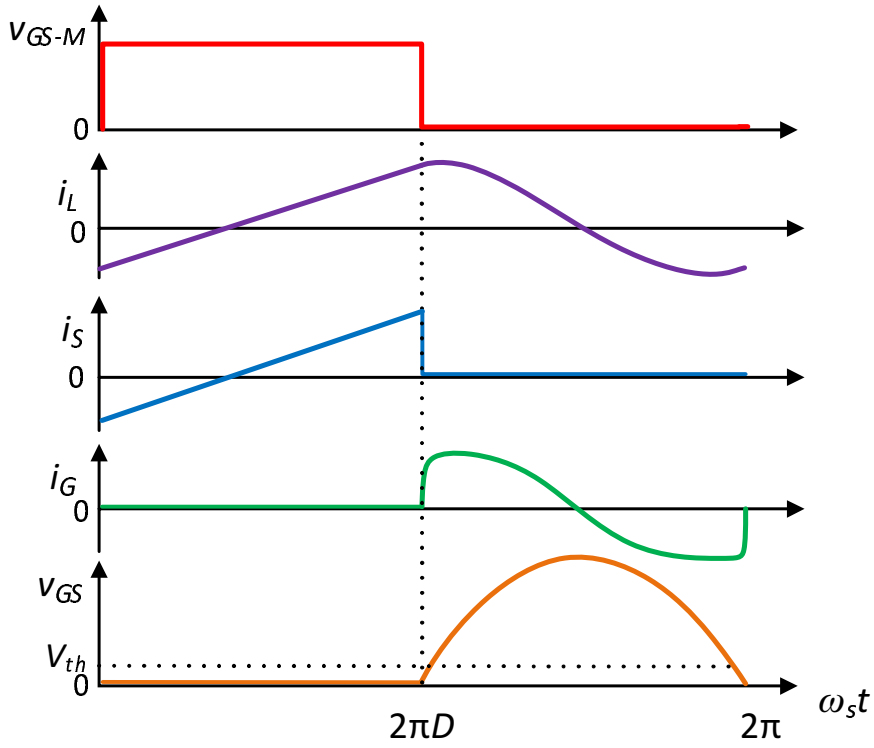

Figure 3.2: Current and voltage waveforms of the proposed gate driver. From top to bottom: drive signal voltage, inductor current, switch current, gate current, and gate-source voltage.

3.2.1 Switch-on $0 < \omega_s t \leq 2\pi D$

In this interval, the power transistor M is ON and its drain-source voltage is zero. The gate-source voltage v_{GS} across the input capacitance C_{iss} is zero because the switch voltage is zero. The equivalent circuit during this interval is shown in Fig. 3.3. The switch current i_S is equal to the inductor current i_L, while the gate current i_G is zero during this interval. Thus, the capacitance C_{iss} is discharged during this interval and the power MOSFET M_D is OFF. When the switch M is ON, the voltage through the inductor v_L is equal to the input voltage V_I. The inductor current i_L rises linearly and its waveform begins from an initial value $i_L(0)$. Its waveform is derived as follows:

$$i_L(t) = \frac{1}{L}\int_0^t v_L(t)dt + i_L(0) = \frac{V_I}{L}t + i_L(0). \tag{3.1}$$

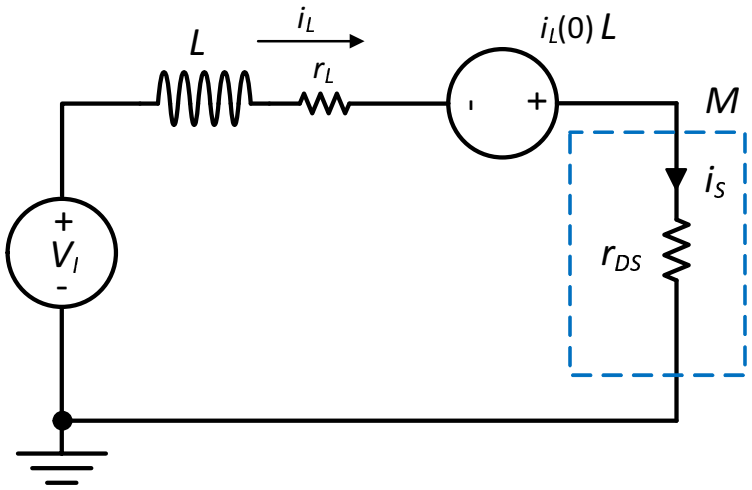

Figure 3.3: Equivalent circuit when the driving switch M is closed.

At the end of this interval, the inductor current i_L at $2\pi D$ is

$$i_L(2\pi D) = \frac{2\pi D V_I}{\omega_s L} + i_L(0), \tag{3.2}$$

where ω_s is the angular switching frequency. Hence, the peak-to-peak inductor current over the interval from 0 to $2\pi D$ is

$$\Delta i_L = i_L(2\pi D) - i_L(0) = \frac{D V_I}{f_s L}, \tag{3.3}$$

where f_s is the switching frequency. From (3.3), the initial inductor current can be expressed as

$$i_L(0) = -\frac{\Delta i_L}{2} = -\frac{D V_I}{2 f_s L} = -\frac{\pi D V_I}{\omega_s L} = -i_L(2\pi D). \tag{3.4}$$

During this interval, the inductor current i_L is flowing through the switch M. In other words, the switch M supports a low-impedance path to the ground. Thus, the switch current i_S is

$$i_S(t) = \begin{cases} \frac{V_I}{L} t - \frac{D V_I}{2 f_s L} & 0 < \omega_s t \le 2\pi D \\ 0 & 2\pi D < \omega_s t \le 2\pi. \end{cases} \tag{3.5}$$

3.2.2 Switch-off $2\pi D < \omega_s t \le 2\pi$

In this interval, the power transistor M is OFF and its current i_S is zero. Therefore, the gate-source voltage v_{GS} of the power switch M_D increases from zero to a maximum

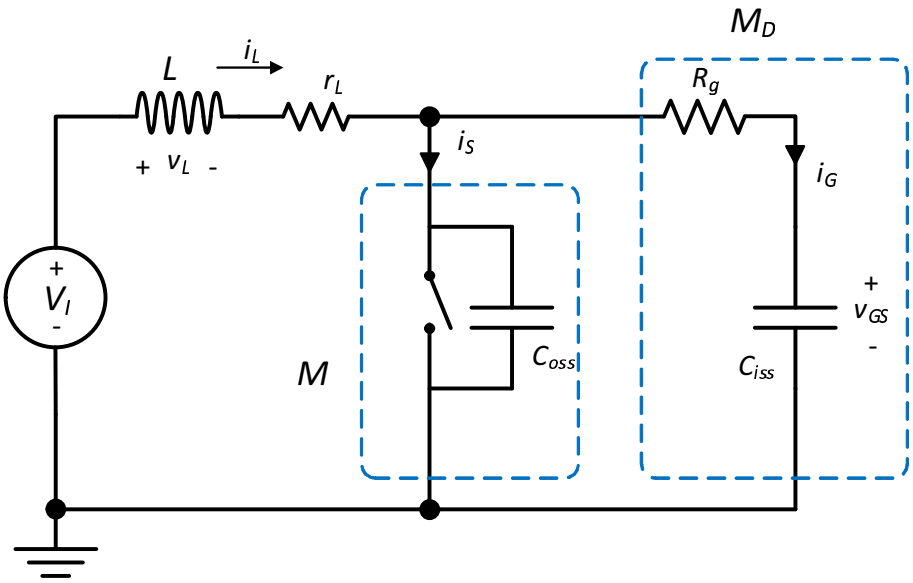

Figure 3.4: Equivalent circuit when the driving switch M is opened.

value and then decreases to zero, as shown in Fig. 3.2. The equivalent circuit of the gate driver relevant to this interval is shown in Fig. 3.4. The inductor operates as a current source that supplies the sufficient charge to the driven transistor input capacitance C_{iss}. In this study, it is assumed that both the capacitances C_{iss} and C_{oss} are linear. The equivalent capacitance C is equal to the output capacitance C_{oss} of the driving M and the input capacitance C_{iss} of the driven transistor M_D

$$C = C_{oss} + C_{iss}. \tag{3.6}$$

The total resistance R is the sum of resonant inductor equivalent series resistance r_L and the internal gate resistance R_g of the driven transistor M_D

$$R = R_g + r_L. \tag{3.7}$$

During this interval, the gate current i_G is equal to the inductor current i_L. By using s-domain analysis, the inductor current can be expressed as

$$i_L(s) = \left[\frac{V_I}{L}\frac{1}{s^2 + \frac{R}{L}s + \frac{1}{LC}} + \frac{i_L(0)s}{s^2 + \frac{R}{L}s + \frac{1}{LC}}\right] e^{-st_1}, \tag{3.8}$$

where $t_1 = 2\pi D/\omega_s$. The inductor current time domain expression can be obtained as follows:

$$i_L(\omega_d t) = L^{-1}\{i_L(s)\} \tag{3.9}$$

$$= e^{-\alpha t}\left[\frac{V_I}{\omega_d L}\sin\omega_d\left(t-\frac{2\pi D}{\omega_s}\right)+i_L(0)\cos\omega_d\left(t-\frac{2\pi D}{\omega_s}\right)-i_L(0)\frac{\alpha}{\omega_d}\sin\omega_d\left(t-\frac{2\pi D}{\omega_s}\right)\right],$$

where

$$\omega_o=\frac{1}{\sqrt{LC}},\ \omega_d=\sqrt{\omega_o^2-\alpha^2}=\omega_o\sqrt{1-\frac{1}{4Q^2}}, \tag{3.10}$$

and

$$\gamma=\frac{\omega_d}{\omega_o},\ Q=\frac{Z_o}{R}=\frac{\omega_o L}{R}=\frac{1}{\omega_o CR},\ \alpha=\frac{R}{2L}. \tag{3.11}$$

The switching angular frequency ω_s does not depend on the resonant circuit components and is an independent variable. It can be related to resonant angular frequency ω_o and the system natural frequency ω_d as follows:

$$\omega_s=a\ \omega_o=\frac{a}{\gamma}\omega_d, \tag{3.12}$$

where a is the frequency ratio. Since the inductor current i_L is equal to the gate current in this interval, the gate current can be expressed as

$$i_G(\omega_d t)=e^{-\frac{R}{2Z_o}(\omega_d t)}\left[\left(\frac{V_I}{\omega_d L}-\frac{R}{Z_o}\right)\sin\frac{\gamma}{a}\left(\omega_s t-2\pi D\right)+i_L(2\pi D)\cos\frac{\gamma}{a}\left(\omega_s t-2\pi D\right)\right]. \tag{3.13}$$

From (3.4),

$$i_L(2\pi D)=\frac{\pi D V_I}{\omega_s L}=\frac{\pi D V_I}{aZ_o}. \tag{3.14}$$

According to (3.13) and (3.14), the gate current is

$$i_G(\omega_d t)=e^{-\frac{R}{2Z_o}(\omega_d t)}\left[\left(\frac{V_I}{\omega_d L}-\frac{R}{Z_o}\right)\sin\frac{\gamma}{a}\left(\omega_s t-2\pi D\right)+\frac{\pi D V_I}{aZ_o}\cos\frac{\gamma}{a}\left(\omega_s t-2\pi D\right)\right]. \tag{3.15}$$

If $R << 2Z_o$, then $\omega_d=\omega_o$, $\gamma\approx 1$, and $Q >> 1$, the above equation is simplified to the form

$$i_G(\omega_s t)=\frac{V_I}{Z_o}\left[\sin\frac{1}{a}(\omega_s t-2\pi D)+\frac{\pi D}{a}\cos\frac{1}{a}\left(\omega_s t-2\pi D\right)\right]. \tag{3.16}$$

Fig. 3.5 shows the waveform of the gate current i_G at duty cycle $D=0.5$. Fig. 3.6 shows the normalized gate current through the total capacitance C for different values of duty cycle D. During switching transient, the MOSFET is strongly influenced by the capacitances of the device. The gate-drain capacitance C_{gd}, which is connected between the input (gate) and the output (drain) of the MOSFET, is an important

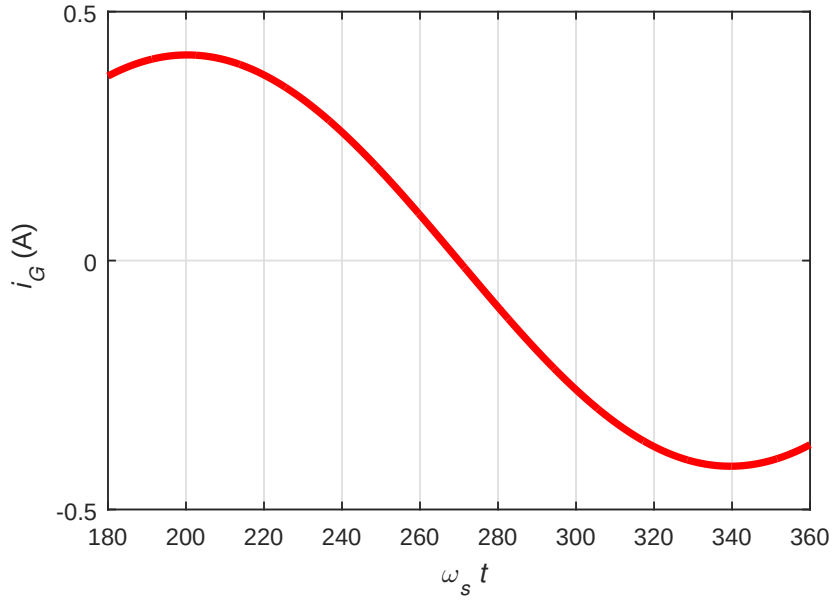

Figure 3.5: Gate current waveform i_G at $D = 0.5$.

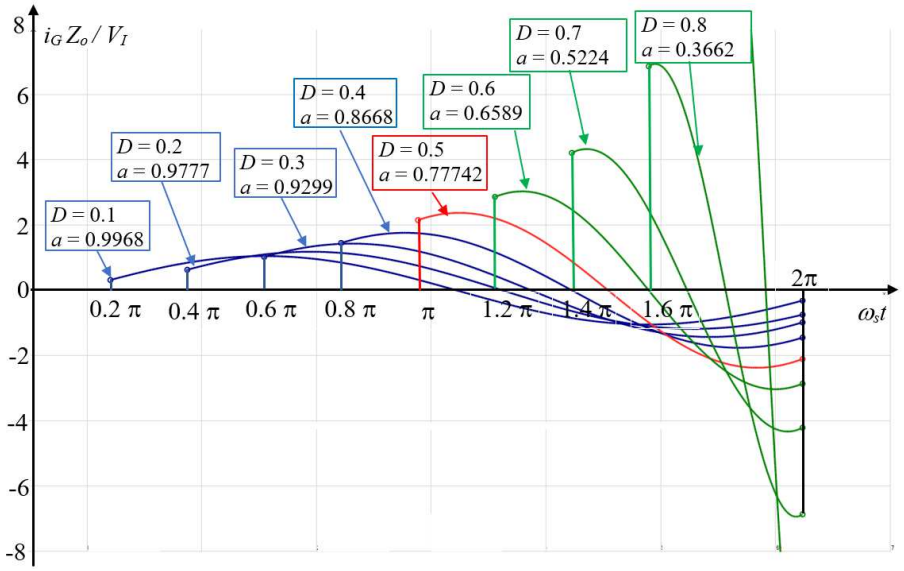

Figure 3.6: Normalized gate current waveforms for different values of D.

parameter in the MOSFET. During the turn ON transition of the power switch M_D, the gate current i_G has to supply a total charge $Q_g = Q_{gs} + Q_{gd}$ to charge the gate-source capacitance C_{gs} and gate-drain capacitance C_{gd}, respectively. Fig. 3.7 shows the schematic and the gate charge behavior of the driven transistor M_D. The gate-source voltage v_{GS} begins to increase when the gate current i_G supplies the charge to

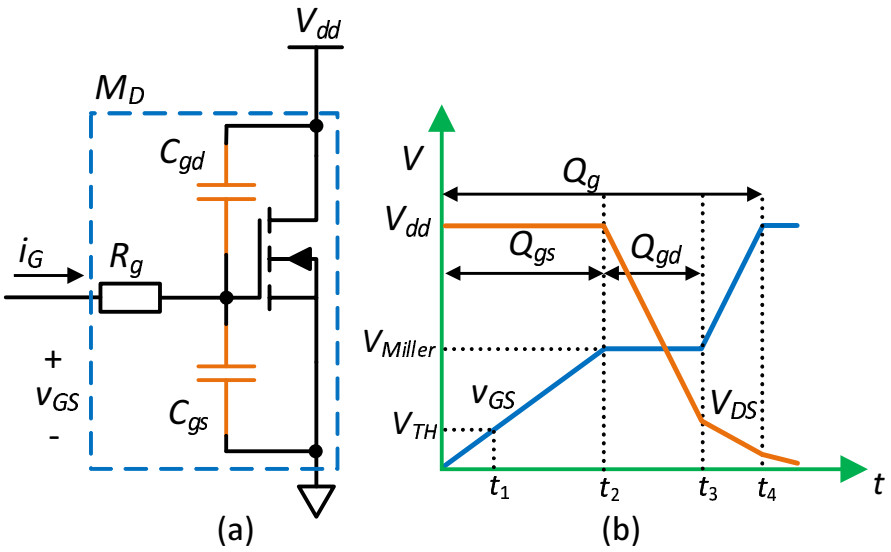

Figure 3.7: (a) Schematic of a MOSFET. (b) Characteristics of gate-charge for MOSFET.

the transistor input capacitance C_{iss}. when the drain-source voltage V_{DS} is zero, the input capacitance C_{iss} is

$$C_{iss} = C_{gs} + C_{gd}. \tag{3.17}$$

An important effect that should be considered during the turn-ON transition is Miller's effect. When the drain-source voltage decreases and the gate-source voltage v_{GS} increases of the driven transistor M_D, the transistor input capacitance C_{iss} is significantly influenced due to the Miller's effect. Therefore, the total input capacitance C_{in} with Miller's effect can be expressed as

$$C_{in} = C_{gs} + (1 - A_v)C_{gd}, \tag{3.18}$$

where A_v is instantaneous voltage gain when the drain-source voltage V_{DS} decreases

$$Av = \frac{\Delta v_{DS}}{\Delta v_{GS}}. \tag{3.19}$$

In this interval, the initial value of the voltage across the equivalent capacitance C is zero at $\omega_s t = 2\pi D$. From (3.15), the gate-source voltage v_{GS} can be obtained as

$$v_{GS}(\omega_s t) = \frac{1}{\omega_s C} \int_{2\pi D}^{\omega_s t} i_G(\omega_s t)\ d(\omega_s t) \tag{3.20}$$

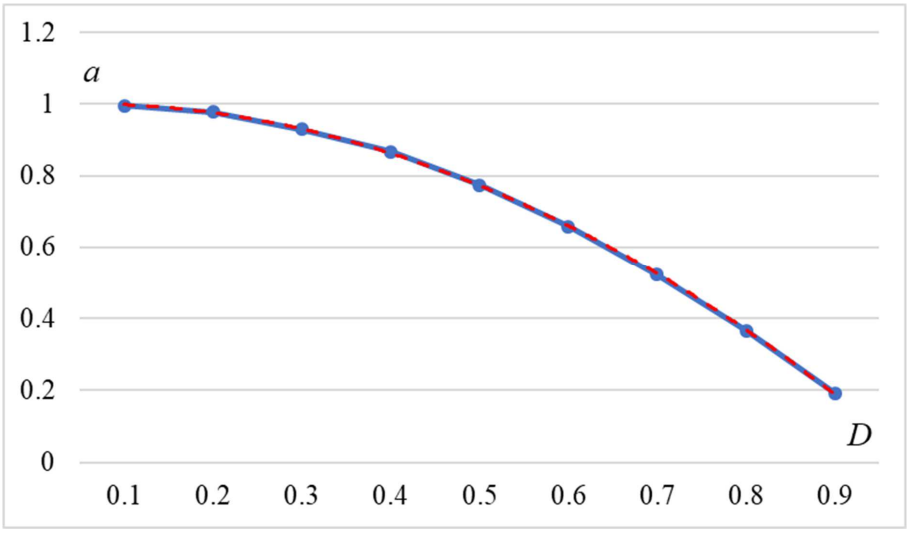

Figure 3.8: Approximation of $a = f(D)$ by polynomial (3.20) according to the values given in Table 3.1.

Table 3.1: Duty cycle D versus frequency ratio a.

D	$a = f_s/f_o$
0.1	0.9968
0.2	0.9777
0.3	0.9299
0.4	0.8668
0.5	0.7742
0.6	0.6589
0.7	0.5224
0.8	0.3662
0.9	0.1917

$$= V_I \left\{ \left(1 - \frac{R}{Z_o}\frac{\pi D}{a}\right)\left[1 - \cos\frac{1}{a}(\omega_s t - 2\pi D)\right] + \frac{\pi D}{a}\sin\frac{1}{a}(\omega_s t - 2\pi D) \right\}.$$

If R is small and $R << Z_o$, (3.20) can be simplified to

$$v_{GS}(\omega_s t) = V_I\left[1 - \cos\frac{1}{a}(\omega_s t - 2\pi D) + \frac{\pi D}{a}\sin\frac{1}{a}(\omega_s t - 2\pi D)\right]. \tag{3.21}$$

The ZVS condition $v_{GS}(2\pi) = 0$ in (3.21) yields the relationship between a and D

$$1 - \cos\frac{1}{a}2\pi(1-D) + \frac{\pi D}{a}\sin\frac{1}{a}2\pi(1-D) = 0. \tag{3.22}$$

According to (3.22), Fig.3.8 shows the duty cycle D is a function of the duty ratio a. The solution of this transcendental equation produces $a = 0.7742$ for $D = 0.5$.

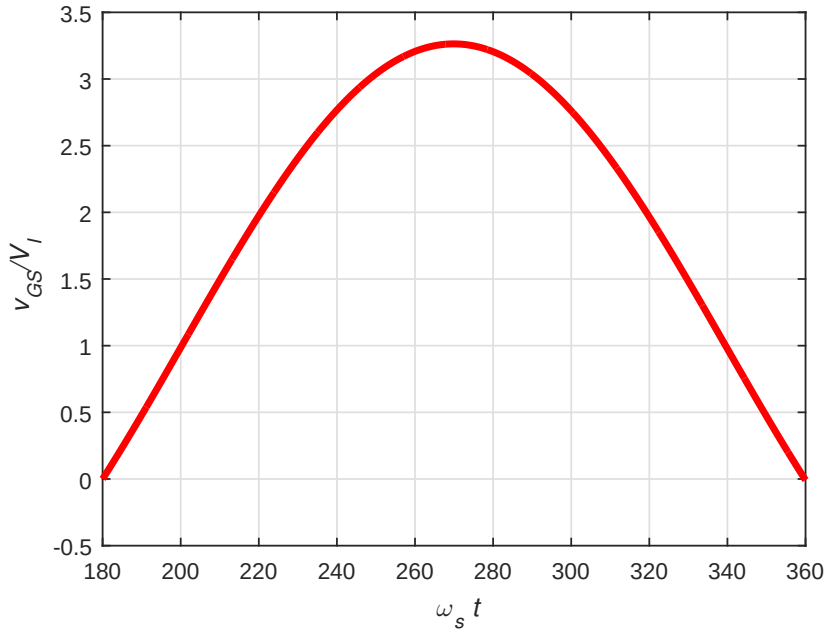

Figure 3.9: Normalized gate-source voltage waveform v_{GS}/V_I at $D = 0.5$.

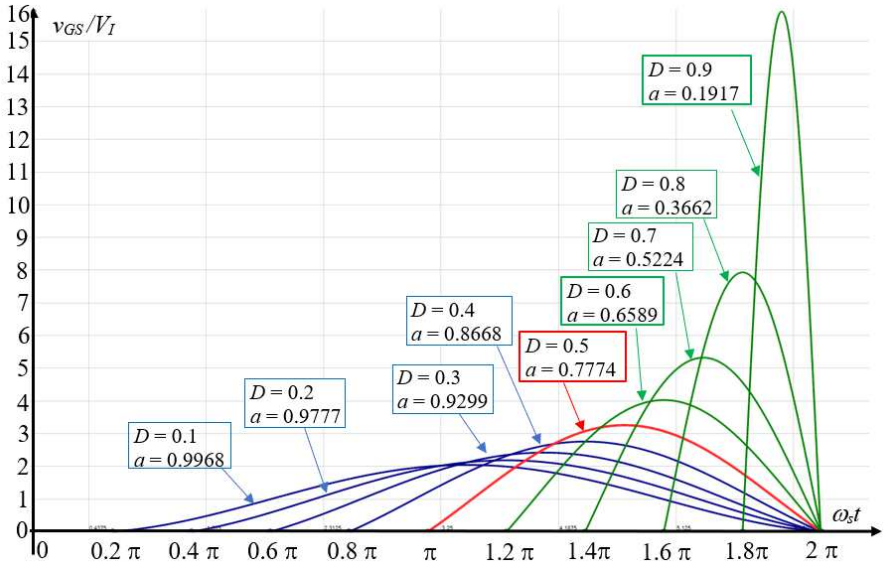

Figure 3.10: Normalized gate-source voltage waveforms for different values of D.

Table 3.1 shows the other combinations of D values with respect to the frequency ratio a. The set of these values are approximated by a second-order polynomial

$$a = -0.0112D^2 - 0.0108D + 0.9991. \tag{3.23}$$

The normalized gate-source voltage v_{GS}/V_I at duty cycle $D = 0.5$ is depicted in Fig. 3.9. Fig. 3.10 shows the normalized gate-source voltage v_{GS}/V_I for values of D in the range $(0.1 - 0.9)$. It is clear that the ZVS condition can be satisfied at different values of D.

3.2.3 Voltage and Current Stresses

The maximum value of v_{GS} occurs at $\omega_s t_v = 4.6945$ rad $= 269.11°$ and its value is $V_{GSmax}/V_I = 3.2629$ for $D = 0.5$. The maximum value of gate-source voltage V_{GSmax} depends on the duty cycle D. Fig.3.11 shows the maximum values of normalized gate-source voltage for different values of D. Table 3.2 gives the list of normalized

Table 3.2: $\omega_s t_v$ and maximum values of normalized V_{GSmax}/V_I.

D	$\omega_s t_v$ (deg.)	V_{GSmax}/V_I
0.1	198.08	2.0483
0.2	219.56	2.1886
0.3	233.05	2.4238
0.4	252.12	2.7611
0.5	268.98	3.2629
0.6	288.13	4.0305
0.7	306.14	5.3267
0.8	324.15	7.9356
0.9	342.95	15.9148

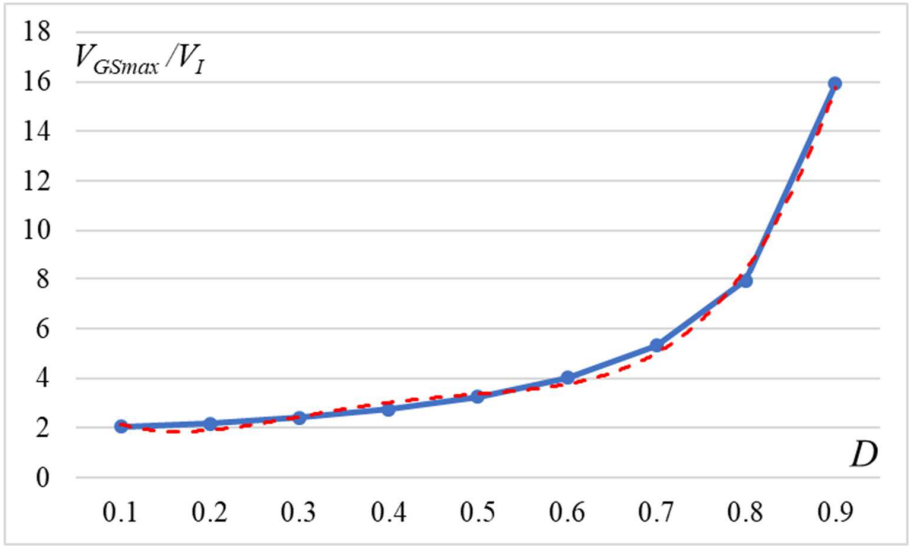

Figure 3.11: Normalized maximum gate-source voltage V_{GSmax}/V_I as a function of D.

V_{GSmax} with respect to various angles. The set of these values are represented by a polynomial forth-order function as follows

$$\frac{V_{GSmax}}{V_I}(D) = 0.0214D^4 - 0.34D^3 - 3.8692D + 4.4498. \tag{3.24}$$

The maximum switch current can be approximated by

$$I_{Smax} = i_L(2\pi D) = \frac{DV_I}{f_s L}. \tag{3.25}$$

3.3 Analysis of Power Losses

In this section, the loss analysis of the proposed gate driver is provided. Since the power MOSFET M is switched under ZVS condition, the switching loss is eliminated. The total power loss in the proposed gate driver includes inductor loss, on-resistance and gate losses of the switch M, and gate resistance of the power MOSFET M_D. Power MOSFETs are appropriate for high frequencies due to their power rating and dynamic properties; however, switching and gate losses are dominant in the megahertz range [34], [43]. Moreover, the on-resistances of the MOSFETs can cause a significant conduction loss in the circuit. Therefore, the following design considerations are applied to determine the total loss in the proposed gate-drive circuit. The conduction loss is determined by calculating the root-mean-square (rms) current $I_{S(rms)}$ of the switch current i_S. By using (3.5), the rms current $I_{S(rms)}$ of the switch M is

$$I_{S(rms)} = \sqrt{\frac{1}{T}\int_0^{DT} i_S^2(t)\ dt} = \frac{D\sqrt{D}V_I}{\sqrt{12}f_s L}. \tag{3.26}$$

Hence, the conduction power loss in the switch M is

$$P_{r_{DS}} = I_{S(rms)}^2 r_{DS} = \frac{D}{12}\left(\frac{V_I D}{f_s L}\right)^2 r_{DS} = \frac{\pi^2 D^3 V_I^2}{3a^2 Z_o^2} r_{DS}. \tag{3.27}$$

According to (3.16), the rms value of the gate current i_G is

$$I_{G(rms)} = \sqrt{\frac{1}{2\pi}\int_{2\pi D}^{2\pi} i_G^2(\omega_s t)\ d(\omega_s t)} \tag{3.28}$$

$$= \frac{V_I}{Z_o}\left\{\left(\frac{1-D}{2}\right)\left[1+\frac{\pi^2 D^2}{a^2}\right]+\left(\frac{\pi^2 D^2}{a^2}-1\right)\frac{a}{8\pi}\sin\frac{4\pi}{a}(1-D)+\frac{D}{4}\left[1-\cos\frac{4\pi}{a}(1-D)\right]\right\}^{1/2}.$$

The conduction power loss in the gate resistance R_g of the driven power MOSEFT is

$$P_{Rg} = I^2_{G(rms)} R_g. \tag{3.29}$$

Since air-core inductor is used, the inductor core power losses are negligible [44]. The rms inductor current is

$$I_{L(rms)} = \sqrt{I^2_{S(rms)} + I^2_{G(rms)}}. \tag{3.30}$$

The inductor conduction loss is

$$P_{r_L} = I^2_{L(rms)} r_L. \tag{3.31}$$

From the above equations of loss analysis, we determine the total dissipative power conduction loss P_{LS} in the gate driver as follow:

$$P_{LS} = P_{r_L} + P_{Rg} + P_{r_{DS}}. \tag{3.32}$$

If the input capacitance of the switch M is C_{iss}, the power gate loss in the switch M at switching frequency f_s is

$$P_g = f_s C_{iss} V^2_{GS(pp)}, \tag{3.33}$$

where $V_{GS(pp)}$ is the maximum magnitude of the drive voltage v_{GS-M}.

3.4 Design of Gate Driver

The gate driver is designed for the switching frequency $f_s = 20$ MHz. The design is applied to determine the following design parameters: the resonant inductor L, the equivalent capacitance C, the resonant frequency f_o, the characteristic impedance Z_o, and the quality factor Q. In this study, the optimal design of the proposed gate driver is applied to class-E power inverter [1]. The design procedure is used to drive the power transistor M_D of the class-E inverter. The peak value of the gate-source voltage v_{GS} depends on the duty cycle D. Therefore, the input voltage of the gate driver depends on the characteristic of the power transistor. It is important to select a power MOSFET with a driving voltage rating that can be proper to the driven voltage v_{GS}. The supply voltage V_I was selected to be 4 V. The driving and driven transistors were VRF148A, whose data are listed in Table 3.3. From Table 3.1, the

value of frequency ratio $a = 0.7742$ at $D = 0.5$. According to (3.12), the resonant frequency can be determined

$$f_o = \frac{f_s}{a} = \frac{20 \times 10^6}{0.7742} = 25.833 \text{ MHz}. \tag{3.34}$$

When the switch M is OFF, the resonant circuit consists of the inductor L, the output capacitance C_{oss} of the switch M and the input capacitance C_{in} of the switch M_D. According to datasheet, the values of these capacitances are given in Table 3.3. The gate-source capacitance of the driven switch M_D can be found as

$$C_{gs} = C_{iss} - C_{rss} = 160 - 2.6 = 157.4 \text{ pF}. \tag{3.35}$$

In class-E inverter, the drain-source voltage v_{DS} of the driven switch M_D is 35 V when the DC power supply voltage V_{in} of the class-E is 10 V. The gate-source voltage, which is supplied by the proposed gate driver, is 13.05 V. Therefore, the voltage gain A_v of the switch M_D is determined as

$$A_v = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{V_{DS_2} - V_{DS_1}}{V_{GS_2} - V_{GS_1}} = \frac{0 - 35}{13.05 - 0} = -2.682. \tag{3.36}$$

Thus, the total input capacitance C_{in} with the Miller's effect of the driven transistor M_D is given by

$$C_{in} = C_{gs} + (1 - A_v)C_{gd} = 157.4 + (1 + 2.682) \times 2.6 = 167 \text{ pF}. \tag{3.37}$$

Since the output capacitance C_{oss} of the switch M is highly nonlinear, it is taken into account in the analysis [45]. The equivalent value the output capacitance C_{oss} can be determined at drain-source voltage $V_{DS} = V_{GSmax}/2 = 13.05/2 = 6.525$ V.

$$C_{oss} = \frac{C_{J0}}{\left(1 + \frac{V_{DS}}{V_{bi}}\right)^m} = \frac{228}{\left(1 + \frac{6.525}{0.7}\right)^{0.42}} = 85 \text{ pF}. \tag{3.38}$$

Fig. 3.12 shows the value of output capacitance C_{oss} at $V_{DS} = 6.525$ V. Fig. 3.13 shows the parasitic capacitances, gate-source voltage, and drain-source voltage of the driven switch M_D. Therefore, the equivalent capacitance C can be found

$$C = C_{oss} + C_{in} = 85 + 167 = 252 \text{ pF}. \tag{3.39}$$

From (3.10), the resonant inductor L can be determined

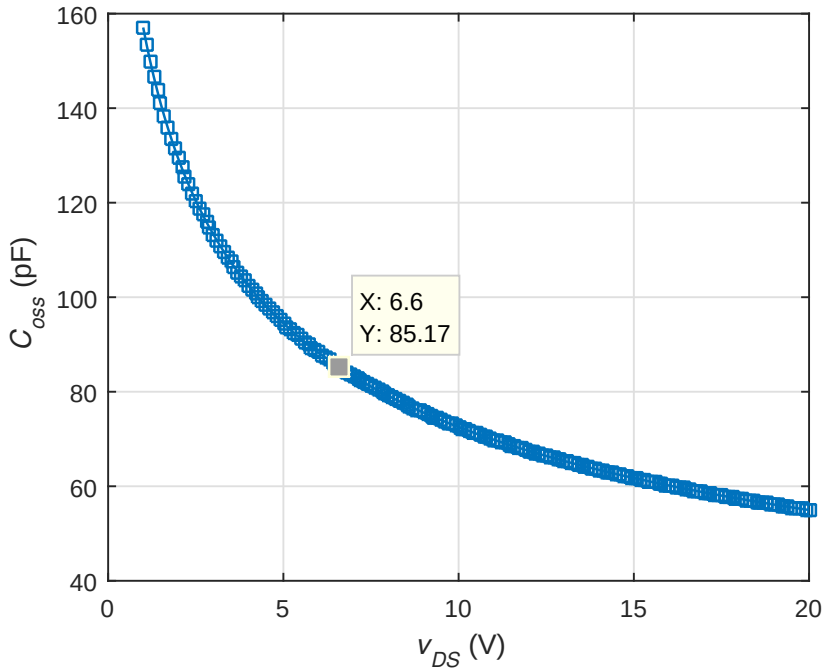

Figure 3.12: The equivalent output capacitance C_{oss} at $V_{DS} = 6.6$ V.

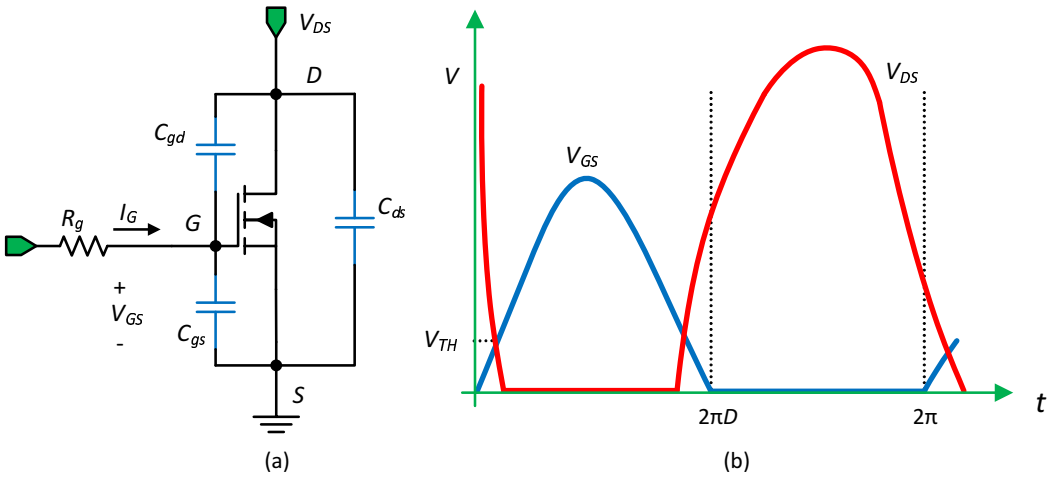

Figure 3.13: (a) Driven transistor (M_D). (b) Drain-source and gate-source voltages for the power switch (M_D).

$$L = \frac{1}{C\omega_o^2} = \frac{1}{252 \times 10^{-12} \times (162.23 \times 10^6)^2} = 150 \text{ nH}. \tag{3.40}$$

The characteristic impedance of the resonant circuit is

$$Z_o = \sqrt{\frac{L}{C}} = \sqrt{\frac{150 \times 10^{-9}}{252 \times 10^{-12}}} = 24.4\ \Omega. \tag{3.41}$$

The quality factor Q of the resonant gate-driver depends on the characteristic impedance Z_o and the parasitic resistances r_L and R_g

$$Q = \frac{\omega_o L}{r_L + R_g} = \frac{162.23 \times 10^6 \times 150 \times 10^{-9}}{0.211 + 0.3} = 47.62. \tag{3.42}$$

When the input voltage $V_I = 4$ V is applied, the maximum value of gate-source voltage V_{GSmax} at $D = 0.5$ is

$$V_{GSmax} = (V_{GSmax}/V_I) \times V_I = 3.2629 \times 4 = 13.05 \text{ V}. \tag{3.43}$$

The maximum switch current is

$$I_{Smax} = \frac{DV_I}{f_s L} = \frac{0.5 \times 4}{20 \times 10^6 \times 150 \times 10^{-9}} = 0.66 \text{ A}. \tag{3.44}$$

The conduction power loss in the switch M at $D = 0.5$ is

$$P_{r_{DS}} = \frac{D}{12}\left(\frac{V_I D}{f_s L}\right)^2 r_{DS} = \frac{0.5}{12}\left(\frac{2}{3}\right)^2 1.2 = 22.22 \text{ mW}. \tag{3.45}$$

From (3.28), the rms gate current is $I_{G(rms)} = 0.202$ A, yielding the loss dissipation in the internal gate resistance of the power switch M_D

$$P_{Rg} = I_{G(rms)}^2 R_g = 0.202^2 \times 0.3 = 12.24 \text{ mW}. \tag{3.46}$$

The rms inductor current $I_{L(rms)}$ can be obtained from the rms switch current $I_{S(rms)}$ and the rms gate current $I_{G(rms)}$. The conduction power loss in the inductor L is

$$P_{r_L} = I_{L(rms)}^2 r_L = \left[I_{S(rms)}^2 + I_{G(rms)}^2\right] r_L \tag{3.47}$$

$$= \left(0.136^2 + 0.202^2\right) \times 0.211 = 12.5 \text{ mW}.$$

From (3.31), the total conduction loss of the proposed gate driver is

$$P_{LS} = P_{r_{DS}} + P_{Rg} + P_{r_L} = 22.22 + 12.24 + 12.5 = 46.96 \text{ mW}. \tag{3.48}$$

Since $P_I = P_{LS}$, the input current I_I can be calculated

$$I_I = \frac{P_I}{V_I} = \frac{46.96 \times 10^{-3}}{4} = 11.74 \text{ mA}. \tag{3.49}$$

Table 3.3: List of components for gate driver at $f_s = 20$ MHz.

Components	Value
L, r_L	150 nH, 0.211 Ω
Si MOSFET M, M_D	VRF148A $C_{iss} = 160$ pF, $C_{oss} = 85$ pF, $C_{rss} = 2.6$ pF $V_{DS} = 170$ V, $I_{DS} = 6$ A, $R_g = 0.3$ Ω $Q_g = 3.2$ nC, $r_{DS} = 1.2$ Ω

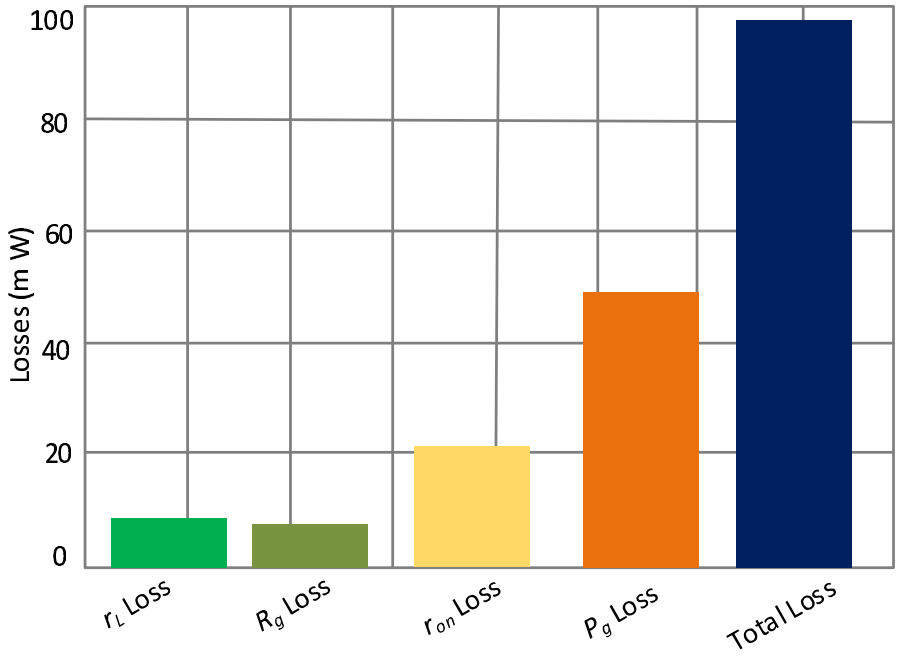

Figure 3.14: Calculated losses at $V_I = 4$ V and $f_s = 20$ MHz switching frequency.

The peak value of gate-source square voltage waveform v_{GS-M} of the driving transistor M was 4 V for $D = 0.5$. The power gate loss in the switch M is calculated as

$$P_g = f_s C_{iss} V_{GS(pp)}^2 = 20 \times 10^6 \times 160 \times 10^{-12} \times 4^2 = 51.2 \text{ mW}. \tag{3.50}$$

According to above analysis, the power losses of the proposed gate driver are shown in Fig. 3.14 at 20 MHz switching frequency. It can be noticed that the gate loss was dominant due to high switching frequency of the power switch M. The specifications of the proposed gate-driver components are given in Table 3.3.

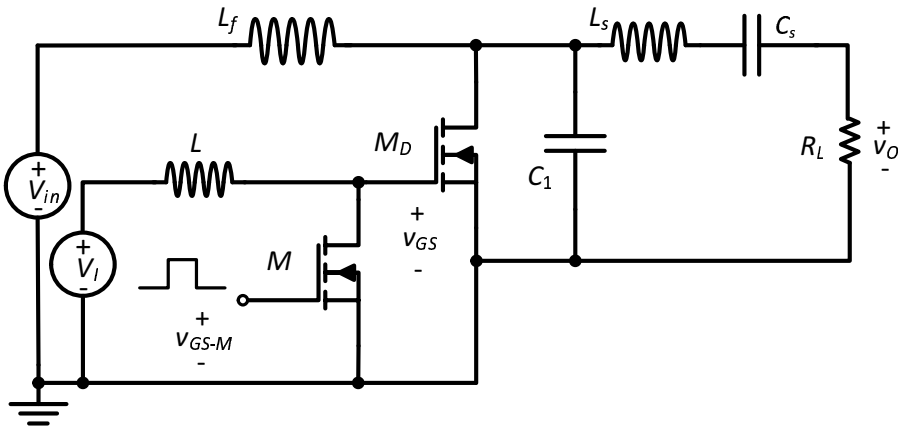

Figure 3.15: Class-E inverter in [1] by using proposed gate-driver at $f_s = 20$ MHz.

Table 3.4: Class-E Inverter Parameters.

Parameter	Value	Parameter	Value
Input voltage V_{in}	10 V	Quality factor Q_L	8
Output Power P_O	10 W	inductor L_f	2 μH
Duty Cycle D	50%	Inductor L_s	0.367 μH
Switching frequency f_s	20 MHz	Capacitor C_s	200 pF
Gate-source voltage v_{GS}	13	Capacitor C_1	160 pF

3.5 Design Gate Driver for Class-E Power Inverter

The presented approach can be used for the class-E inverter to drive the swish M_D as depicted in Fig. 3.15. The ZVS operation at the switch M_D can be achieved when the duty cycle is $D = 0.5$, the quality factor of the filter LC is high, and the output load at the resistance R_L is optimum [21], [22]. The load resistance R_L is [1]

$$R_L = \frac{8}{\pi^2 + 4}\frac{V_{in}^2}{P_o} = 0.5768 \times \frac{10^2}{10} = 5.77\ \Omega, \tag{3.51}$$

and the desired chock inductance L_f is

$$L_f = 2\left(\frac{\pi^2}{4} + 1\right)\frac{R_L}{f_s} = 6.93 \times \frac{5.77}{20 \times 10^6} = 2\ \mu\text{H}. \tag{3.52}$$

The parameters of the class-E are shown in Table 3.4. Since the class-E has single switch and its source is connected in the ground, the proposed gate driver is suited to drive the single switch of class-E inverter.

3.6 Simulation and Experimental Results

3.6.1 Simulations

Based on the circuit operation and design approach presented in Sections 3.2, the gate driver was designed, and tested to verify the theoretical predictions. The SaberRD software was used to simulate the proposed gate-driver at a constant 20 MHz switching frequency. The input voltage V_I was 4 V. The class-E inverter was simulated at 20 MHz and its switch M_D was driven by the proposed circuit. A Si power MOSFET was utilized in the proposed gate-driver and class-E inverter. To achieve ZVS operation at turn-ON transition of the driving transistor M, the inductance L was reduced from 150 to 142 nH. The magnitude of the gate-source voltage depends on the duty cycle D. The maximum value of gate-source voltage V_{GSmax} was 13 V at $D = 0.5$.

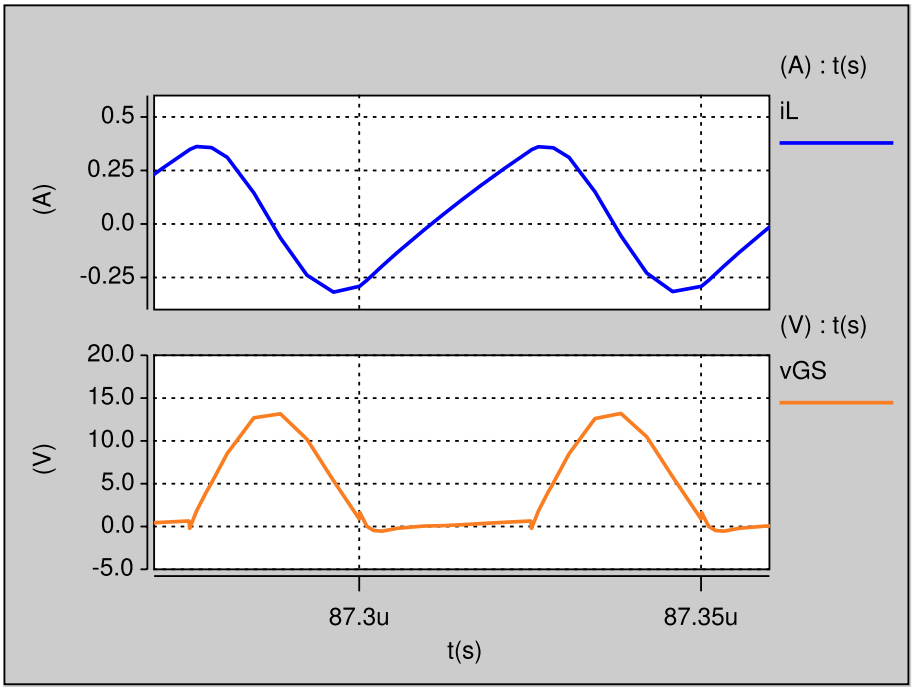

Figure 3.16: Simulated waveforms of inductor current i_L and gate-source voltage v_{GS}.

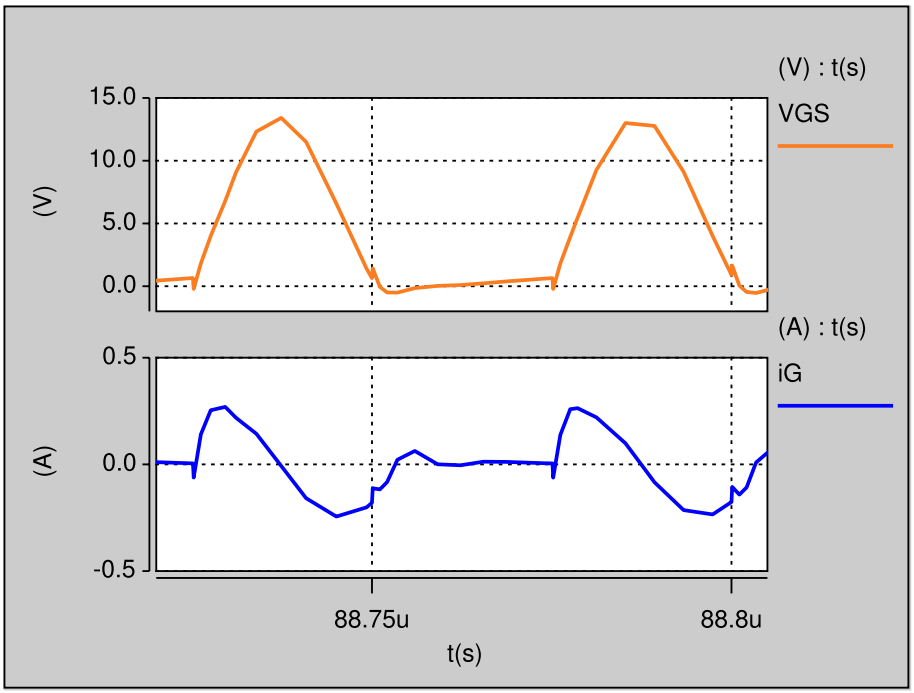

Figure 3.17: Simulated waveforms of gate-source voltage v_{GS} and gate current i_G of the driven power MOSFET M_D.

Fig. 3.16 shows the inductor current i_L and gate-source voltage v_{GS} waveforms for the entire cycle. It is clear that the inductor current rises linearly and starts from an initial value when the switch M is ON. As the switch M is OFF, the resonance occurs between the inductor L and the equivalent capacitance C. The gate-source voltage v_{GS} and gate-current i_G waveforms of the driven power transistor M_D were captured during the turn-ON and turn-OFF transitions as shown in Fig. 3.17. It can be noticed that the power transistor input capacitance C_{iss} is charged/discharged when the switch M is OFF. A quick transition time is observed, indicating that high-speed switching is achieved.

The gate-source voltage v_{GS}, the switch voltage v_S, and the switch current i_S of the driven switch M_D are shown in Fig. 3.18. It can be noticed that the ZVS operations is achieved in the switch M_D. The output voltage v_O, the output current of the class-E inverter are shown in Fig. 3.19. The performance of the new gate driver proves many features that the topology has over conventional designs. Particularly, it proves high-speed transient response, small storage components, and low-design complexity for high frequency operation.

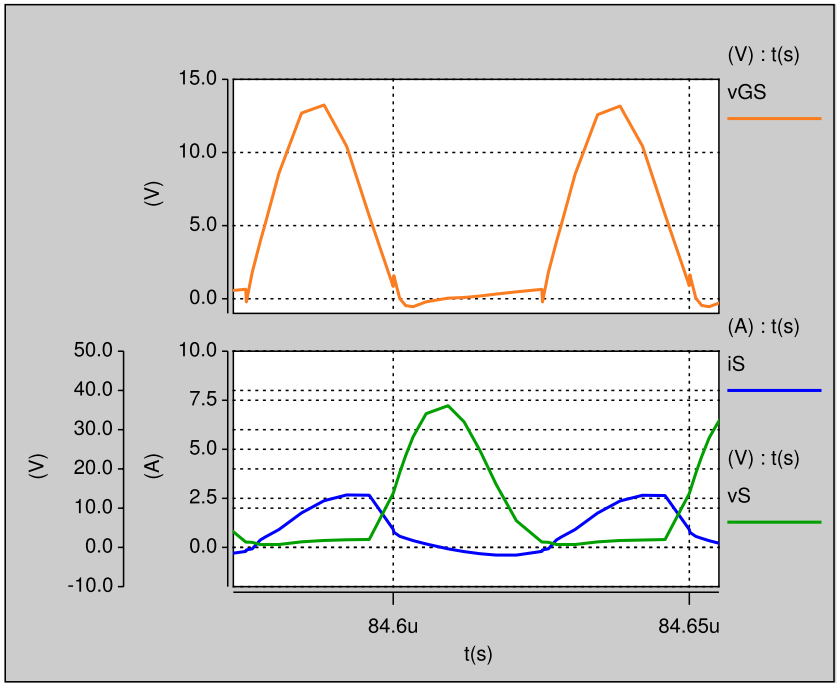

Figure 3.18: Simulated waveforms of gate-source voltage v_{GS}, switch voltage v_S, and switch current i_S of class-E inverter.

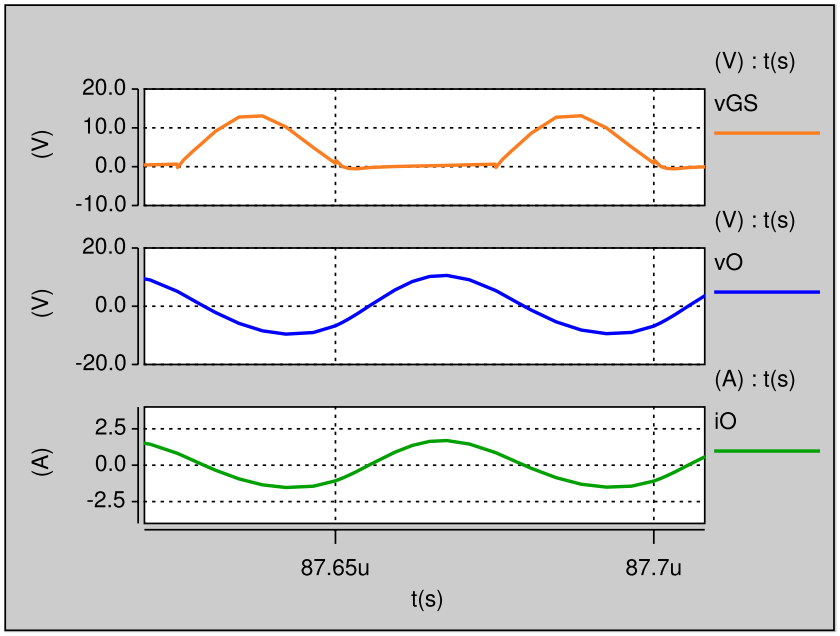

Figure 3.19: Simulated waveforms of gate-source voltage v_{GS}, output current i_O, and output voltage v_O of the class-E inverter.

3.6.2 Experimental Results

A VRF148A MOSFET from Microsemi Technologies was used as the switching device in the circuit. It is driven by the proposed gate driver, enabling the duty cycle to be constant at $D = 0.5$ with fixed switching frequency $f_s = 20$ MHz. The dc supply voltage was applied through the inductor L. Fig. 3.20 shows the experimentally obtained waveform of the inductor current i_L and the gate-source voltage v_{GS}. It can be noticed that the maximum value of gate-source voltage V_{GSmax} was 11 V at $D = 0.5$, safely within the manufacturer's rating of 40 V ($11/40 = 0.275$). The gate-source voltage v_{GS} and and gate current i_G waveforms of the driven transistor M_D is shown in Fig. 3.21. They were measured at $V_I = 4$ V supply voltage, $I_I = 13.4$ mA supply current, and $P_I = 53.6$ mW input power. The calculated, simulated, and measured values of the proposed gate driver at $D = 0.5$ are shown in Table 3.5.

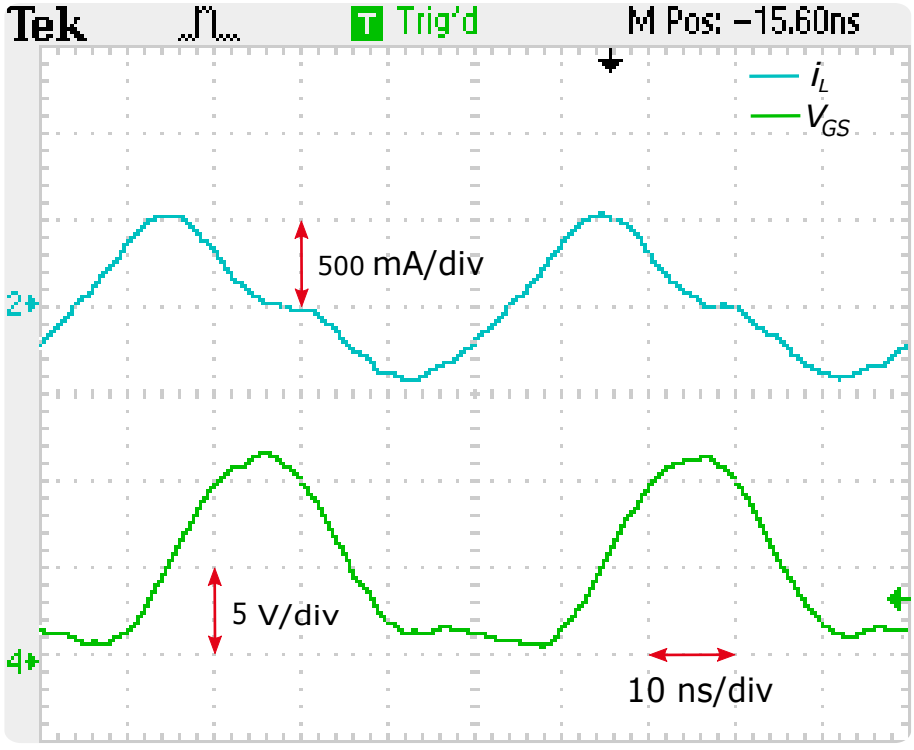

Figure 3.20: Experimental waveforms of inductor current i_L and gate-source voltage v_{GS} of the proposed gate-driver.

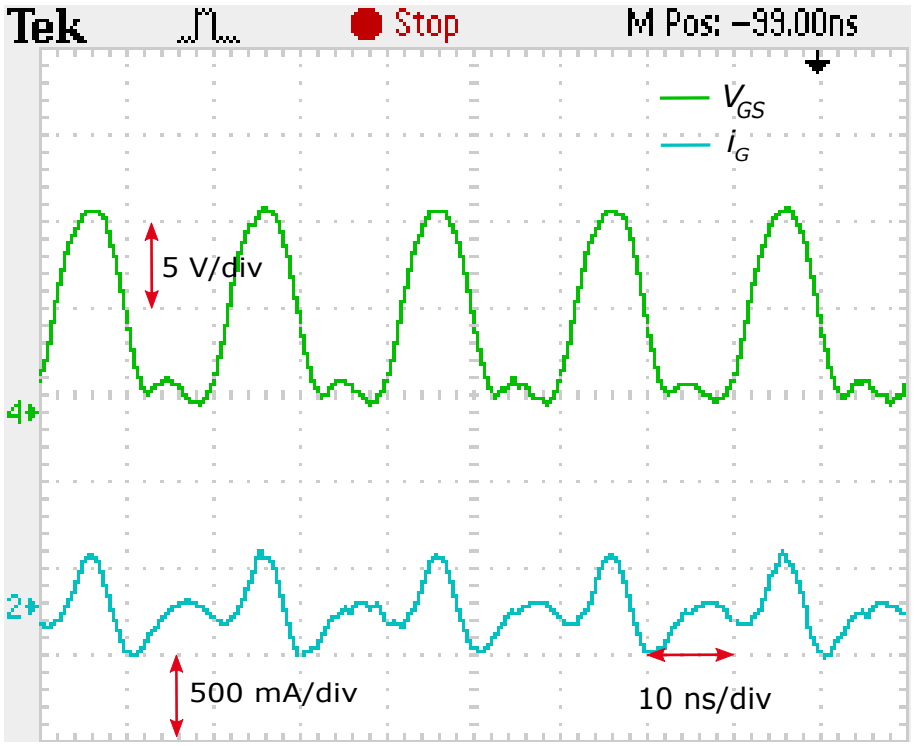

Figure 3.21: Experimental waveforms of gate-source voltage v_{GS} and gate current i_G of the proposed gate driver.

The photograph of the laboratory prototype of the gate driver including the class-E power inverter is shown in Fig. 3.22. The circuit was built and tested at 20 MHz. The gate source voltage v_{GS}, switch current i_S, and switch voltage v_S waveforms were experimentally obtained for the driven transistor M_D as depicted in Fig. 3.23. The maximum switch voltage of the transistor M_D was $V_{SM} \approx 37.5$ V and the maximum switch current was $i_{SM} \approx 2.79$ A. The average input current for the class-E inverter was measured as $I_I = 1.005$ A. When the input voltage $V_{in} = 10$ V, the input power is $P_I = V_{in} \times I_I = 10 \times 1.005 = 10.05$ W. The output current i_O and output voltage v_O waveforms of the class-E inverter are shown in Fig. 3.24. The amplitude of output voltage was $V_{Om} = 10.2$ V and the amplitude of output current was 1.86 A. The load power is $P_O = V_{Om}^2/(2R_L) = 10.2^2/(2 \times 5.77) = 9.016$ W. The measured efficiency of class-E inverter is $\eta = P_O/P_I = 9.016/10.05 = 89.7\%$.

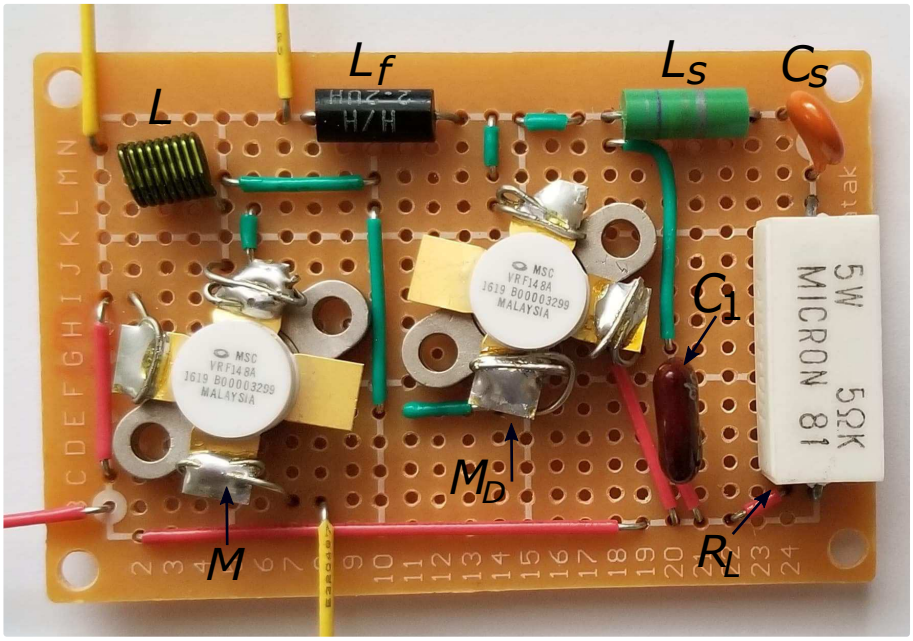

Figure 3.22: Photograph of the proposed gate-driver and the class-E power inverter.

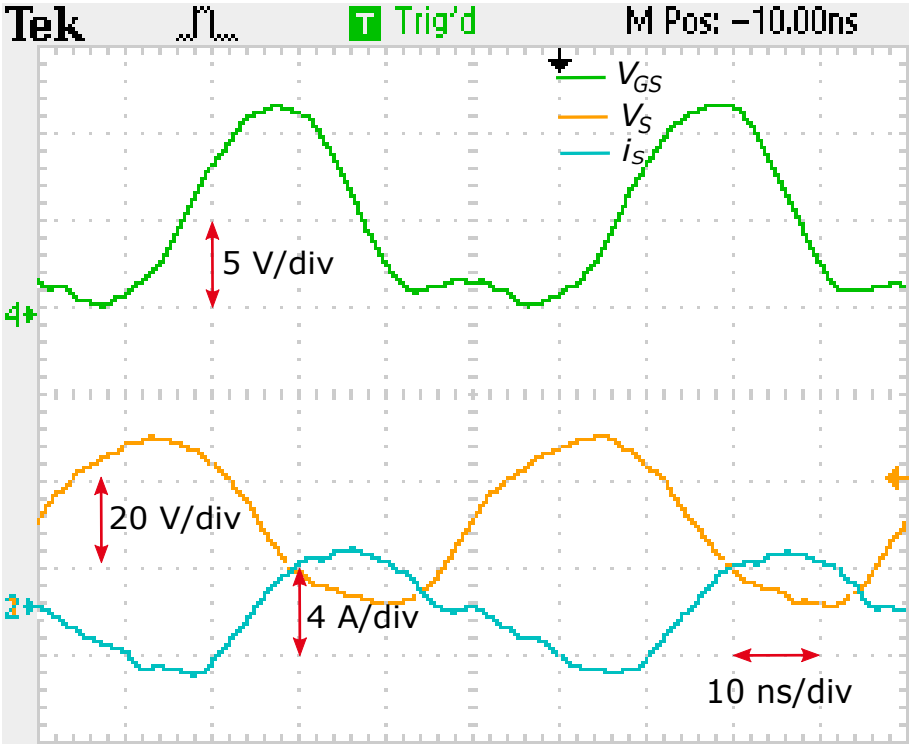

Figure 3.23: Experimental waveforms of gate-source voltage v_{GS}, switch current i_S, and switch voltage v_S of class-E inverter.

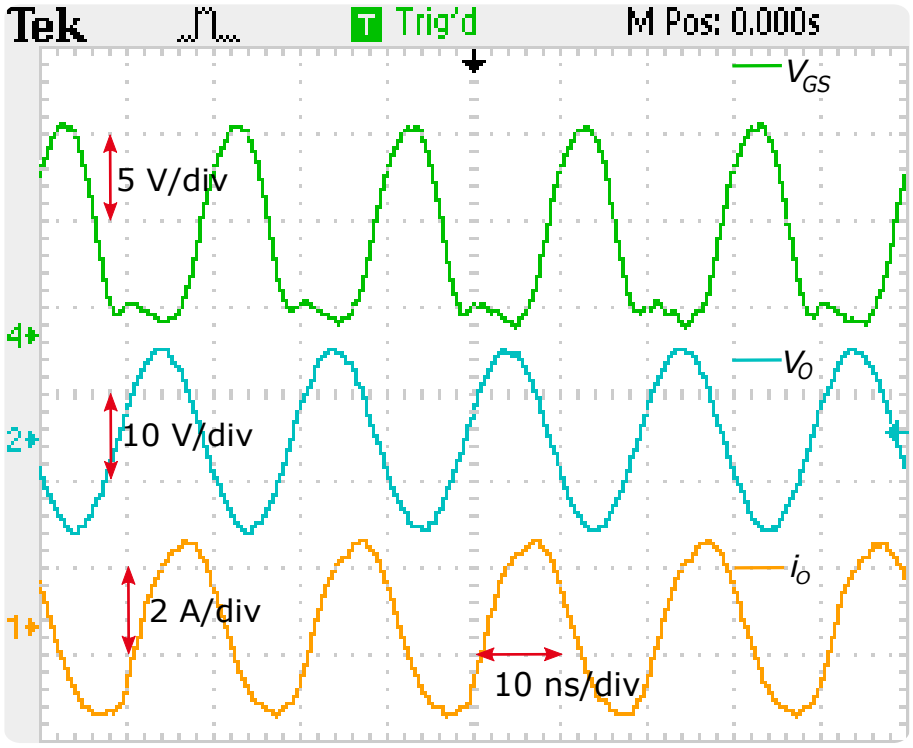

Figure 3.24: Experimental waveforms of gate-source voltage v_{GS}, output current i_O, and output voltage v_o of class-E inverter.

Table 3.5: Theoretical, simulated, and experimental parameters of the proposed gate driver.

Parameter	Calculation	Simulation	Experiment
L (nH)	150	142	150
C (pF)	252	247.6	250
I_{Lmax} (A)	0.33	0.393	0.49
I_{Gmax} (A)	0.33	0.265	0.282
V_{GSmax} (V)	13.05	13.01	11
V_{GSmax}/V_I	3.2629	3.2525	2.75
I_{Smax} (A)	0.66	0.47	0.523
$I_{S(rms)}$ (A)	0.136	0.142	0.148
$I_{G(rms)}$ (A)	0.202	0.158	0.162
$I_{L(rms)}$ (A)	0.243	0.238	0.295
I_I (mA)	11 .74	12.25	13.4

3.7 Conclusions

A new resonant gate driver has been introduced. It has a low component count and a low complexity. The circuit was analyzed, designed, and tested. A good agreement between theoretically produced results and the simulations was observed. It is useful as a low-side gate-drive circuit, especially at high operating frequencies. The turn-ON and turn-OFF transitions were fast. Because of the non-linearity of transistor capacitances, especially the transistor output capacitance, the adjustment of the value of resonant inductance L may be required. The proposed gate driver is suitable for telecom and RF applications that operate in the switching-mode from a few MHz to tens of MHz.

4 High-Frequency Single-Switch ZVS Gate Driver Based on a Class Φ_2 Resonant Inverter

4.1 Introduction

This chapter proposes a single-switch gate-driver with the capability to rapidly charge and discharge the input capacitance of the driven power transistor and achieve quick turn-ON and turn-OFF transitions. In the proposed topology, a series resonant circuit L_r-C_r is tuned to the second harmonic, and connected in parallel with the power MOSFET M. The waveform voltage of the driven power transistor M_D is formed based on the resonant network same as in the class Φ_2, EF_2, and F converters [27]-[17]. Then, the gate-source voltage v_{GS} becomes a near trapezoidal waveform and has the lowered peak value as shown in Fig.4.1. In order to determine the best shape of trapezoidal voltage, an appropriate design has been applied. To apply single-ended ZVS gate driver, two inductors and one capacitor are utilized to have the appropriate impedance. This is primarily to present high impedance to the fundamental and third-harmonic components, and low impedance to the second harmonic [20], [18].

The steady-state waveforms of the proposed gate-driver are analyzed in detail. Expressions to design the gate driver based on the user-specified constraints are derived. In addition, the loss analysis for the gate-driver circuit are presented. The new topology also utilizes small passive components, produces a fast dynamic response, and presents a low-design complexity. These features make the proposed gate-drive

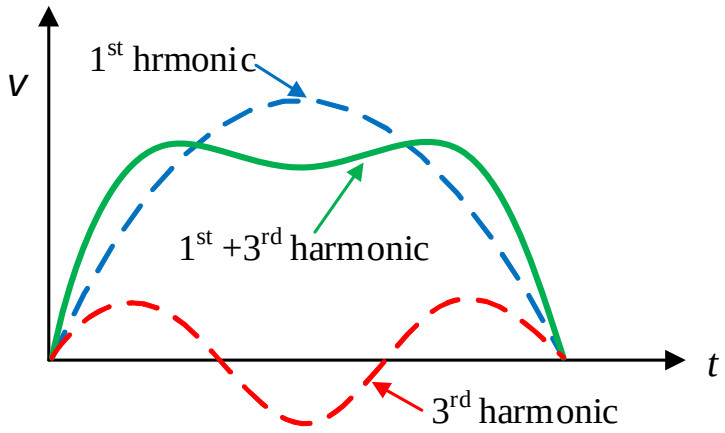

Figure 4.1: Trapezoidal voltage waveform.

topology advantageous in applications that require high-frequency operation such as telecommunication systems and radio-frequency (RF) applications. The described gate driver was designed, built, and tested at 20 MHz switching frequency. Experimental results are demonstrated to validate the predicted analysis.

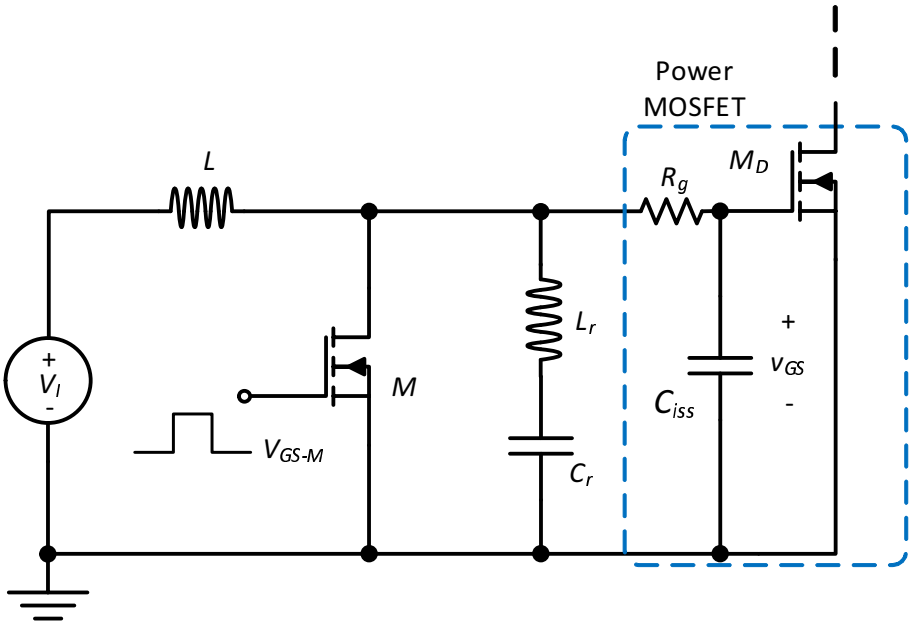

Figure 4.2: Proposed single-switch gate driver circuit.

4.2 Circuit Description

Fig. 4.2 shows a circuit of the proposed single-switch gate driver. It consists of DC voltage supply V_I, an inductor L, a low-side switch M, and a passive resonant network L_r-C_r. The series-resonant circuit L_r-C_r is tuned to the second harmonic and connected in parallel with the driven transistor M_D, which has gate resistance R_g and the input capacitance C_{iss}. The gate-driver transistor M satisfies zero-voltage switching at duty ratio $D = 0.5$. The inductor L behaves as a current source to supply the charge to the input capacitance C_{iss}. The inductor L_r and capacitor C_r form a series resonant circuit, whose current shapes the voltage across the transistor M. The resonant circuit L_r-C_r modifies the half-wave drain-to-source voltage of switch M to produce a fast rise and fall times for the gate-source voltage of the driven-transistor M_D. As a result, a quasi-trapezoidal waveform voltage v_{GS}, which is composed of the fundamental and third-harmonic frequencies, is achieved at the transistor input

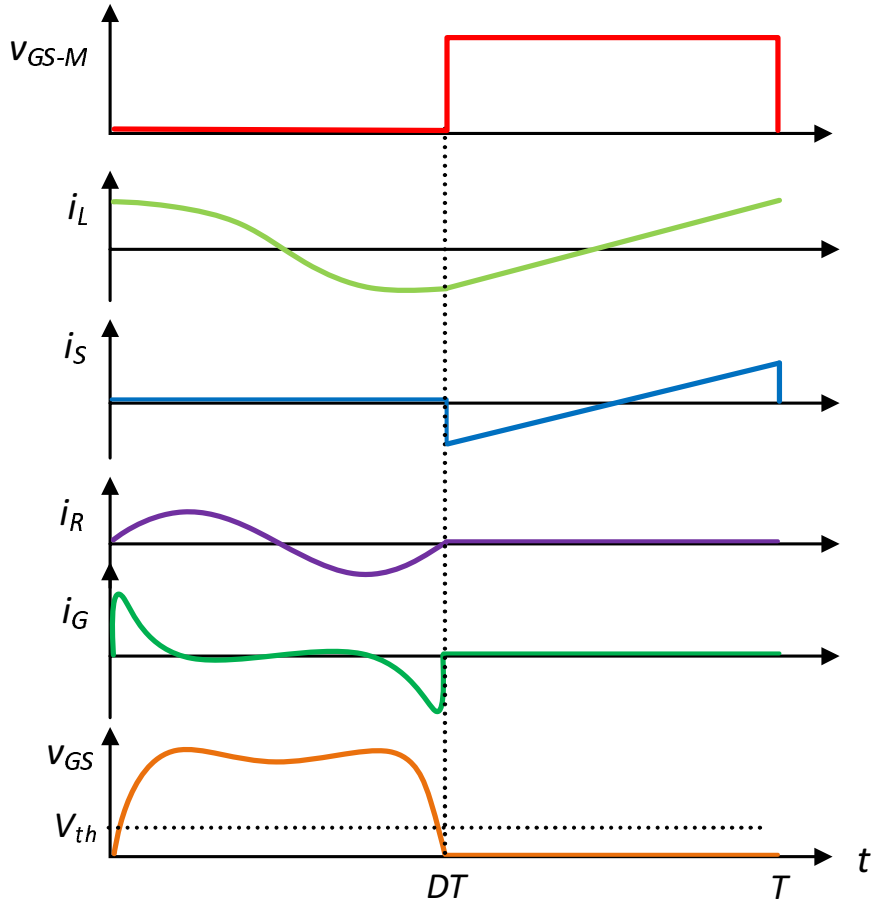

Figure 4.3: Waveforms of the proposed gate driver. From top to bottom: drive signal v_{GSM}, inductor current i_L, switch current i_S, resonant current i_R, gate current i_G, and gate-source voltage v_{GS}.

capacitance C_{iss}. In this study, the interval $0 < t \leq DT$ is defined with the switch M is OFF, and $DT < t \leq T$ as the interval with the switch M is ON.

4.3 Steady-State Analysis

The circuit behavior in each switching sub-interval is analyzed to establish the design equations. The transistor M is a switch with ON-state resistance r_{DS} during the ON interval and offers infinite resistance during the OFF interval. In this study, it assumed that the output parasitic capacitance C_{oss} of the switch M is constant. The switch M can be driven at any duty cycle D, which is determined by the specifications of the power stage. The idealized waveforms illustrating operation of the proposed gate

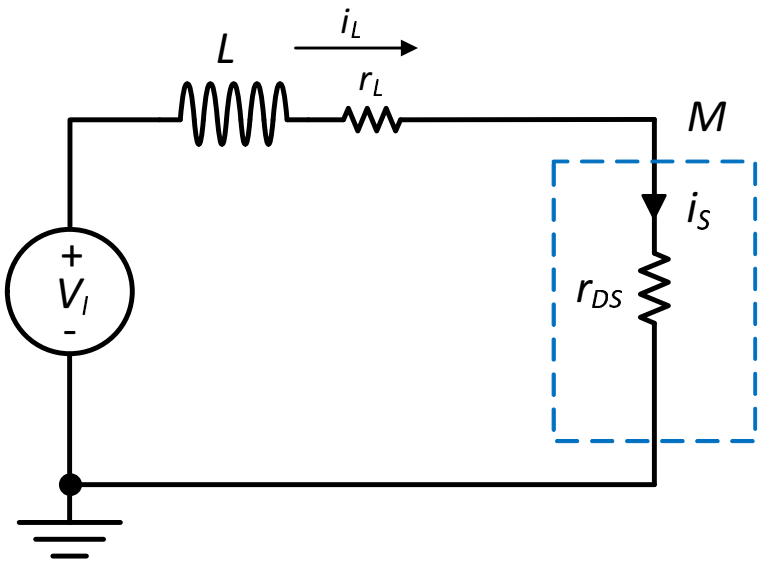

Figure 4.4: Equivalent circuit of the gate driver when the switch M is closed.

driver over a switching period are shown in Fig. 4.3. In this analysis, the proposed gate driver has two operation modes.

4.3.1 Switch-on $DT < t \leq T$

The equivalent circuit corresponding to this phase can be represented as shown in Fig. 4.4. In this time interval, transistor M is ON and its drain-source voltage is zero. Since the voltage across the switch M is zero, the gate-source voltage v_{GS} across the input capacitance C_{iss} is zero, causing the driven-transistor M_D to be in OFF-state. The inductor current i_L flows through the switch M because the switch offers a low impedance path. At this time interval, the gate current i_G is zero and the capacitance C_{iss} is discharged. When the switch M is ON, the voltage across the inductor L is normally equal to the input voltage V_I and the inductor current i_L increases linearly from an initial value $i_L(0)$. The instantaneous inductor current i_L is

$$i_L(t) = \frac{1}{L}\int_{DT}^{t} v_L(t)dt + i_L(0) = \frac{V_I}{L}(t - DT) + i_L(0). \tag{4.1}$$

At the end of this interval $t = T$, the inductor current i_L is

$$i_L(T) = \frac{(1 - D)V_I}{f_s L} + i_L(0), \tag{4.2}$$

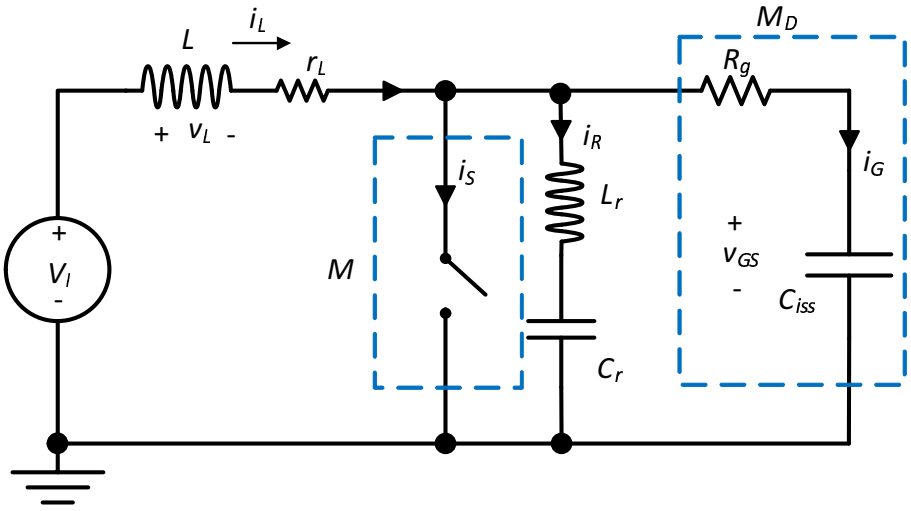

Figure 4.5: Equivalent circuit of the gate driver when the switch M is opened.

where f_s is the switching frequency and $i_L(0)$ is the initial current of the inductor L at time $t = DT$. Hence, the peak-to-peak inductor current over a period T is

$$\Delta i_L = i_L(T) - i_L(0) = \frac{(1-D)V_I}{f_s L}. \tag{4.3}$$

From (4.3), the initial inductor current $i_L(0)$ can be obtained

$$i_L(0) = -\frac{\Delta i_L}{2} = -\frac{(1-D)V_I}{2f_s L} = -\frac{\pi(1-D)V_I}{\omega_s L}. \tag{4.4}$$

During this interval, the switch M supports a low-impedance path to the ground. Thus, the switch current is given by the following equation:

$$i_S = \frac{DV_I}{(1-D)L}(t - DT) - \frac{(1-D)V_I}{2f_s L} \quad \text{for} \quad DT < t \leq T. \tag{4.5}$$

4.3.2 Switch-off $0 < t \leq DT$

During this interval, transistor M is OFF. The switch current i_S is zero. The switch voltage is equal to the gate-source voltage v_{GS} of the driven-transistor M_D. The gate-source voltage v_{GS} rises from zero to the maximum value as shown in Fig. 4.3. The equivalent circuit of the gate-driver relevant to this time interval is shown in Fig. 4.5. To facilitate the analysis, we assume that the internal gate resistance R_g of the driven-transistor M_D is approximated zero ($R_g \approx 0$). To obtain a sinusoidal

current waveform at the resonant circuit L_r-C_r, the inductor L_r and the capacitor C_r are tuned to conduct second harmonic current component. The second harmonic component is related to the resonant elements as

$$\omega_r = 2\omega_s = \frac{1}{\sqrt{L_r C_r}}, \tag{4.6}$$

where ω_r is the angular resonant frequency of the series-resonant circuit L_r-C_r and ω_s is the fundamental frequency. Since the resonant network L_r-C_r is tuned to the second harmonic, its current i_R is sinusoidal waveform and can be expressed as

$$i_R(\omega_s t) = I_m \sin(2\omega_s t + \phi), \tag{4.7}$$

where I_m and ϕ are the amplitude and the phase of the current i_R, respectively. In this interval, the inductor current i_L is the sum of current i_R and gate current i_G. The gate current can be expressed as

$$i_G(\omega_s t) = i_L(\omega_s t) - i_R(\omega_s t), \tag{4.8}$$

where

$$i_G = C_{iss}\frac{dv_{GS}}{dt}. \tag{4.9}$$

Assuming that C_{iss} is linear, we get

$$C_{iss}\frac{dv_{GS}}{dt} = \frac{1}{L}\int_0^t v_L \, dt - I_m \sin(2\omega_s t + \phi), \tag{4.10}$$

and

$$\frac{d^2 v_{GS}}{dt^2} + \frac{v_{GS}}{C_{iss}L} = \frac{V_I}{C_{iss}L} - \frac{2\omega_s}{C_{iss}} I_m \cos(2\omega_s t + \phi). \tag{4.11}$$

This is a second-order non-homogenous differential equation and solving it yields a general solution (homogenous) and a particular solution. The general homogenous solution is

$$v_{GS1}(t) = A\cos(\frac{t}{\sqrt{LC_{iss}}}) + B\sin(\frac{t}{\sqrt{LC_{iss}}}), \tag{4.12}$$

where A and B are arbitrary constants. The zero-state particular voltage response is

$$v_{GS2}(\omega_s t) = V_I + \left(\frac{2a}{4a^2 - 1}\right) Z_o I_m \cos(2\omega_s t + \phi). \tag{4.13}$$

In (4.13),

$$a = \frac{\omega_s}{\omega_o}, \quad Z_o = \sqrt{\frac{L}{C_{iss}}}, \quad \omega_o = \frac{1}{\sqrt{LC_{iss}}}, \tag{4.14}$$

where a is the frequency ratio, Z_o is the characteristic impedance, and ω_o is the resonant frequency. Subsequently, the gate-source voltage $v_{GS}(t)$, which is required to drive the power MOSFET M_D, is the superposition of the two solutions $v_{GS1}(t)$ and $v_{GS2}(t)$ obtained in (4.12) and (4.13), respectively, given by

$$\begin{aligned} v_{GS}(\omega_s t) = V_I + \left(\frac{2a}{4a^2-1}\right) Z_o I_m \cos\left(2\omega_s t + \phi\right) \\ + A\cos\left(\frac{\omega_o t}{a}\right) + B\sin\left(\frac{\omega_o t}{a}\right). \end{aligned} \tag{4.15}$$

In order to solve for constants A and B, two initial conditions are required. The gate-source voltage v_{GS} is equal to 0 at $t = 0^-$, when the switch M_D turns ON. The constants can be determined in terms of the input voltage V_I and the initial inductor current $i_L(0)$. Consequently, the two initial conditions in this interval are $v_{GS}(0) = 0$ and $i_G(0) = i_L(0)$. After finding the constants, the function $v_{GS}(t)$ becomes

$$\begin{aligned} v_{GS}(\omega_s t) = V_I + \left(\frac{2a}{4a^2-1}\right) Z_o I_m \cos\left(2\omega_s t + \phi\right) \\ - \left[V_I + \left(\frac{2a}{4a^2-1}\right) Z_o I_m \cos\left(\phi\right)\right] \cos\left(\frac{\omega_s t}{a}\right) \\ + Z_o \left[i_L(0) + \left(\frac{1}{4a^2-1}\right) I_m \sin\left(\phi\right)\right] \sin\left(\frac{\omega_s t}{a}\right). \end{aligned} \tag{4.16}$$

From (4.4),

$$i_L(0) = \frac{\pi(D-1)V_I}{\omega_s L} = \frac{\pi(D-1)V_I}{aZ_o}. \tag{4.17}$$

The gate-source voltage v_{GS} is

$$\begin{aligned} v_{GS} = V_I + \left(\frac{2a}{4a^2-1}\right) Z_o I_m \cos\left(2\omega_s t + \phi\right) \\ - \left[V_I + \left(\frac{2a}{4a^2-1}\right) Z_o I_m \cos\left(\phi\right)\right] \cos\left(\frac{\omega_s t}{a}\right) \\ + \left[\frac{\pi(D-1)V_I}{a} + \left(\frac{1}{4a^2-1}\right) Z_o I_m \sin\left(\phi\right)\right] \sin\left(\frac{\omega_s t}{a}\right), \end{aligned} \tag{4.18}$$

The gate-source voltage waveform v_{GS} of the driven switch M_D at duty cycle $D = 0.5$ is depicted in Fig. 4.6. Since the gate resistor R_g is neglected in the analysis, the gate-source voltage of the driven switch M_D is equal to the switch voltage of the switch M. In order to produce the desired trapezoidal shape of the gate-source voltage v_{GS} consisting of the 1st and 3rd harmonic frequencies, the resonant frequency ω_o is less than or equal to three times the fundamental frequency. Substitution of the

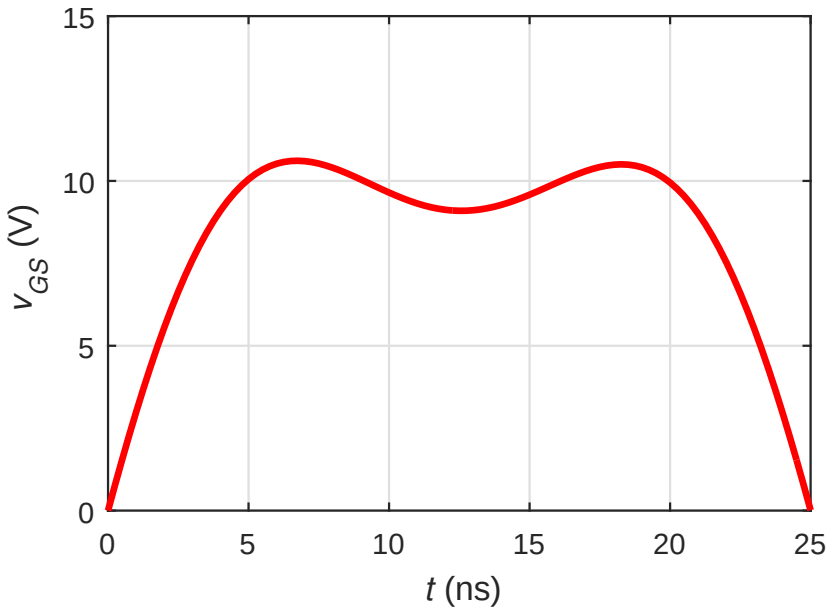

Figure 4.6: Gate-source voltage waveform v_{GS} at $D = 0.5$.

resonant frequency ω_o into (4.14) produces $a = 1/3$. To achieve ZVS operation of the switch M, the switch voltage should be zero at the instant the power switch M is switched ON. When the switch M turns ON at time $t = 2\pi D$, the ZVS condition is satisfied

$$v_{GS}(2\pi D) = 0, \tag{4.19}$$

and yields the relationship

$$I_m = \frac{10V_I}{12Z_o \cos(\phi)}. \tag{4.20}$$

As the power switch M turns ON at $\omega_s t = 2\pi D$, both switch voltage and switch current for ZVS operation are satisfied as shown in Fig 4.7. In the same figure, the voltage waveform of the power switch M are modified for different values of (ϕ).

Since the gate driver operates in periodic steady state, both the average voltage across the inductor v_L and the average gate current i_G through the input capacitance

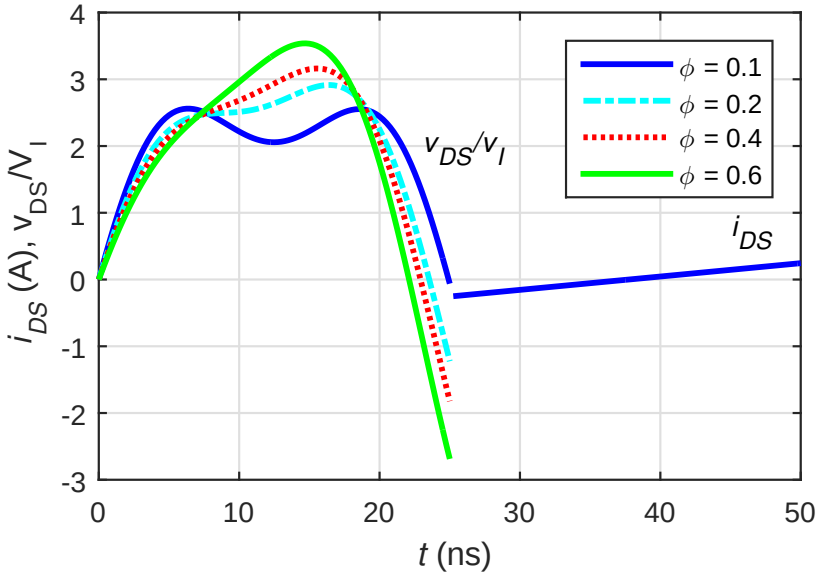

Figure 4.7: Normalized drain-source voltage and drain-source current of the switch M for different values of ϕ (rad).

C_{iss} are zero. The gate current i_G can be expressed as

$$\begin{aligned} i_G(\omega_s t) = &-\left(\frac{4a^2}{4a^2-1}\right) I_m \sin(2\omega_s t + \phi) \\ &+ \left[\frac{V_I}{Z_o} + \left(\frac{2a}{4a^2-1}\right) I_m \cos(\phi)\right] \sin\left(\frac{\omega_s t}{a}\right) \\ &+ \left[\frac{\pi(D-1)V_I}{aZ_o} + \left(\frac{1}{4a^2-1}\right) I_m \sin(\phi)\right] \cos\left(\frac{\omega_s t}{a}\right). \end{aligned} \tag{4.21}$$

Fig. 4.8 shows the gate current waveform at $D = 0.5$. In the proposed gate driver, the gate current supplies the charge to the transistor input capacitance and pulls the charge from the transistor input capacitance when the switch M is OFF.

Another important parameter in the MOSFET is the gate-drain capacitance C_{gd}, which is connected between the input (gate) and the output (drain) of the MOSFET. During the turn ON transition of the power switch M_D, the gate current i_G has to supply a total charge $Q_g = Q_{gs} + Q_{gd}$ to charge the gate-source capacitance C_{gs} and gate-drain capacitance C_{gd}, respectively. Fig. 4.9 shows the schematic and characteristic of the gate charge. The equivalent input capacitance C_{iss} with Miller's effect can be expressed as

$$C_{iss} = C_{gs} + (1 - A_v)C_{gd}, \tag{4.22}$$

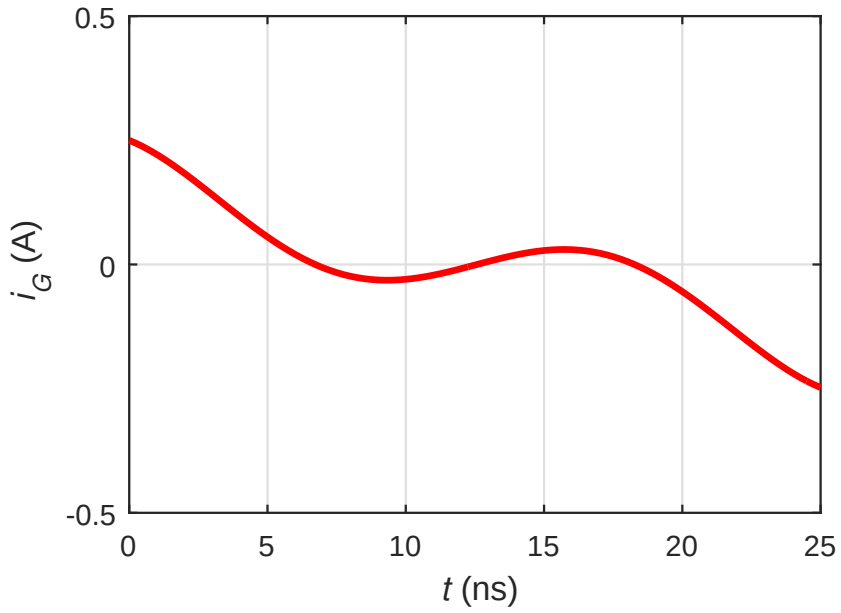

Figure 4.8: Gate current waveform i_G at $D = 0.5$.

where A_v is instantaneous voltage gain

$$Av = \frac{\Delta v_{DS}}{\Delta v_{GS}}. \tag{4.23}$$

The properties of the proposed gate-driver circuit are as follows:

1. The voltage and current stresses of the power switch M depend on the value of the duty cycle D of the power switch M.

2. It has been noticed that the impact of output capacitance C_{oss} of the switch M is a negligible effect on the switch M_D. Thus, its effect on the design and the operation of the gate driver is neglected.

3. The capacitor C_r has an important role in the resonance as well as participating in blocking the dc voltage. Thus, an additional capacitor is not required.

4. The gate driver has fast transient response, and small values (L and L_r) of a few hundred nH at the switching frequency 20 MHz allow for the use of inductors with a few turns of the windings. Since the inductors are air core and the circuit

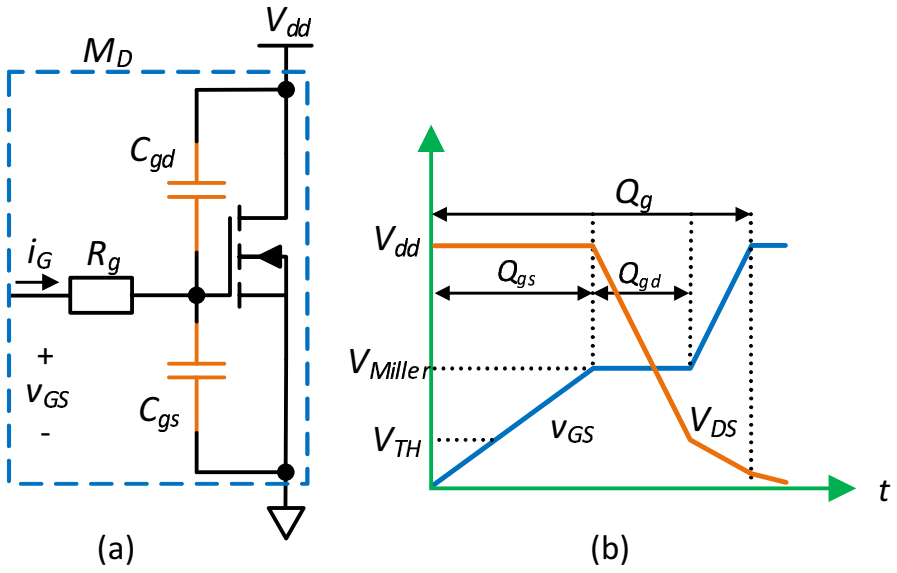

Figure 4.9: (a) Schematic of a MOSFET. (b) Gate charge characteristics of a MOSFET.

is operated in MHz-frequency ranges, the losses associated with magnetic cores are eliminated.

4.3.3 Impedance Analysis

The equivalent impedance Z_g of the proposed gate driver is a significant part to shape the gate-source voltage of the power MOSFET M_D [20]. When the switch M is OFF, the gate-source voltage v_{GS} is shaped by the resonance of capacitors and inductors forming the impedance network Z_g. Thus, the steady-state waveform of v_{GS} of the driven power switch M_D is changed with respect to the impedance Z_g [18]. Since the gate resistance is small, its effect is neglected in the analysis of impedance network. The equivalent impedance network of the proposed gate driver is shown in Fig. 4.10. It has two positive poles and one zero. Therefore, the position of the poles are important in waveform shaping to achieve ZVS at the power switch M and reduce the peak switch voltage [20]. The equivalent impedance is

$$Z_g(s) = \frac{sL(s^2L_rC_r + 1)}{s^4LL_rC_rC_{iss} + s^2(LC_r + LC_{iss} + L_rC_r) + 1}. \tag{4.24}$$

To analyze the characteristic impedance of the gate-drive circuit, a low-frequency pole p_1 and a high-frequency pole p_2 are considered. To achieve ZVS for the switch M, p_1

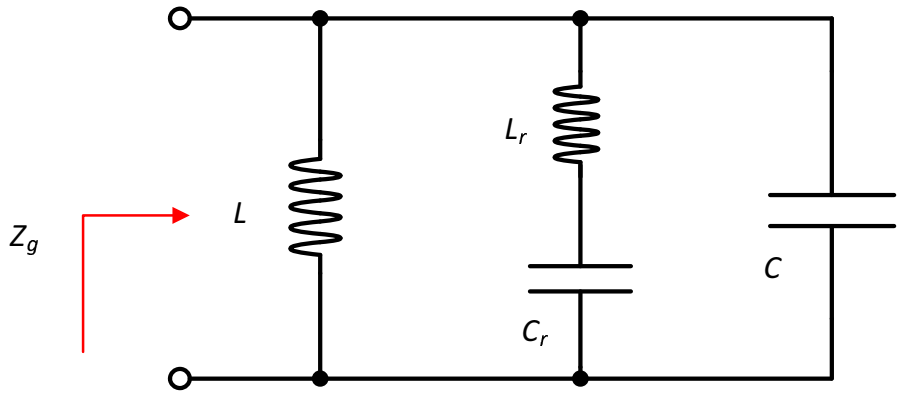

Figure 4.10: Equivalent impedance network of the gate driver.

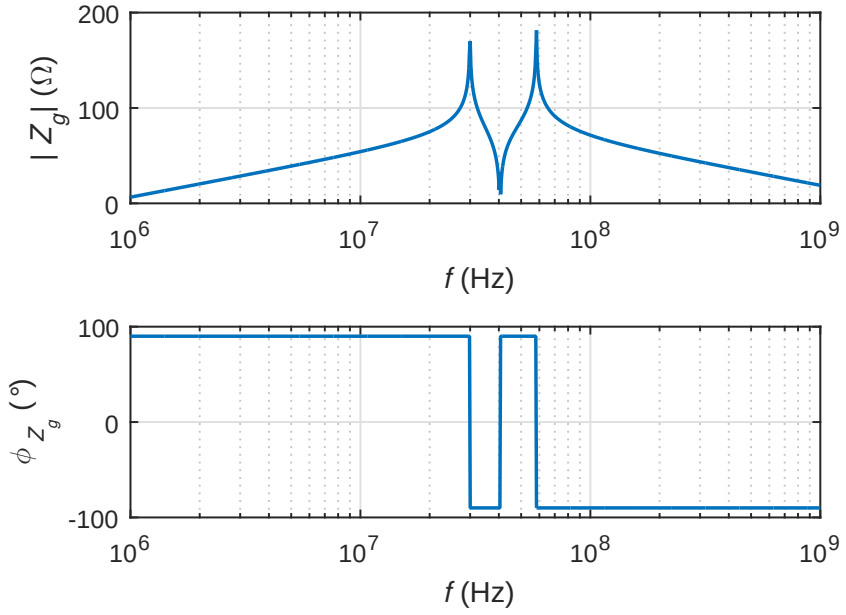

Figure 4.11: Magnitude and phase of the equivalent network impedance Z_g.

is placed to be higher than the fundamental frequency ω_s to make Z_g be inductive at the frequency ω_s. As a result, the zero crossing point in the switch voltage is prior to the switch current. Moreover, the position of p_2 is chosen to be lower than $3\omega_s$ to make Z_g be capacitive. Consequently, the peak voltage of the power device M is reduced. Fig. 4.11 shows the magnitude and phase of the equivalent impedance of the proposed gate-driver. The impedance characteristic of the gate leads to the following results:

- The impedance is inductive at the fundamental switching frequency 20 MHz.
- At the second harmonic, the magnitude of the impedance value is small due to the $L_r - C_r$ resonance circuit, which is a part of the total impedance Z_g and involved in wave-shaping of the gate-source voltage for the power transistor M.
- The impedance is high in magnitude and capacitive in phase below the third harmonic.

4.4 Analysis of Power Losses

In this section, the loss analysis of the proposed gate driver is explained. Many power MOSFETs are suitable for high frequency applications due to their dynamic properties and power ratings; however, gate and switching losses are dominant in the megahertz range [46], [3]. These types of power losses are typically negligible, but with increasing switching frequency they become significant. In addition, the on-resistances of the MOSFETs can cause considerable conduction power losses [37], [2]. Since the power switch is switched under ZVS operation, the switching loss is eliminated. Therefore, the total power loss in the proposed gate driver includes the conduction and gate losses.

The conduction loss in the series tuned branch L_r-C_r due to the internal ESR resistances (r_{Lr} and r_{Cr}) of the inductor L_r and the capacitor C_r is determined. From (4.7), the root-mean-square (rms) current $I_{R(rms)}$ of the L_r-C_r circuit can be calculated as

$$I_{R(rms)} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi D} i_R^2(\omega_s t)\; d\omega_s t} = \frac{I_m}{\sqrt{2}}\sqrt{2D - \frac{\sin 2\phi}{4\pi}}. \tag{4.25}$$

The current flowing in the capacitor C_r is the same as the current in the inductor L_r. Thus, the power loss in the L_r-C_r circuit is

$$P_F = \frac{I_m^2}{2}\left(2D - \frac{\sin 2\phi}{4\pi}\right)(r_{Lr} + r_{Cr}). \tag{4.26}$$

Due to the on-resistance r_{DS} of the power switch M, its conduction power loss is found by calculating the rms current $I_{S(rms)}$. From (4.5), the $I_{S(rms)}$ is given by

$$I_{S(rms)} = \sqrt{\frac{1}{T}\int_{DT}^{T} i_S^2(t)\; dt} = \frac{D\sqrt{1-D}V_I}{\sqrt{12}f_s L}. \tag{4.27}$$

Hence, the conduction power loss in the switch M is

$$P_M = I^2_{S(rms)} r_{DS} = \frac{1-D}{12}\left(\frac{V_I D}{f_s L}\right)^2 r_{DS}. \tag{4.28}$$

When the switch M turns OFF, the behavior of inductor current i_L and the gate current i_G waveforms are nonlinear. In order to estimate the power loss in the inductor L and internal gate resistance R_g of the switch M_D, It is considered that the inductor current and gate current waveforms increase and decrease linearly in a full cycle T. Thus, these waveforms can be described mathematically with linear behavior to simplify the equations. The power loss for each component can then be calculated. When the switch M is OFF, the inductor current waveform can be approximately expressed as

$$i_L = -\frac{V_I}{L}t + \frac{DV_I}{2f_s L} \qquad \text{for } \; 0 < t \; \leq \; DT. \tag{4.29}$$

From (4.1) and (4.29), the rms current $I_{L(rms)}$ of the inductor current i_L for full cycle T is determined as

$$I_{L(rms)} = \frac{DV_I}{\sqrt{12} f_s L}. \tag{4.30}$$

Conduction power loss in the inductor L is dissipated in the equivalent series resistance r_L, which includes the winding resistance loss. The inductor conduction loss is given by

$$P_{rL} = I^2_{L(rms)} r_L = \frac{1}{12}\left(\frac{DV_I}{f_s L}\right)^2 r_L. \tag{4.31}$$

To determine the power loss in R_g, it is considered that $I_{G(rms)}$ is the rms value of the gate current i_G when it flows through the gate terminal of the power transistor M_D. The rms gate current is approximated as follows:

$$I_{G(rms)} = \frac{D\sqrt{D}V_I}{2\sqrt{3} f_s L}. \tag{4.32}$$

The conduction power dissipated in the gate resistance at switching frequency f_s is

$$P_{Rg} = I^2_{G(rms)} R_g = \frac{D}{12}\left(\frac{DV_I}{f_s L}\right)^2 R_g. \tag{4.33}$$

Hence, the total conduction power loss in the gate driver is

$$P_{cond} = P_F + P_M + P_{rL} + P_{Rg}. \tag{4.34}$$

If the total gate charge of the switch M is Q_g at switching frequency f_s, the gate power is defined as

$$P_{gate} = f_s V_{GS-M} Q_g, \tag{4.35}$$

where V_{GS-M} is drive voltage for the switch M. As a result, the total dissipative power loss P_{diss} in the gate driver is

$$P_{diss} = P_{cond} + P_{gate}. \tag{4.36}$$

4.5 Design Procedure

A design procedure for the proposed gate driver is presented to drive the power MOSFET M_D at switching frequency $f_s = 20$ MHz. The design is applied to determine the following design parameters C_r, L_r, L, I_m, and ϕ. The input voltage V_I and duty cycle D were selected to be 4 V and 50%, respectively. This is not a fundamental limit, as the designer can easily choose arbitrary duty cycles. The peak value of the gate-source voltage v_{GS} depends on the duty cycle. Therefore, it is important to select a power transistor with a driving voltage rating that can accommodate this driven voltage. The large output capacitance C_{oss} of the switch M prevents the desired high-switching frequency from being achieved [25]. The power MOSFET MRF136, which has an output capacitance $C_{oss} = 27$ pF, was utilized as driving transistor M in circuit. Thus, the value of capacitor C_r is chosen equal to or less than the output capacitance of the power MOSFET M, i.e., $C_r = 30$ pF. Substituting this into (4.6) yields

$$L_r = \frac{1}{C_r}\left(\frac{1}{4\pi f_s}\right)^2 = \frac{1}{30\times 10^{-12}}\left(\frac{1}{4\pi \times 20 \times 10^6}\right)^2 = 528 \text{ nH}. \tag{4.37}$$

The power MOSFET PD55003, which has an input capacitance $C_{iss} = 36$ pF and reverse transfer capacitance $C_{rss} = 2.4$ pF, was used as the driven transistor M_D in the proposed circuit. The Miller's effect of the switch M_D depends on the gate-source and drain-source voltages of the switch M_D. In this case, the load of the switch M_D is selected to be resistive load $R_L = 50\ \Omega$ and the drain-source voltage $V_{dd} = 10$ V. Since the gate-source voltage $v_{GS} = 10$ V of the switch M_D, the equivalent input capacitance C_{iss} with Miller's effect is given by

$$C_{iss} = C_{gs} + (1 - A_v)C_{gd} = C_{iss} + \left(1 - \frac{V_{dd}}{V_{GS}}\right) C_{rss} \tag{4.38}$$

$$= (36 - 2.4) + \left(1 + \frac{10}{10}\right) \times 2.4 = 38.4 \text{ pF}.$$

According to (4.19), the switch M can be turned ON under ZVS condition if the resonant frequency f_o of the gate driver is less than or equal to three times the operating switching frequency f. To satisfy this condition, the resonant frequency f_o is chosen to be 55 MHz. From (4.14), the frequency ratio a is

$$a = \frac{f_s}{f_o} = \frac{20 \times 10^6}{55 \times 10^6} = 0.3636. \tag{4.39}$$

From (4.14), the value of L can be calculated

$$L = \frac{1}{C_{iss}} \left(\frac{1}{2\pi f_o}\right)^2 = \frac{1}{38.4 \times 10^{-12}} \left(\frac{1}{2\pi \times 55 \times 10^6}\right)^2 = 218 \text{ nH}. \tag{4.40}$$

Based on (4.14), the characteristic impedance Z_o can be obtained by

$$Z_o = \sqrt{\frac{L}{C_{iss}}} = \sqrt{\frac{218 \times 10^{-9}}{38.4 \times 10^{-12}}} \approx 75 \ \Omega. \tag{4.41}$$

According to (4.20), the current magnitude I_m can be found,

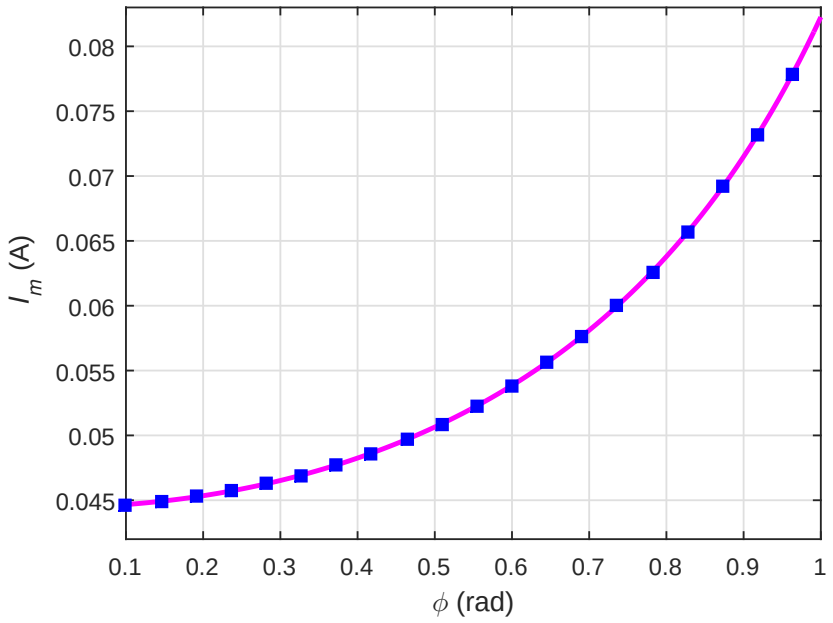

Figure 4.12: I_m as a function of phase angle ϕ.

$$I_m = \frac{10V_I}{12Z_o \cos(\phi)} = \frac{10 \times 4}{12 \times 75 \cos(\phi)} = \frac{2}{45 \cos(\phi)}. \tag{4.42}$$

The relationship between I_m and ϕ can then be determined for different values of ϕ as shown in Fig. 4.12. By choosing $\phi = \ 0.1$, the magnitude current I_m of the i_R current is 44 mA.

From (4.25), the rms current $I_{Lr(rms)}$ of the L_r-C_r circuit is

$$I_{R(rms)} = \frac{I_m}{\sqrt{2}}\sqrt{2D - \frac{\sin 2\phi}{4\pi}} = \frac{0.044}{\sqrt{2}}\sqrt{2 \times 0.5 - \frac{\sin 2 \times 0.1}{4\pi}} = 30.86 \text{ mA}. \quad (4.43)$$

The power loss in the series L_r-C_r is

$$P_F = I_{R(rms)}^2 \left(r_{Lr} + r_{Cr}\right) = 0.03086^2 \left(0.703 + 0.105\right) = 0.7695 \text{ mW}. \quad (4.44)$$

The rms current $I_{S(rms)}$ of the switch current i_S is calculated as

$$I_{S(rms)} = \frac{D\sqrt{1-D}V_I}{\sqrt{12}f_s L} = \frac{0.5\sqrt{1-0.5} \times 4}{\sqrt{12} \times 20 \times 10^6 \times 218 \times 10^{-9}} = 93.635 \text{ mA}. \quad (4.45)$$

Hence, the conduction power loss due to the on-resistance r_{DS} in the switch M is

$$P_M = I_{S(rms)}^2 r_{DS} = 0.093635^2 \times 0.08 = 0.7014 \text{ mW}. \quad (4.46)$$

The rms current $I_{L(rms)}$ of the inductor current i_L for full cycle T is

$$I_{L(rms)} = \frac{DV_I}{\sqrt{12}f_s L} = \frac{0.5 \times 4}{\sqrt{12} \times 20 \times 10^6 \times 218 \times 10^{-9}} = 0.1324 \text{ A}. \quad (4.47)$$

Conduction power loss, which is dissipated in the equivalent series resistance r_L in the inductor L, is

$$P_{rL} = I_{L(rms)}^2 r_L = 0.1324^2 \times 0.29 = 5.083 \text{ mW}. \quad (4.48)$$

From (4.32), the value of rms gate current is

$$I_{G(rms)} = \frac{D\sqrt{D}V_I}{2\sqrt{3}f_s L} = \frac{0.5\sqrt{0.5} \times 4}{2\sqrt{3} \times 20 \times 10^6 \times 218 \times 10^{-9}} = 94.94 \text{ mA}. \quad (4.49)$$

The conduction power loss in the gate resistance R_g is

$$P_{Rg} = I_{G(rms)}^2 R_g = 0.09494^2 \times 0.36 = 3.245 \text{ mW}. \quad (4.50)$$

Hence, the total conduction power loss in the gate driver can be obtained as

$$P_{cond} = P_F + P_M + P_{rL} + P_{Rg} = 0.7695 + 0.7014 + 5.083 + 3.245 = 9.7989 \text{ mW}. \quad (4.51)$$

Table 4.1: List of components for gate driver at $f_s = 20$ MHz.

Components	Value
M_D PD55003	$C_{iss} = 36$ pF, $C_{oss} = 24$ pF, $C_{rss} = 2.4$ pF $V_{ds} = 40$ V, $V_{GS} = 20$ V, $I_{ds} = 2.5$ A $Q_g = 0.288$ nC, $r_{DS} = 0.75\ \Omega$, $R_g = 0.36\ \Omega$
M MRF136	$C_{iss} = 24$ pF, $C_{oss} = 27$ pF, $C_{rss} = 5.5$ pF $V_{ds} = 65$ V, $V_{GS} = 40$ V, $I_{ds} = 2.5$ A $Q_g = 0.24$ nC, $r_{DS} = 0.08\ \Omega$
L, r_L	218 nH, 0.29 Ω
L_r, r_{Lr}	528 nH, 0.703 Ω
C_r, r_{Cr}	30 pF, 0.105 Ω

The gate power dissipated in the gate power switch M at switching frequency $f_s = 20$ MHz is

$$P_{gate} = f_s V_{GS-M} Q_g = 20 \times 10^6 \times 4 \times 0.24 \times 10^{-9} = 19.2 \text{ mW}. \tag{4.52}$$

As a result, the total dissipative power loss P_{diss} in the gate driver is

$$P_{diss} = P_{cond} + P_{gate} = 9.7989 + 19.2 = 28.99 \text{ mW}. \tag{4.53}$$

When the input voltage $V_I = 4$ V is applied at the gate-drive, the peak value of gate-source voltage v_{GS} is 10 V at duty cycle $D = 50\%$. The v_{GS} requirement to drive the power MOSFET depends on the characteristics of the transistor. In this study, the maximum v_{GS} rating of the power transistor, which used in the gate-drive circuit, is 20 V. Thus, a v_{GS} voltage between 4.5 V and 20 V is a safe margin and desirable to realize full enhancement of the power MOSFET. The major difference between the proposed gate driver and the conventional gate drivers is the number of switches and passive components; the proposed ZVS gate driver has single switch and three passive elements. It has the minimum number to achieve the same purpose at high switching frequency. The specifications of the gate-driver components are shown in Table 4.1.

4.6 Simulation Results

Based on the circuit operation and design approach presented in Sections 4.3, the gate driver has been verified through SaberRD simulation. The simulations were performed using PSpice device model of the power MOSFETs. A 20 MHz PWM square wave is used to supply the switch M and the gate-source voltage V_{GS-M} was 6 V. The inductor current i_L was captured in Fig. 4.13. The inductor current supplies the charge to the input capacitance C_{iss} of the power switch M_D, when the switch M turns OFF. In order to analyze current and voltage waveforms of the driven power switch M_D, the whole cycle of the proposed gate driver was recorded in Fig. 4.14. It can be observed that the transistor input capacitance C_{iss} is charged/discharged upon turning ON, OFF, respectively. The gate-source voltage shape is a trapezoidal waveform. The peak gate-source voltage v_{GS} was 11 V to drive the power switch M_D at 50% duty cycle.

High-speed transient response of the gate-source voltage v_{GS} can be increased by reducing the L, but this consideration can have an adverse effect on the desired performance of the gate driver. The numerical value of L should be compatible with

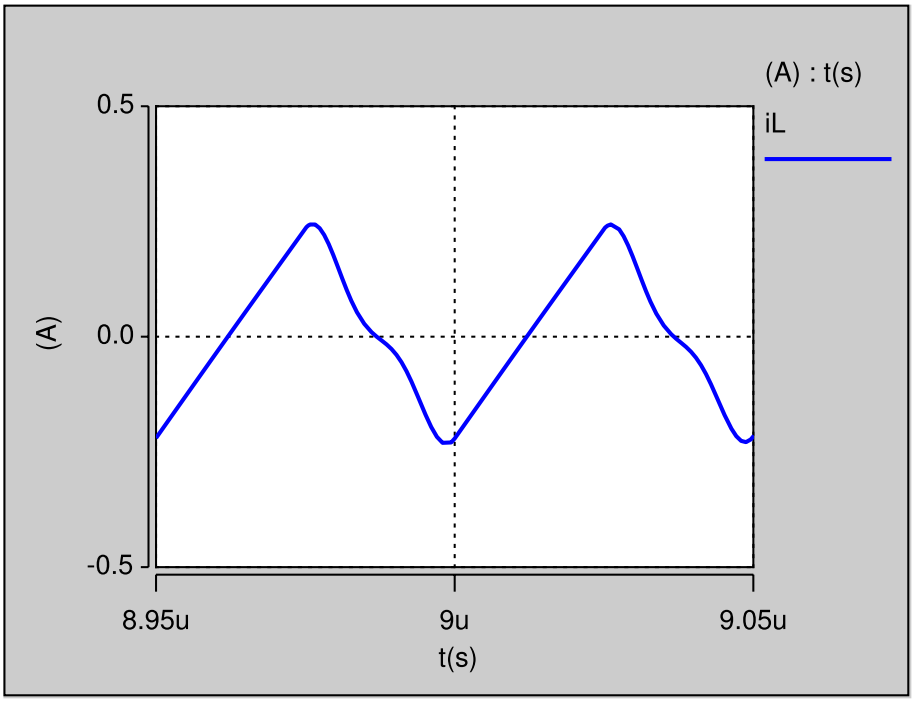

Figure 4.13: Simulated inductor current i_L waveform.

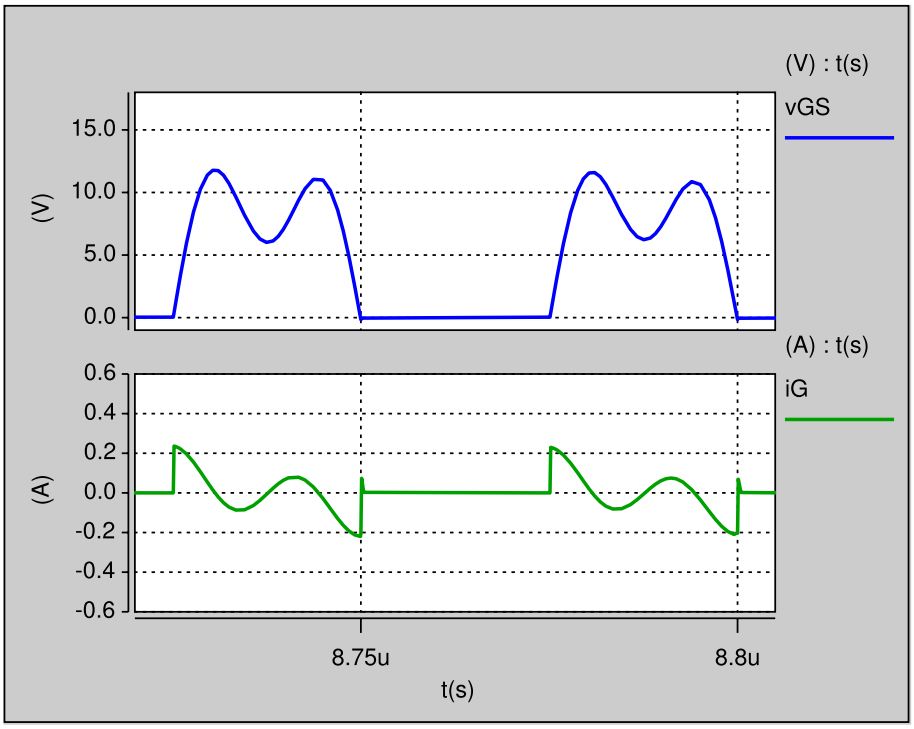

Figure 4.14: Simulated gate current i_G and gate-source voltage waveforms.

tuning process at the series resonant circuit L_r-C_r. At high frequencies, L acts a resonant inductor (i.e., not a choke inductor) and its value is small with low energy storage. This design choice satisfies faster response than a choke inductor. Moreover, the L_r and C_r can be adjusted iteratively to obtain the desired characteristics. The new gate driver proves many advantages that the topology has over conventional designs. It provides high-speed transient response, small-valued components, and low-voltage stress for high frequency operation.

4.7 Experimental Verification

A PDS55003 power MOSFET (40 V, 2.5 A) from STMicroelectronics was used as driven switch M_D in the circuit. It is driven by the proposed gate drive circuit. A MRF136 power MOSFET (65 V, 2.5 A) from Macom was used as a power switch M in the gate driver. These transistors belong to power MOSFET family whose members are optimized for low switching losses and high speed. All components of the gate driver were measured using an HP4194A Impedance Analyzer. A Tektronix TDS2004C digital oscilloscope was used to record the voltage and current waveforms. The prototype gate driver constructed on a printed circuit board (PCB) (2-Layers, 1.25 oz copper) as shown in Fig. 4.15.

The waveforms in Fig. 4.16 and Fig. 4.17 depict the operation of the experimental results of the gate-drive circuit. The inductor current i_L supplies sufficient charge to the transistor input capacitance C_{iss} of the driven transistor M_D when the switch M is OFF. It is clear that the inductor current rises linearly when the switch M is ON. The gate-source voltage v_{GS} waveform, which is a trapezoidal voltage with

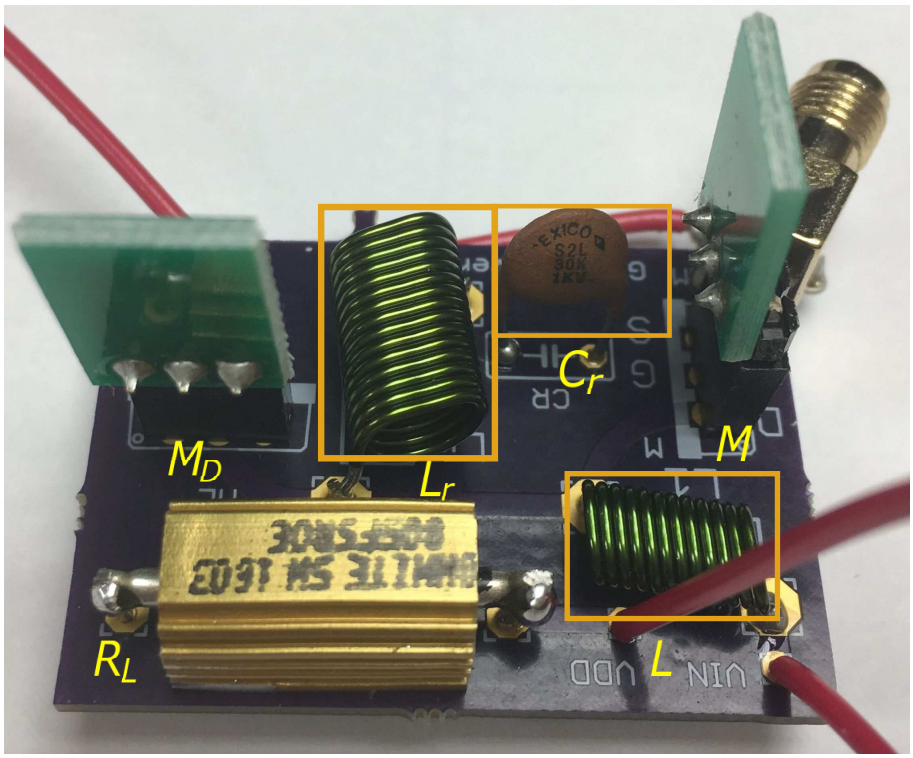

Figure 4.15: Photograph of the proposed gate-drive circuit PCB.

third-harmonic content, demonstrates the operation of the gate-drive circuit. The maximum value of v_{GS} was measured as 10 V. The peak switch voltage is about 2.5 times larger than the input voltage. The gate current i_G waveform is positive when the slope of the gate-source voltage is positive and negative when the slope of the gate-source voltage is negative. The waveforms were recorded for the supply voltage $V_I =$ 4 V, the duty cycle $D =$ 0.5, and the operating frequency $f_s =$ 20 MHz. The theoretical results were verified experimentally using the gate-drive circuit in Fig. 4.2. A comparison of theoretical, simulation, and experimental parameters of the proposed gate-drive circuit is shown in Table 4.2, demonstrating a good agreement. On the other hand, the nominal difference between experimental and the theoretical results may be caused in part by the assumptions of the analysis that the output capacitance of the power MOSFET M in the gate-drive circuit is neglected.

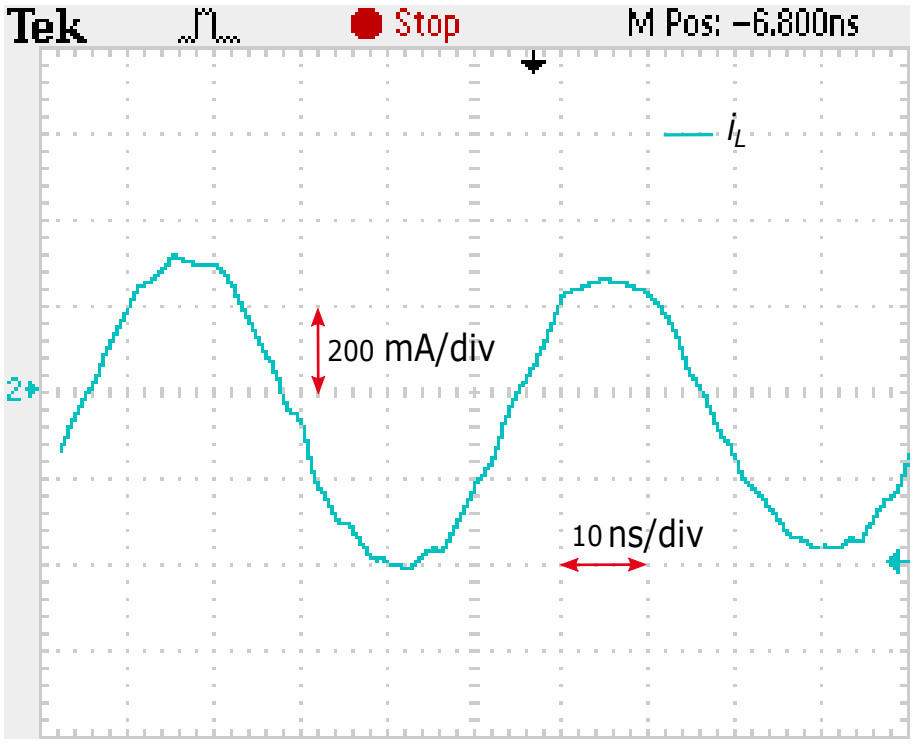

Figure 4.16: Experimental waveform of inductor current i_L.

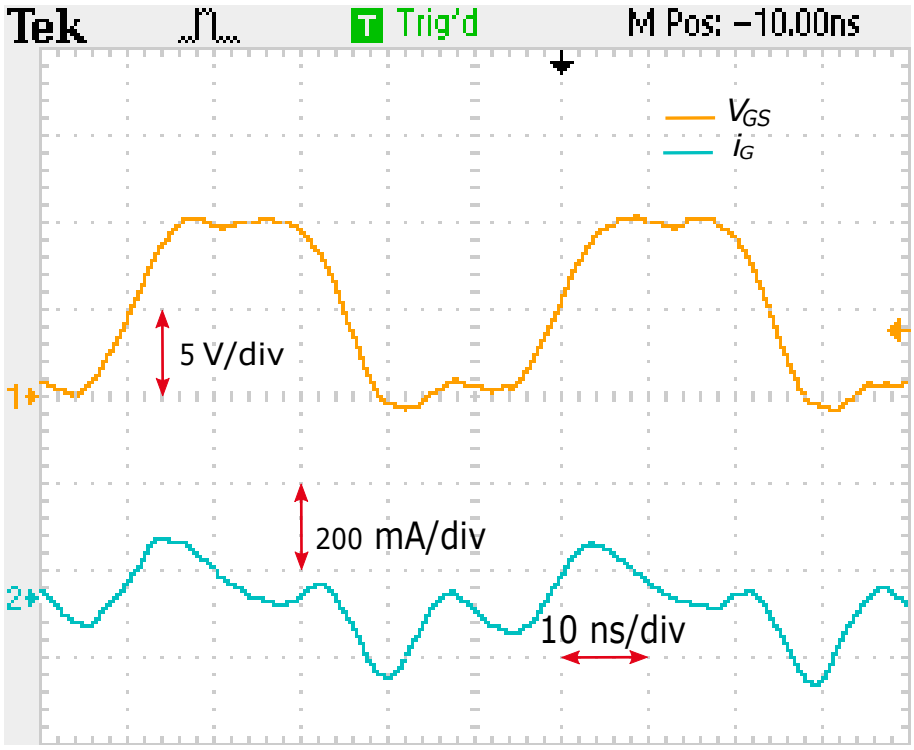

Figure 4.17: Experimental waveforms of v_{GS} and i_G.

In Table 4.2 is shown that the voltage across the power MOSFET is approximately 2.5 times the input voltage at 50% duty cycle. Hence, it is necessary to select a power transistor with a driving voltage rating that can endure this driven voltage. To turn-ON PD55003 transistor, the gate-source voltage was between 4 V to 20 V. The inductance of the power transistors should be as low as possible so that a proper voltage waveform can be attained at high switching frequencies. Moreover, the power MOSFET input capacitance C_{iss} and the output capacitance C_{oss} should be also as low as possible to reduce gate-drive losses and allow high frequency operation.

Table 4.2: Theoretical, simulated and experimental parameters of the gate driver.

Parameter	Calculation	Simulation	Experiment
V_I	4 V	4 V	4 V
L	218 nH	220 nH	220 nH
C_{iss}	38.4 pF	40 pF	40 pF
C_r	30 pF	30 pF	28 pF
L_r	528 nH	510 nH	512 nH
v_{GS}	11 V	11 V	10 V
i_L	0.229 A	0.232 A	0.235 A
i_G	0.225 A	0.22 A	0.18 A

4.8 Conclusions

A new switched-mode ZVS gate driver, which is derived from class Φ_2, has been introduced. It has a low number of passive elements, low switch voltage stress, and high flexibility of design. Based on above analysis, a 20 MHz prototype was designed, simulated, built, and tested. A good agreement between the measurements and the calculations was obtained. The transient response is very fast compared to conventional gate drivers. The gate-source voltage waveform of the gate driver was combined from 1st and 3rd harmonic to offer a trapezoidal waveform voltage. It was shown that incorporating the series resonant L_r-C_r circuit allows single-switch gate driver to operate more effectively at high frequencies. The new topology can be utilized in applications that require high operating frequencies and fixed duty ratio, such as class-E inverter.

5 Class-D Resonant Gate Driver

5.1 Introduction

This chapter proposes a resonant gate-drive circuit, which is based on half-bridge class-D amplifier under high frequency operations. The proposed gate driver can operate in the power converters at several megahertz. The resonant technique has proven to be a good choice for mitigating the power losses in gate-drive circuit [3], [4], [11]. In the proposed technique, a resonant inductor L_r is tuned to resonate with the transistor input capacitance C_{iss}. Due to this approach, the transistors in the gate driver operate under resonant condition. In this chapter, the steady-state waveforms of the proposed gate driver are analyzed in details. The main objectives of this chapter are: (a) to propose a resonant half-bridge gate-drive circuit, (b) to explain and analyze the operation of the proposed gate-driver circuit, (c) to derive design expressions for the proposed circuit, (d) to analyze power losses for the gate driver , (e) to verify the validity of the proposed technique by an experimental prototype.

5.2 Circuit Description

A resonant gate-drive circuit is introduced to drive transistors by using resonant current, which flows through a series resonant circuit as shown in Fig. 5.1. It consists of two switches M_1, M_2, and an inductor L_r. The input capacitance of the driven power MOSFET M is C_{iss}, which should be charged and discharged during turn-ON and turn-OFF intervals, respectively. The resonant current flows through the resonant inductor L_r, leading to charge/discharge the transistor input capacitance C_{iss}. The key waveforms of the proposed gate driver are shown in Fig. 5.2. The v_{GS1} and v_{GS2} are drive signals. The i_{Lr} and i_G are the currents that flow through the resonant inductor L_r and power MOSFET gate resistance R_g, respectively. The v_{GS} is the gate-source voltage across the input capacitance C_{iss}. The MOSFETs are N-channel enhancement-mode type. The circuit operation can be divided into three interval modes.

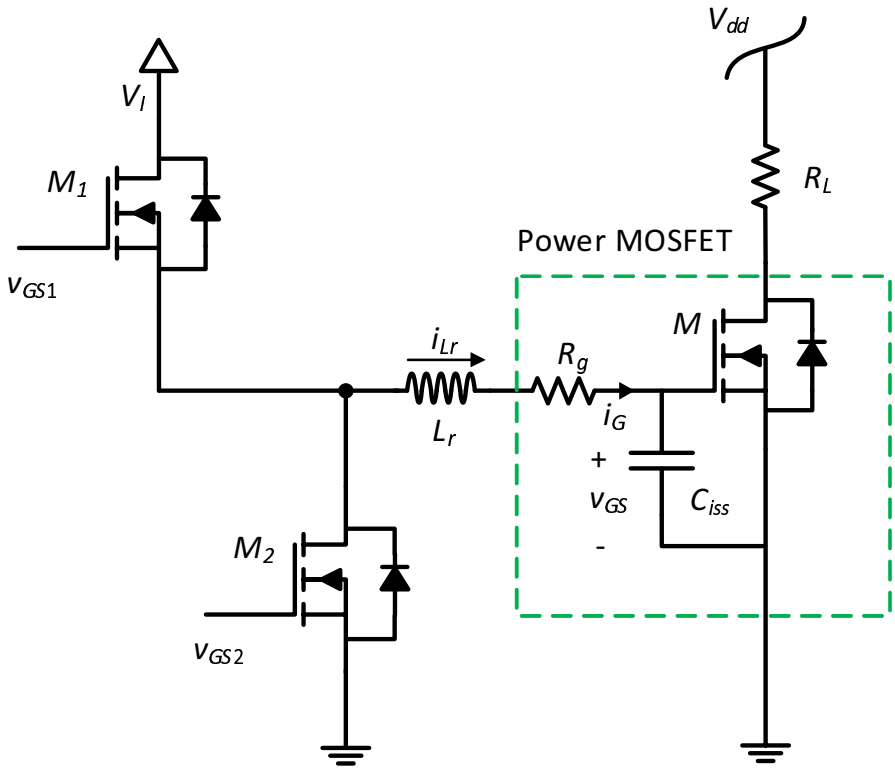

Figure 5.1: Proposed resonant gate-drive circuit.

5.3 Steady-State Analysis

Interval A $[t_1, t_2]$: In this interval, at time t_1 the switch M_2 is OFF and the switch M_1 is turned-ON to allow the input capacitance C_{iss} to be charged. The equivalent circuit of the gate-drive circuit is shown in Fig. 5.3. During this interval, the inductor current i_{Lr} is rising by applying voltage V_I to supply the charge to the input capacitance C_{iss}. Therefore, the gate-source voltage v_{GS} ramps up and the power MOSFET M turns-ON. This interval is represented as t_r, when i_{Lr} flows through the gate resistance R_g. At the end of the interval, the input capacitance C_{iss} of the power MOSFET M is fully charged. To find the gate current that charges the transistor input capacitance, a second-order equation is used as follows.

$$i_G(s) = \frac{V_I}{L_r} \frac{1}{s^2 + \frac{R_g}{L_r}s + \frac{1}{L_r C_{iss}}} = \frac{V_I}{L_r} \frac{1}{(s+\alpha)^2 + \omega_d^2}, \tag{5.1}$$

where

$$\alpha = \frac{R_g}{2L_r}, \quad \omega_d = \sqrt{\omega_o^2 - \alpha^2} = \omega_o \sqrt{1 - \frac{1}{4Q^2}}, \tag{5.2}$$

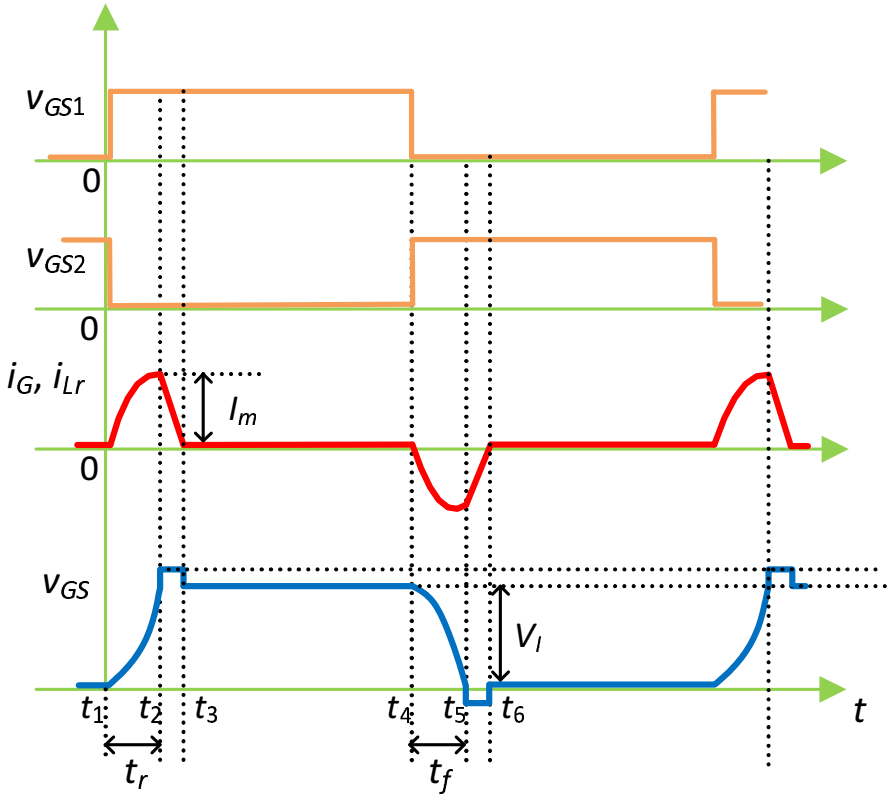

Figure 5.2: Key waveforms of the proposed resonant gate-drive circuit.

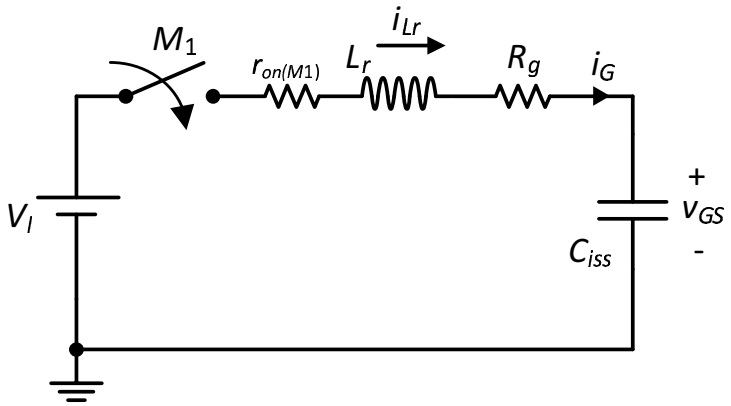

Figure 5.3: Equivalent circuit when switch M_1 is ON and switch M_2 is OFF.

and

$$\omega_o = \frac{1}{\sqrt{L_r C_{iss}}}, \quad Z_o = \sqrt{\frac{L_r}{C_{iss}}}. \tag{5.3}$$

The gate current can be expressed in time domain according to the following equation:

$$i_G(t) = L^{-1}\{i_G(s)\} = \frac{V_I}{\omega_d L_r} e^{-\alpha t} \sin(\omega_d t) = \frac{V_I}{Z_o} e^{-\alpha t} \sin(\omega_d t). \tag{5.4}$$

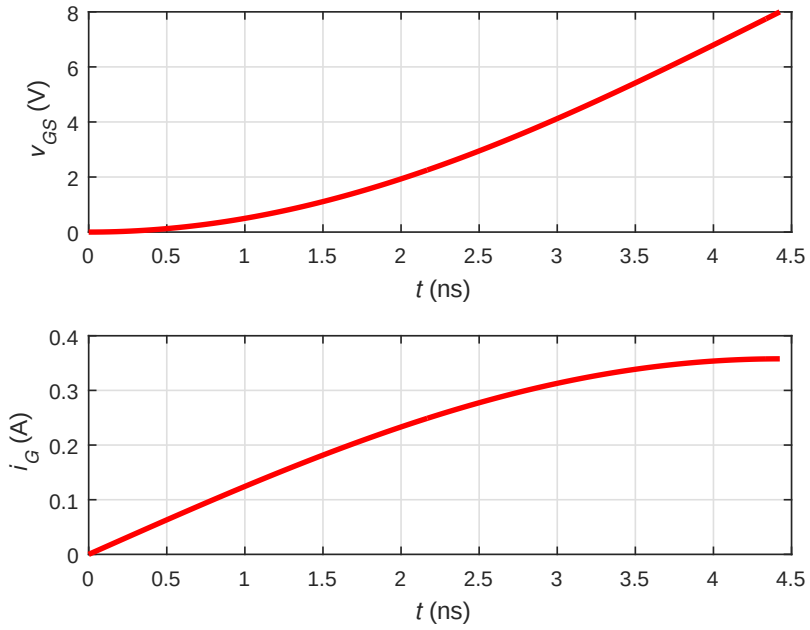

Figure 5.4: Gate-source voltage and gate current, when switch M_1 is ON and switch M_2 is OFF.

During the charge period, the gate current fluctuates sinusoidally and reaches to its peak value at the end level of the gate-source voltage v_{GS} as shown in Fig. 5.4. The inductor voltage v_{Lr} can be obtained as

$$v_{Lr}(t) = L_r \frac{di_G(t)}{dt} = V_I e^{-\alpha t} \cos(\omega_d t). \tag{5.5}$$

In this interval, the initial condition of the gate-source voltage is $v_{GS}(0) = 0$. The gate-source voltage v_{GS} across the input capacitance C_{iss} is

$$v_{GS}(t) = \frac{1}{C_{iss}} \int_0^t i_G(t)\ dt = V_I \left[1 - e^{-\alpha t} \cos(\omega_d t) - \frac{\alpha}{\omega_d} e^{-\alpha t} \sin(\omega_d t)\right]. \tag{5.6}$$

From (5.6), the gate-source voltage v_{GS} rises sinusoidally from zero to the peak value V_I as shown in Fig. 5.4. During the rise time t_r, the gate-source voltage v_{GS} reaches to greater than the supply voltage V_I, and its peak value depends on the quality factor Q of the resonant circuit.

The gate resistance R_g is a damping component for the circuit and is lower than the characteristic impedance Z_o, i.e., $R_g << Z_o$, leading to $R_g \approx 0$, $\alpha = 0$, and

$\omega_o \approx \omega_d$. At the rise time t_r, the gate-source voltage v_{GS} reaches the supply voltage V_I

$$v_{GS}(t_r) = V_I, \tag{5.7}$$

then

$$V_I[1 - \cos(\omega_o t_r)] = V_I, \tag{5.8}$$

yielding

$$\cos(\omega_o t_r) = 0, \tag{5.9}$$

which produces

$$\omega_o t_r = \frac{\pi}{2}. \tag{5.10}$$

Hence, the rise time is

$$t_r = \frac{\pi}{2\omega_o} = \frac{\pi}{2}\sqrt{L_r C_{iss}}. \tag{5.11}$$

The speed at which the MOSFET is driven typically 1% to 4% of the switching time period T. In this study, the turn-ON speed of MOSFET is considered to be 3% of switching period T

$$\frac{t_r}{T} = 0.03. \tag{5.12}$$

Thus, the resonant inductor L_r at switching frequency f_s is

$$L_r \leq \frac{4t_r^2}{\pi^2 C_{iss}} = \frac{4}{C_{iss}}\left(\frac{0.03}{\pi f_s}\right)^2. \tag{5.13}$$

Interval B [t_3, t_4]: This interval begins when C_{iss} of M is fully charged and the energy is zero in the inductor L_r. Therefore, the inductor current i_{Lr} and the current i_G through the gate resistance are zero. During this interval, v_{GS} is constant and clamped to the input voltage V_I as shown in Fig. 5.2 .

Interval C [t_4, t_5]: Fig. 5.5 shows the equivalent circuit during this interval. The switch M_1 is OFF and the switch M_2 is turned ON. At time t_4, the gate-source voltage v_{GS} of the power switch M starts to decrease sinusoidally until time instant t_5. During this interval, the input capacitance C_{iss} of M is discharged through the inductor L_r. This time duration is represented as t_f for the power switch M. At the instant t_5, the gate-source voltage v_{GS} is clamped to ground and the capacitance C_{iss} is completely

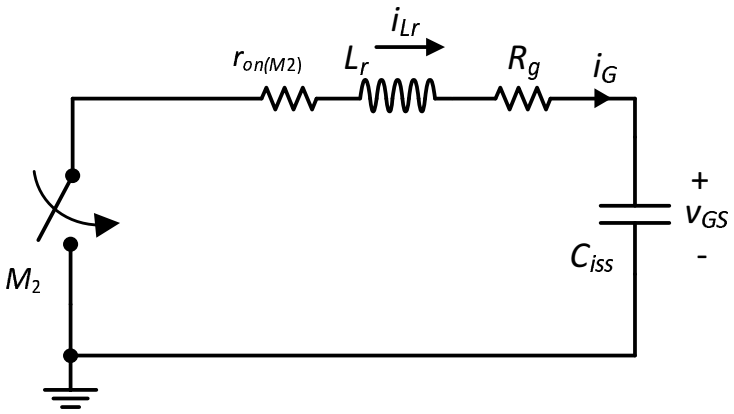

Figure 5.5: Equivalent circuit when switch M_1 is OFF and switch M_2 is ON.

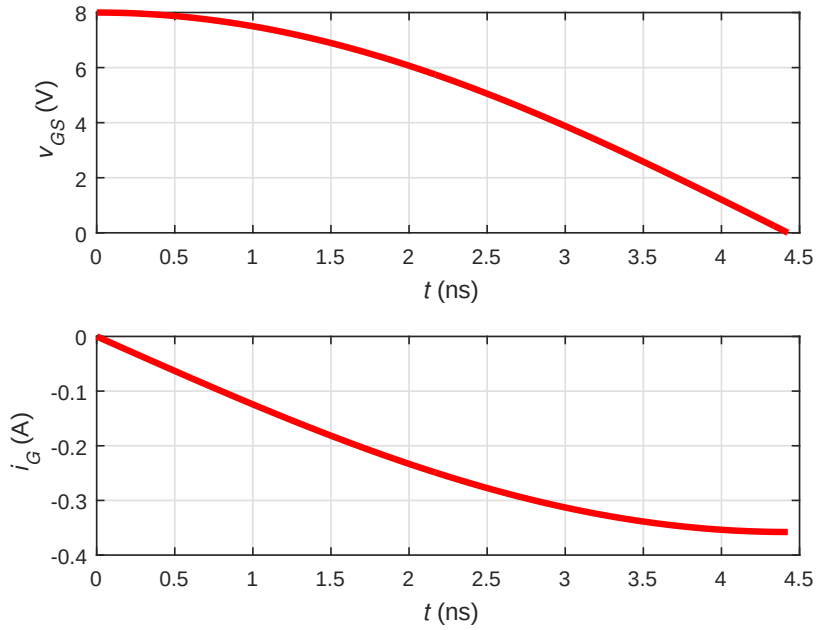

Figure 5.6: Gate current and gate-source voltage, when switch M_1 is OFF and switch M_2 is ON.

discharged. The gate current flowing through the gate resistance R_g and the resonant inductor L_r is

$$i_G(s) = -\frac{V_I}{L_r}\frac{1}{(s+\alpha)^2+\omega_d^2}e^{-s(t-t_4)}. \tag{5.14}$$

Hence,

$$i_G(t) = L^{-1}\{i_G(s)\} = -\frac{V_I}{\omega_d L_r}e^{-\alpha(t-t_4)}\sin[\omega_d(t-t_4)]. \tag{5.15}$$

The gate current waveform is shown in Fig. 5.6. Also, the gate current i_G can be expressed as

$$i_G(t) = -\frac{V_I}{Z_o} e^{-\alpha(t-t_4)} \sin \omega_o (t - t_4) = -I_m e^{-\alpha(t-t_4)} \sin \omega_o (t - t_4), \tag{5.16}$$

where $I_m = V_I/Z_o$ is the amplitude of gate current.

Since the resonance occurs in C_{iss} and L_r, both the gate-source voltage v_{GS} and gate current i_G will decrease sinusoidally. In this interval, the initial value of the gate-source voltage is $v_{GS}(\omega_o t_4) = V_I$. The gate-source voltage during discharge interval is

$$v_{GS}(t) = V_I + \frac{1}{C_{iss}} \int_{t_4}^{t} i_G(t)\ dt \tag{5.17}$$

$$= V_I \left[e^{-\alpha t - t_4} \cos \omega_d (t - t_4) + \frac{\alpha}{\omega_d} e^{-\alpha t - t_4} \sin \omega_d (t - t_4) \right].$$

The gate-source voltage waveform is shown in Fig. 5.6. The fall time $t_f = t_5 - t_4$ of the voltage v_{GS} is determined by the following condition:

$$v_{GS}(t_4) = V_I \cos \omega_o (t_5 - t_4) = V_I \cos \omega_o (t_f) = 0, \tag{5.18}$$

producing

$$\cos(\omega_o t_f) = 0, \tag{5.19}$$

which gives

$$\omega_o t_f = \frac{\pi}{2}. \tag{5.20}$$

Hence, the fall time is

$$t_f = \frac{\pi}{2\omega_o} = \frac{\pi}{2} \sqrt{L_r C_{iss}}. \tag{5.21}$$

5.4 Analysis of Power Losses

According to Fig. 5.1, the power stage loss of the proposed resonant gate-drive circuit is analyzed. In the proposed circuit, the input capacitance C_{iss} and the series gate resistance R_g are considered as parasitic components of the power MOSFET. Moreover, the loss analysis includes the equivalent series resistance r_{Lr} of the resonant inductor and the on-resistance r_{on} of the switches M_1 and M_2, respectively. The conduction loss can be determined by finding first the rms current $I_{G(rms)}$ that flows through the on-resistance r_{on} of the power MOSFET M_1 given by

$$I_{G(rms)} = \sqrt{\frac{2}{T}\int_0^{T_d/2} I_m^2 \sin^2(t)dt} = \frac{I_m}{\sqrt{2}}\sqrt{\frac{f_s}{f_d}} = I_m\sqrt{\frac{k}{2}} = \frac{V_I}{Z_o}\sqrt{\frac{k}{2}}, \tag{5.22}$$

where $k = f_s/f_d$. The total conduction loss in the circuit is

$$P_{LS} = I_{G(rms)}^2(r_{on} + r_{Lr} + R_g) = \frac{I_m^2}{2}k(r_{on} + r_{Lr} + R_g). \tag{5.23}$$

The P_{LS} is the power loss in ON-states for both switches M_1 and M_2 as described above. We consider P_I as the input power of the gate drive-circuit. The input power P_I is based on input voltage V_I and supply current I_I. The average input current of the gate-drive circuit can be determined as

$$I_I = \frac{I_m}{2\pi}\int_0^{\omega_d t_r} \sin\omega_d t \; d(\omega_d t) = \frac{I_m}{2\pi}\left[1 - \cos(\omega_d t_r)\right]. \tag{5.24}$$

The input power amounts to

$$P_I = V_I I_I = \frac{V_I I_m}{2\pi}\left[1 - \cos(\omega_d t_r)\right] = \frac{V_I^2}{2\pi Z_o}\left[1 - \cos(\omega_d t_r)\right]. \tag{5.25}$$

5.5 Design Procedure

In this section, an example resonant gate-drive circuit is provided. The specifications of the circuit are as follows: the input voltage $V_I = 8$ V, switching frequency $f_s = 6.78$ MHz, the duty cycle $D = 0.5$. The input capacitance C_{iss} of power MOSFET is linear, whose value is $C_{iss} = 126$ pF. In this study, the speed of the MOSFET is selected as 3% of the switching time period T, i.e., $t_r/T = 0.03$. From (5.13), the resonant inductance L_r is

$$L_r = \frac{4}{C_{iss}} \left(\frac{0.03}{\pi f_s} \right)^2 = \frac{4}{126 \times 10^{-12}} \left(\frac{0.03}{\pi \times 6.78 \times 10^6} \right)^2 = 63 \text{ nH}. \tag{5.26}$$

Based on (5.3), the characteristic impedance of the resonant gate-drive circuit can be calculated as

$$Z_o = \sqrt{\frac{L_r}{C_{iss}}} = \sqrt{\frac{63 \times 10^{-9}}{126 \times 10^{-12}}} = 22.36 \ \Omega. \tag{5.27}$$

As the slope of the gate-source voltage reaches its maximum value during the time interval t_1 and t_2, the gate current reaches its peak value. Therefore, the peak value of gate current I_{Gpk} is

$$I_{Gpk} = \frac{V_I}{Z_o} = \frac{8}{22.36} = 0.357 \text{ A}. \tag{5.28}$$

In the proposed gate driver, the gate-source voltage v_{GS} exhibits sinusoidally due to the resonance in the circuit. From (5.6), the minimum value of the gate-source voltage v_{GS} is zero and the peak value was $V_I = 8$ V. Then, the average input current can be calculated from (5.24) and its value was $I_I = 48$ mA and the rms value of the gate current can be obtained from (5.22), which was equal to I_{Grms} 34 mA. According to (5.25), the input power of the resonant gate driver was $P_I = 384$ mW.

5.6 Simulation Results

A high-frequency resonant gate driver was designed and simulated. The simulations were performed using the PSPICE device models of the power switches. SaberRD software was used to simulate the resonant gate-drive circuit and observe operating characteristics. The gate driver is tested to drive the power MOSFET M at $V_{dd} =$ 10 V and resistive load $R_L = 50\ \Omega$. The input voltage of the gate driver is 8 V at 50% duty cycle. A 6.78 MHz PWM square wave is used to supply the switches M_1 and M_2.

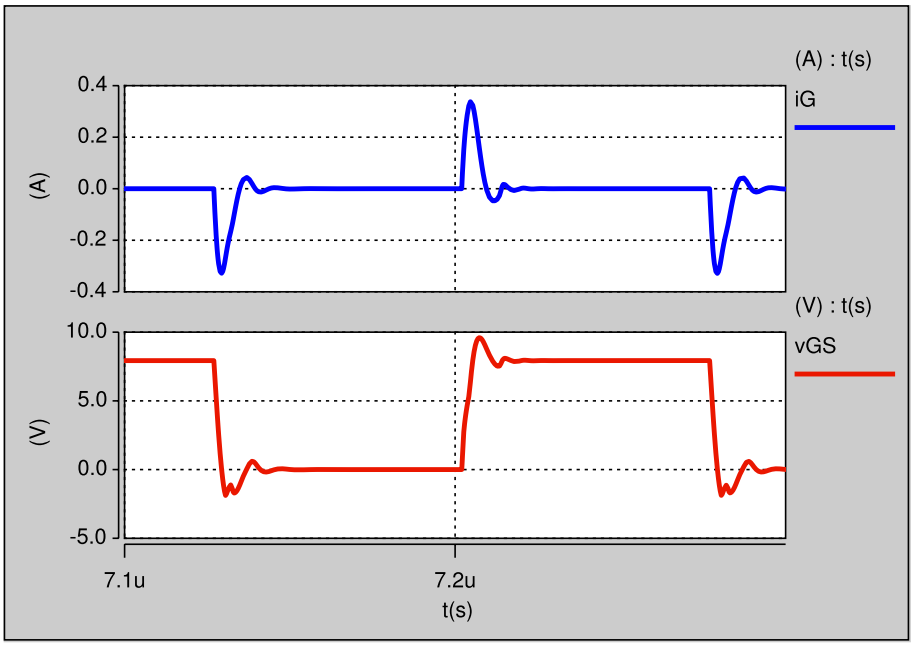

Figure 5.7: Simulated gate current and gate-source voltage waveforms of switch M.

The waveforms of the gate current i_G and the gate-source voltage v_{GS}, which is used to drive power MOSFET M, are shown in Fig. 5.7. It can be observed that the voltage shape is approximately square wave. The gate driver supplies the current through the inductor L_r at each switching interval. Therefore, the gate current provides the sufficient charge to the transistor input capacitance C_{iss} to turn ON the power MOSFET M. In addition, the charge is pulled from the input capacitance C_{iss} by turning OFF operation. From the gate current waveform, it can be seen that due to a small gate charge value and small output capacitance of the power MOSFET, the dv/dt is high at turn-ON and turn-OFF transitions.

In Fig. 5.8, the duty cycle of the switch M is 0.5, the two signals are gate-source voltage v_{GS} and drain-source voltage v_{DS} of the switch M. Significant high stray inductance causes oscillations in the switch voltage waveform at high frequencies. On the other hand, the drain-source voltage has quick turn-ON transition time. It means that high speed switching and resonant operating have been achieved. In the same figure, a transition time of 5.9 ns was recorded for the drain-source voltage waveform. The characteristics of the proposed gate-drive circuit are as follows:

- The proposed gate driver can be used to drive high-side or low-side power

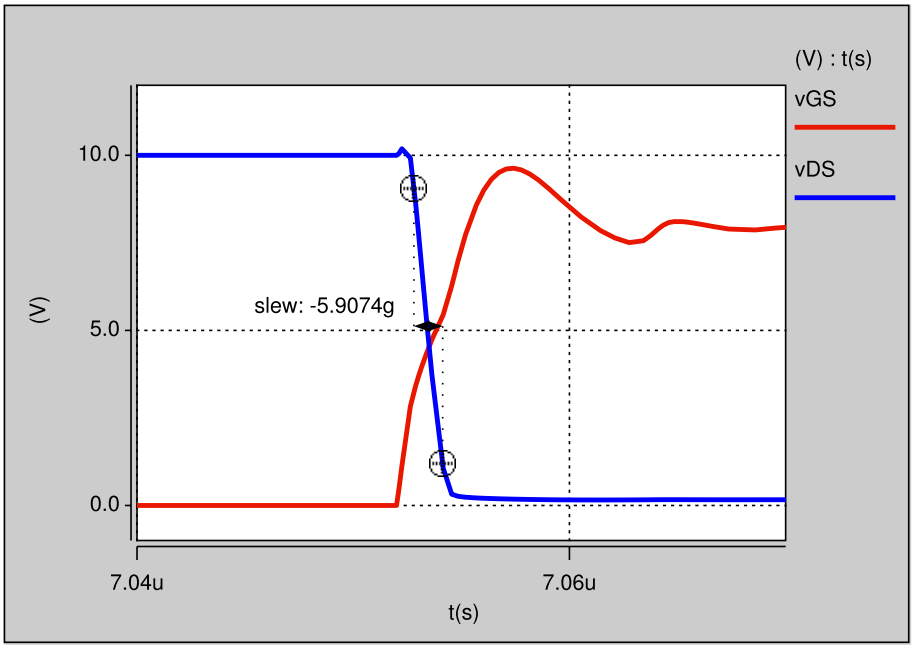

Figure 5.8: Waveforms of drain-source and gate-source voltages of switch M.

switches.

- The gate driver can be utilized for high-frequency power converters.
- Small size energy store components are used in the circuit. The size of L_r is few tens nH. Thus, the loss related to the magnet can be ignored.

5.7 Experimental Verifications

In order to verify the feasibility of the proposed gate driver and corresponding design method, a 6.78 MHz experimental prototype was constructed. It is important to select a MOSFET with low input and output capacitances to allow high switching frequencies to be attained. Moreover, the parasitic inductance of MOSFET should be as low as possible, because high inductance would prevent the desired switching frequency to be realized. The MOSFET AFT05MS003N was used in the high side and low side of the half-bridge. The MOSFET SSM3K336R was chosen as driven transistor in the gate driver. The resistor R_L was connected to the drain-source of the power MOSFET M with power supply V_{dd}. The power MOSFET M is driven by the gate-source voltage v_{GS}, which is obtained from the proposed resonant gate-drive

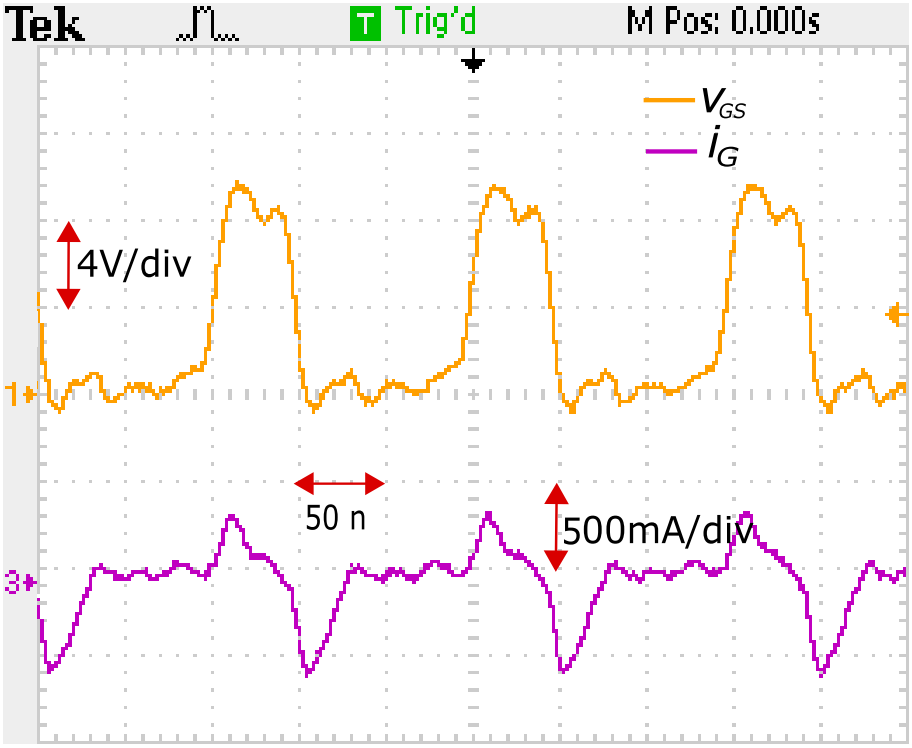

Figure 5.9: Gate-source voltage v_{GS} and gate current i_G of switch M.

circuit.

From Fig. 5.9, it can be observed that the v_{GS} is a rectangular waveform at switching-frequency $f_s = 6.78$ MHz, $V_I = 8$ V, and duty cycle $D = 0.4$. Due to reverse body diode, there is some ripple in the waveform when the switch M turns-OFF. In the same figure, the gate current i_G supplies the charge to the transistor input capacitance C_{iss} during turning ON and OFF. Based on design considerations in Section 5.2, the design parameters of the circuit are provided in Table 5.1.

Table 5.1: Design parameters of the proposed resonant gate-drive circuit.

Components	Value
M	SSM3K336R C_{iss} = 126 pF, C_{oss} = 26 pF, C_{rss} = 8 pF V_{ds} = 30 V, V_{GS} = 20 V, I_{ds} = 3 A Q_g = 1.7 nC, r_{DS} = 0.095 Ω
M_1, M_2	AFT05MS003N C_{iss} = 38.5 pF, C_{oss} = 23.2 pF, C_{rss} = 1.1 pF V_{ds} = 12.5 V, V_{GS} = 12 V, I_{ds} = 2 A Q_g = 0.462 nC, r_{DS} = 0.038 Ω
V_I	8 V
L_r	63 nH
R_L	50 Ω

5.8 Conclusions

A new resonant gate-drive circuit has introduced. The gate driver uses resonance technique for power MOSFETs in enhancement-mode process. Compared with conventional gate drivers, the proposed circuit has fast response at different duty cycles. The circuit is capable to operate over a wide range of switching frequencies. The proposed gate driver was implemented in resistive load operating at 6.78 MHz. The results from the analytical model, SaberRD simulation, and experimental scheme has confirmed the concept and the operation of the gate-drive circuit.

6 High-Frequency Inductor Analysis

6.1 Introduction

Magnetic components are widely employed in many electronic circuits. Air-core inductors are most common choice in variety of applications, such as high-frequency (HF) switched-mode power supplies, communications systems, and wireless power charging [44], [47]. An appropriate model for the air-core inductor is presented to represent the inductor behavior operating at high frequencies. Moreover, a detailed design methodology is presented to predict the dc and ac characteristic of the air-core inductor. The analysis includes an expression to estimate the power loss in the air-core inductor. A design example of air-core inductor is given for switch-mode power gate driver operating at high frequencies.

6.2 Analysis of Air-Core Inductor

Air-core inductor is an integral part of many resonant inverters and filter circuits for high frequency applications. When the frequency increases, the current flows in a narrow skin on the conductor and its resistance increases [48]. Therefore, the winding power loss is a significant contributor to the overall power loss in the resonant gate driver. In this chapter, the behavior of air-core inductor versus high-frequency and ac/dc characteristics are introduced.

6.2.1 Inductance

The photo and invisible components of the air-core inductor is shown in Fig. 6.1. With Nagaoka's coefficient K [48], [49], the total inductance L can be obtained as

$$L = K\frac{\mu_0\mu_{rc}A_cN^2}{l_c} = \frac{\mu_0\mu_{rc}\pi R_c^2N^2}{l_c\left(1+0.9\frac{R_c}{l_c}\right)}, \tag{6.1}$$

where

$$K = \frac{1}{1+0.9\frac{R_c}{l_c}}, \tag{6.2}$$

l_c is the length of the core, R_c is the radius of the core, $A_c = \pi R_c^2$ is core cross-sectional area, μ_{rc} core relative permittivity, and N is the total number of turns.

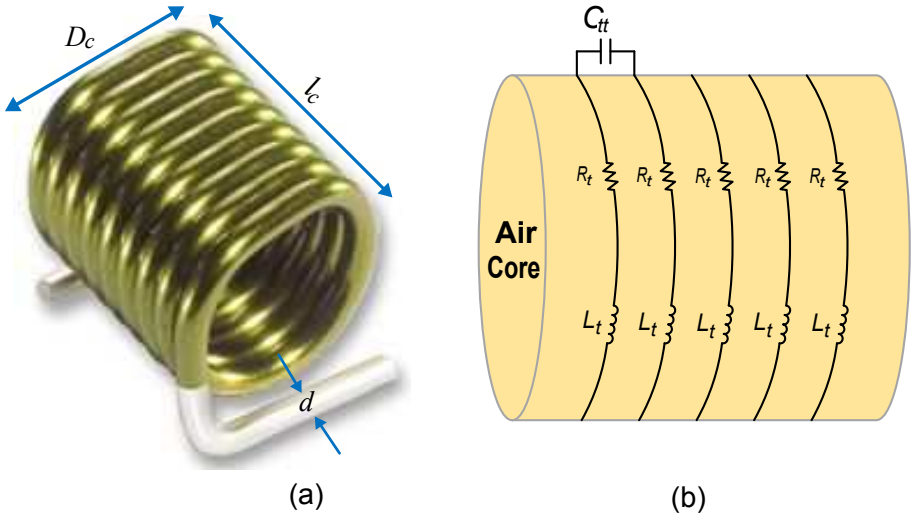

Figure 6.1: Single-layer air-core inductor. (a) Coilcraft air-core inductor. (b) Invisible components of the air-core inductor.

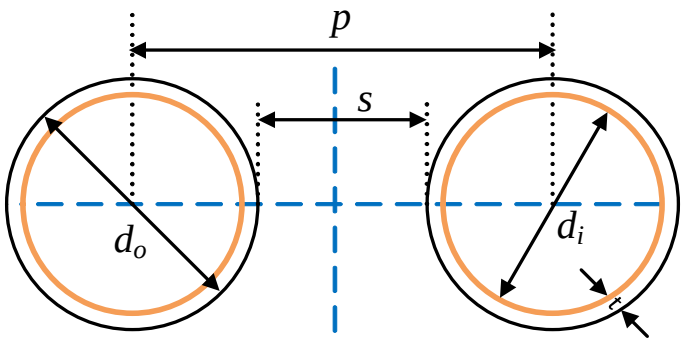

Figure 6.2: Two adjacent round turns of single-layer solenoid inductor with turn separation.

6.2.2 Capacitance

The two adjacent round turns of single-layer solenoid with turn separation is shown in Fig. 6.2. In the figure, d_o and d_i are the outer and inner diameters of the round winding wire, s is the fixed air space at the outer surfaces, and t is the thickness of the wire insulation coating. For a single-layer inductor, the turn-to-turn capacitance C_{tt} with separation between adjacent turns $s = p - d_o$ is [48]

$$C_{tt} = \frac{2\pi\epsilon_0 D_t}{\sqrt{\left(1 + \frac{1}{\epsilon_r}\ln\frac{d_o}{d_i} + \frac{s}{d_o}\right)^2 - 1}} \times \tan^{-1}\left(\sqrt{1 + \frac{2}{\frac{1}{\epsilon_r}\ln\frac{d_o}{d_i} + \frac{s}{d_o}}}\right). \tag{6.3}$$

In (6.3), D_t is the effective coil diameter of one turn, ϵ_0 is the permittivity of free space, ϵ_r is the relative permittivity, and p is the winding pitch. For the outer diameter d_o and the core diameter D_c of one turn, the effective coil diameter is $D_t = D_c + d_o$. The pitch length can be expressed as

$$p = \frac{l_c}{N-1}. \tag{6.4}$$

The total self-capacitance C is

$$C = \frac{C_{tt}}{N-1}. \tag{6.5}$$

Hence, the self-resonant frequency f_{sr} for the air-core inductor with inductance L and capacitance C is

$$f_{sr} = \frac{1}{2\pi\sqrt{LC}}. \tag{6.6}$$

6.2.3 Winding AC Resistance

The air-core inductor can be modeled by the lumped parameter equivalent circuit as shown in Fig. 6.3. In an air-core inductor, the winding ac resistance R_w, the total

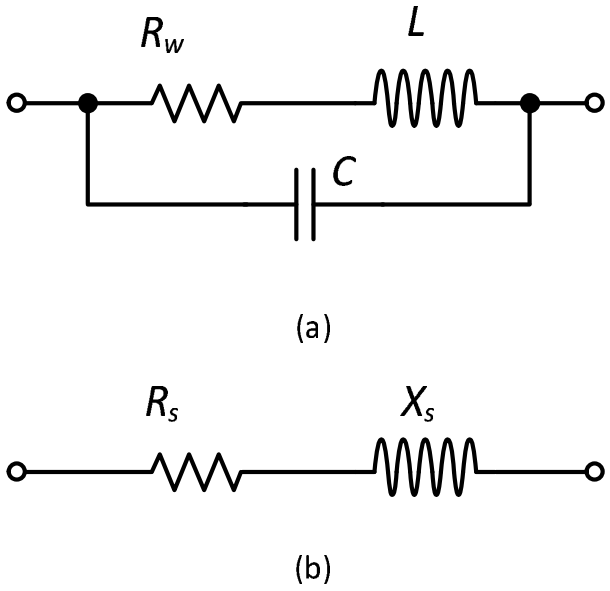

Figure 6.3: High-frequency inductor model. (a) Lumped parameter equivalent circuit. (b) Series equivalent circuit.

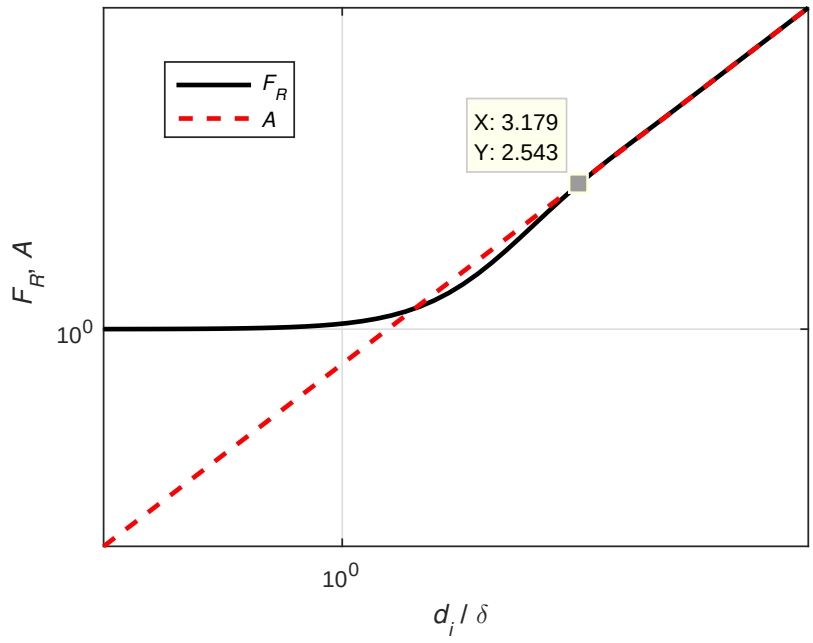

Figure 6.4: F_R and A as functions of d_i/δ.

ac resistance R_s, and the total equivalent reactance X_s can be considered practically dependent of switching frequency f_s. The inductor L and the total capacitance C are considered independent of the switching frequency. If the air-core inductor winding wire has resistivity ρ and number of winding N, the winding dc resistance R_{wdc} can be expressed as

$$R_{wdc} = \rho \frac{l_w}{A_w} = \rho \frac{l_w}{\pi \left(\frac{d_i}{2}\right)^2} = \frac{4}{\pi} \frac{\rho l_w}{d_i^2} = \frac{4}{\pi} \frac{\rho N l_T}{d_i^2}, \tag{6.7}$$

where l_w is total length of the winding, l_T is the average length per turn of winding, and d_i is the wire inner diameter. The ac resistance factor F_R is the ratio of the ac-to-dc resistance of the wire resistance for the inductor,

$$F_R = \frac{R_w}{R_{wdc}} = A \left[\frac{\sinh(2A) + \sin(2A)}{\cosh(2A) - \cos(2A)} \right], \tag{6.8}$$

where A is relative winding wire inner diameter, which depends on the winding geometry and it is unitless quantity. Fig. 6.4 shows the F_R and A functions with respect to d_i/δ. It is clear that the F_R and A functions get closer and equal when $d_i/\delta \geq 3.2$.

The ratio F_R can be approximated according to the following equation:

$$F_R \approx A = \left(\frac{\pi}{4}\right)^{\frac{3}{4}} \sqrt{\eta} \frac{d_i}{\delta} = k \frac{d_o}{\delta} \quad \text{for} \quad \frac{d_i}{\delta} \geq 3.2, \tag{6.9}$$

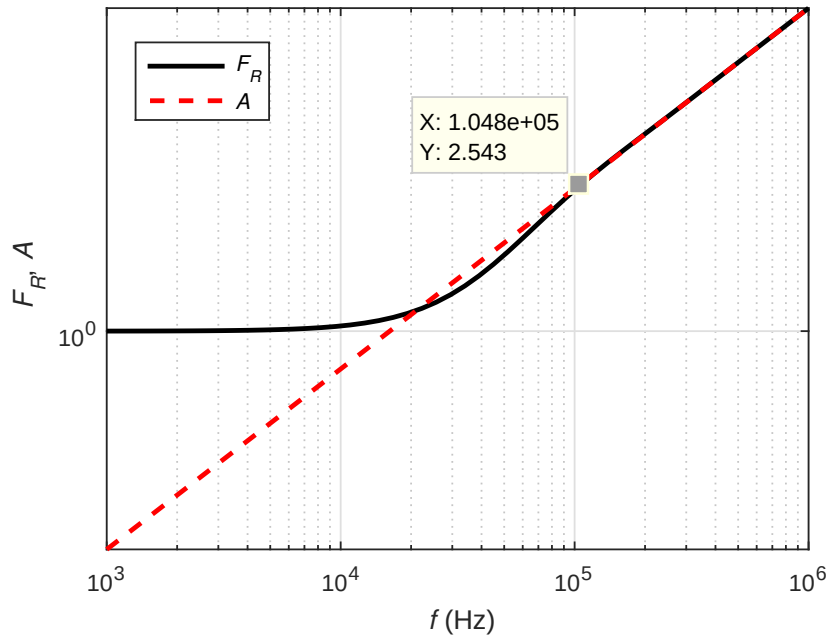

Figure 6.5: F_R and A as functions of frequency f_s.

where $\eta = d_i/p$ is the porosity factor and δ is the winding skin depth. The constant k is

$$k = \left(\frac{\pi}{4}\right)^{\frac{3}{4}} \sqrt{\eta}. \tag{6.10}$$

At switching frequency f_s, the winding wire skin depth of the air-core inductor, which has free-space permittivity μ_0, is [48]

$$\delta = \sqrt{\frac{\rho}{\pi \mu_o f_s}}. \tag{6.11}$$

At high frequencies, the ratio F_R becomes equal to the relative winding wire diameter A as shown in Fig. 6.5. It can be observed that the F_R and A have the same value 104 kHz when the switching frequency f_s is greater than 100 kHz. The ac series winding resistance R_w is given by

$$R_w = R_{wdc} \times F_R = \frac{4}{\pi}\frac{\rho l_w}{d_i^2} \times k\frac{d_i}{\delta} = \frac{4k}{\pi}\frac{N l_T}{d_i}\sqrt{\pi \mu_o \rho f_s}. \tag{6.12}$$

The equivalent series resistance R_s is [50]

$$R_s = \frac{R_w}{\left(1 - \omega^2 LC\right)^2 + \left(\omega C R_w\right)^2}. \tag{6.13}$$

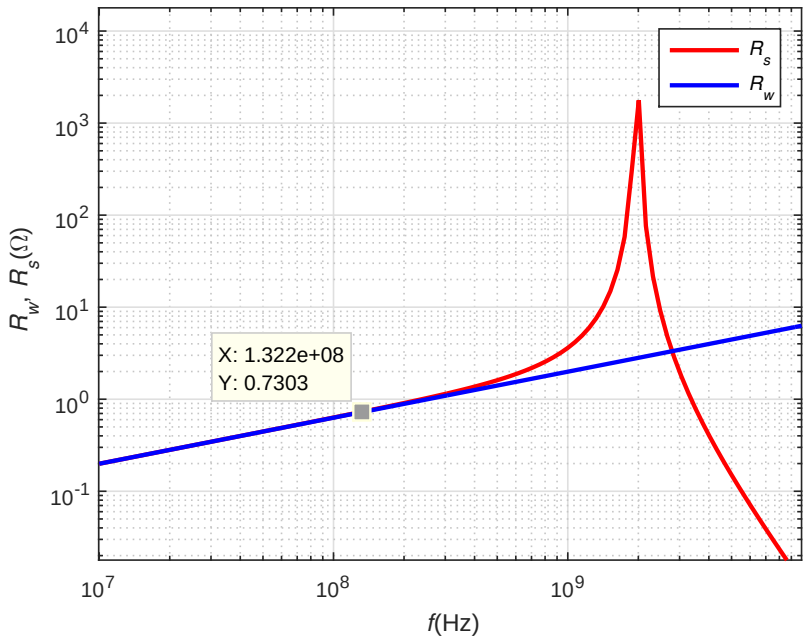

Figure 6.6: The ac resistance R_w and equivalent series resistance R_s as a function of frequency f_s.

The ac resistance R_w and equivalent series resistance R_s are shown in Fig. 6.6. The R_w and R_s are diverged when the frequency is greater than 132 MHz. The ratio of the divergent frequency $f_{b1} = 132$ MHz and self-resonant frequency $f_r = 2$ GHz of the air-core inductor can be expressed as

$$\frac{f_{b1}}{f_r} = \frac{132}{2000} = 6.6\%. \tag{6.14}$$

The ac resistance R_w with respect to the frequency is shown in Fig. 6.7. The resistance R_w increases from 0.065 Ω to 0.365 Ω, as the frequency increases from 1 MHz to 30 MHz. The equivalent series resistance R_s with respect to switching frequency f_s is shown in Fig. 6.8. It can be noticed that resistance R_s increases with respect to the frequency f. Its value is 0.2818 Ω at frequency 20 MHz. Small differences are observed of calculated and directly measured values of the ac resistance R_w and the equivalent series resistance R_s. It can be different from the inductor's material and the accuracy of the impedance analyzer. We considered in our calculation that the inductor is a pure copper metal.

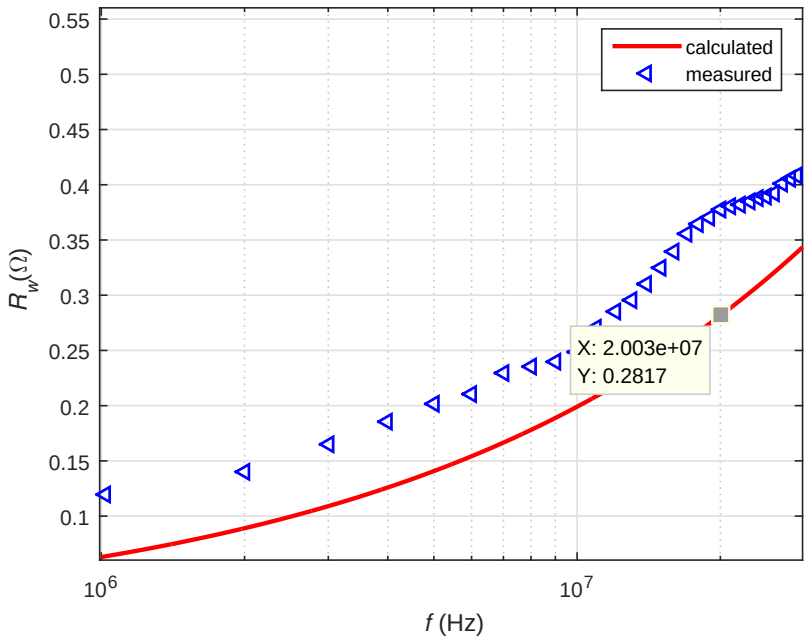

Figure 6.7: The ac winding resistance R_w as functions of frequency f_s.

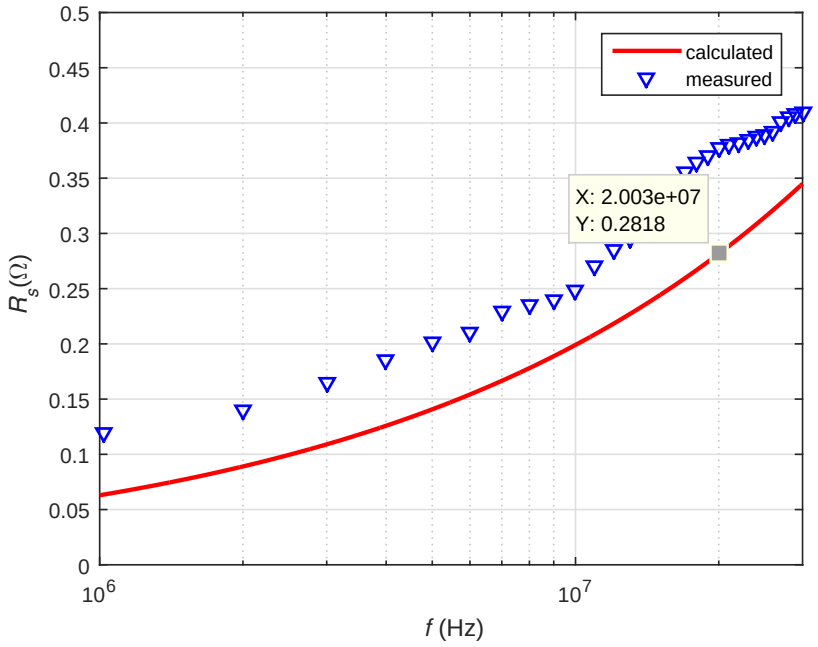

Figure 6.8: Equivalent series resistance R_s as a function of frequency f_s.

The equivalent series reactance X_s is [50]

$$X_s = \omega L \frac{1 - \omega^2 LC - CR_w^2/L}{(1 - \omega^2 LC)^2 + (\omega C R_w)^2}. \tag{6.15}$$

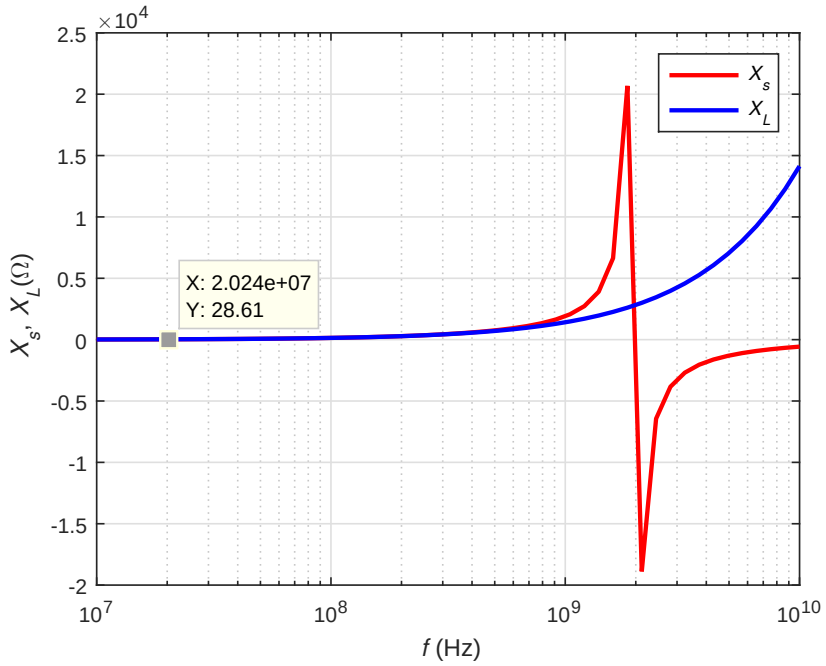

Figure 6.9: The equivalent series reactance X_s and inductor reactance X_L as a function of frequency f_s.

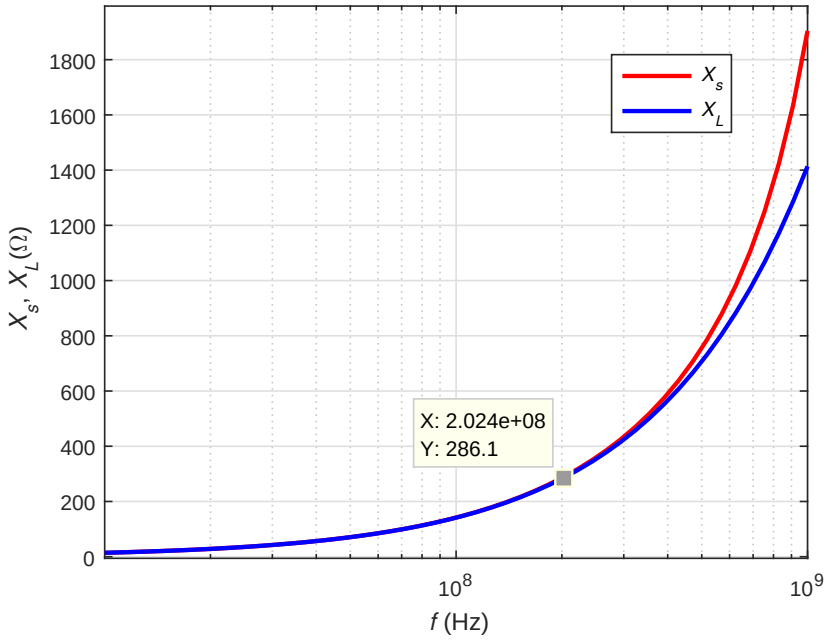

Figure 6.10: The equivalent series reactance X_s and inductor reactance X_L as a function of frequency f_s.

The reactance of the air-core inductor is

$$X_L = 2\pi\omega L. \tag{6.16}$$

Fig. 6.9 shows the equivalent series reactance X_s and the reactance of the air-core inductor X_L. The impedance of the air-core inductor is given by

$$Z_s = R_s + jX_s. \tag{6.17}$$

The equivalent series reactance X_s and the reactance X_L in the frequency range of 10 MHz to 1 GHz are shown in Fig. 6.10. When the frequency is 202 MHz, the divergence is occurred at 286 Ω. The ratio of the divergent frequency $f_{b2} = 202$ MHz and self-resonant frequency $f_r = 2$ GHz of the air-core inductor is

$$\frac{f_{b2}}{f_r} = \frac{202}{2000} = 10.1\%. \tag{6.18}$$

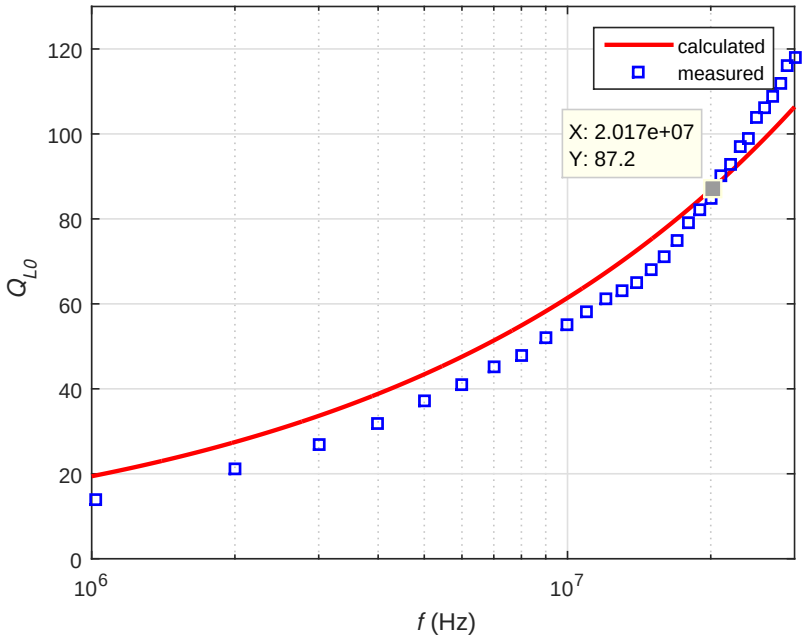

Figure 6.11: Quality factor as a function of frequency f_s.

Table 6.1: Characteristic of the air-core inductor (All dimensions in mm).

Air-core inductor characteristics			
Part number L	2222SQ-221	Radius of the core R_c	2.145
Material	Copper	Length of the core l_c	9
Number of turns N	12	Outer diameter d_o	0.65
Quality factor 20 MHz	120	Inner diameter d_i	0.6

6.2.4 Quality Factor

The quality factor Q_{L0} of an inductor at given frequency f_s is defined as

$$Q_{L0} = \frac{\omega L}{R_w} = \frac{2\pi f_s L}{R_w} = 2\pi f_s L \times \frac{\pi}{4k}\frac{d_i}{l_w\sqrt{\pi\mu_0\rho f_s}} = \frac{\pi^{\frac{3}{2}} d_i L f_s^{\frac{1}{2}}}{2k l_w\sqrt{\mu_o\rho}}. \tag{6.19}$$

The calculated and measured values of the quality factor is shown in Fig. 6.11. It can be observed for frequencies up to 20 MHZ, the air-cor inductor has high quality factor, realizes a more efficient passive component. The physical characteristic of the air-core inductor is shown in Table 6.1

6.3 Winding Power Loss

To determine the power loss of the air-core inductor, the ac resistance R_w can be obtained in three different ways:

1. The ac resistance R_w is calculated by the following expression

$$R_w = \frac{4k}{\pi}\frac{N l_T}{d_i}\sqrt{\pi\mu_o\rho f_s}. \tag{6.20}$$

   The power loss P_L in the air-cor inductor can be found by the rms current $I_{L(rms)}$ of the inductor and the ac resistance R_w

$$P_L = I_{L(rms)}^2 R_w \approx I_{L(rms)}^2 R_s \quad \text{for} \quad \frac{d_i}{\delta} \geq 3.2, \tag{6.21}$$

2. The ac resistance R_w is calculated by quality factor Q_d in the the datasheet

$$R_w = \frac{\omega L}{Q_d}. \tag{6.22}$$

   The loss in the inductor is

$$P_L = I_{L(rms)}^2 R_w. \tag{6.23}$$

3. By using impedance analyzer, the ac resistance R_w is calculated by measuring the quality factor Q_m

$$R_w = \frac{\omega L}{Q_m} \tag{6.24}$$

The loss in the inductor is

$$P_L = I^2_{L(rms)} R_w. \tag{6.25}$$

6.4 Design of Air-Core Inductor

In this section, a step-by-step solution is presented to deign the air-core inductor at high frequency. The air-core inductor is a part of the proposed gate driver as illustrated in Chapter 4. The desired inductance in the resonant gate driver is given by

$$L = \frac{\mu_0 \mu_{rc} \pi R_c^2 N^2}{l_c \left(1 + 0.9 \frac{R_c}{l_c}\right)} = \frac{4\pi \times 10^{-7} \times 1 \times \pi (2.145 \times 10^{-3})^2 12^2}{10 \times 10^{-3} \left(1 + 0.9 \frac{2.145 \times 10^{-3}}{10 \times 10^{-3}}\right)} = 219 \text{ nH}. \tag{6.26}$$

The calculated turn-to-turn capacitance is

$$C_{tt} = \frac{2\pi \epsilon_0 D_t}{\sqrt{\left(1 + \frac{1}{\epsilon_r} \ln \frac{d_o}{d_i} + \frac{s}{d_o}\right)^2 - 1}} \times \tan^{-1} \left(\sqrt{1 + \frac{2}{\frac{1}{\epsilon_r} \ln \frac{d_o}{d_i} + \frac{s}{d_o}}} \right) \tag{6.27}$$

$$= \frac{2 \times 8.854 \times 10^{-12} \times \pi \times 4.94 \times 10^{-3}}{\sqrt{\left(1 + \frac{1}{3.3} \ln \frac{0.65}{0.6} + \frac{0.259}{0.65}\right)^2 - 1}} \times \tan^{-1} \left(\sqrt{1 + \frac{2}{\frac{1}{3.3} \ln \frac{0.65}{0.6} + \frac{0.259}{0.65}}} \right) = 0.319 \text{ pF}.$$

The following parameters are calculated as

$$d_i = d_o - 0.05 = 0.65 - 0.05 = 0.6 \text{ mm}, \tag{6.28}$$

$$p = \frac{l_c}{N-1} = \frac{10}{12-1} = 0.909 \text{ mm}, \tag{6.29}$$

$$s = p - d_o = 0.909 - 0.65 = 0.259 \text{ mm}, \tag{6.30}$$

$$D_c = B - 2d_o = 5.59 - 2 \times 0.65 = 4.29 \text{ mm}, \tag{6.31}$$

and

$$D_t = D_c + d_o = 4.29 + 0.65 = 4.94 \text{ mm}. \tag{6.32}$$

Since the network of turn-to-turn capacitances are in series, the air-core inductor self-capacitance is

$$C = \frac{C_{tt}}{N-1} = \frac{0.319}{12-1} = 0.029 \text{ pF}. \tag{6.33}$$

For the air-core solenoid inductor with inductance L, the self-resonant frequency f_{sr} is

$$f_{sr} = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{219 \times 10^{-9} \times 0.029 \times 10^{-12}}} = 1.998 \text{ GHz}. \tag{6.34}$$

The dc resistance of the air-core inductor is

$$R_{wdc} = \frac{4\rho N l_T}{\pi d_i^2} = \frac{4 \times 1.724 \times 10^{-8} \times 12 \times 2\pi \times 2.145}{\pi \times 0.6^2} = 9.86 \text{ m}\Omega. \tag{6.35}$$

For the copper winding, the skin depth at switching frequency f_s is

$$\delta = \sqrt{\frac{\rho}{\pi\mu_o f_s}} = \sqrt{\frac{1.724 \times 10^{-8}}{\pi \times 4\pi \times 10^{-7} \times f_s}} = \frac{66.11}{\sqrt{f}} = \frac{66.11}{\sqrt{20 \times 10^6}} = 0.01478 \text{ mm}. \tag{6.36}$$

The relative winding inner diameter A at $f_s = 20$ MHz is given by

$$A = k\frac{d_i}{\delta} = 0.705 \times \frac{0.6}{0.01478} = 28.63. \tag{6.37}$$

The ratio of ac-to-dc resistance is approximated as

$$F_R \approx A = 28.63. \tag{6.38}$$

The ac resistance of the air-core winding is calculated as

$$R_w = \frac{4k}{\pi}\frac{N l_T}{d_i}\sqrt{\pi\mu_o\rho f_s} \tag{6.39}$$

$$= \frac{4 \times 0.705}{\pi}\frac{12 \times 2\pi \times 2.145}{0.6}\sqrt{\pi \times 4\pi \times 10^{-7} \times 1.724 \times 10^{-8} \times 20 \times 10^6} = 0.282 \ \Omega.$$

The equivalent series resistance R_s can be calculated as

$$R_s = \frac{R_w}{(1 - \omega^2 LC)^2 + (\omega C R_w)^2} \tag{6.40}$$

$$= \frac{0.282}{(1 - 125.6^2 \times 219 \times 0.029 \times 10^{-9})^2 + (125.6 \times 0.029 \times 10^{-6} \times 0.282)^2} = 0.282 \ \Omega.$$

Also, equivalent series reactance is

$$X_s = \omega L\frac{1 - \omega^2 LC - CR_w^2/L}{(1 - \omega^2 LC)^2 + (\omega C R_w)^2} \tag{6.41}$$

$$= 27.5\frac{1 - 125.6^2 \times 219 \times 0.029 \times 10^{-9} - 37.07 \times 10^{-9}}{(1 - 125.6^2 \times 219 \times 0.029 \times 10^{-9})^2 + (125.6 \times 0.029 \times 10^{-6} \times 0.28)^2} = 28.2 \ \Omega.$$

The impedance of the air-core inductor is

$$Z_s = R_s + jX_s = 0.282 + j28.2. \tag{6.42}$$

The calculated quality factor at 20 MHz is

$$Q_{L0} = \frac{\pi^{\frac{3}{2}} d_i L f_s^{\frac{1}{2}}}{2kNl_T\sqrt{\mu_o\rho}} = \frac{\pi^{\frac{3}{2}} \times 0.6 \times 219 \times 10^{-9} \times (20 \times 10^6)^{\frac{1}{2}}}{2 \times 0.705 \times 12 \times 2 \times \pi \times 2.145\sqrt{4\pi \times 10^{-7} \times 1.724 \times 10^{-8}}} = 87. \tag{6.43}$$

The power loss P_L in the air-cor inductor can be calculated by the rms current $I_{L(rms)} = 0.1324$ A of the inductor and the ac resistance R_w

$$P_L = I_{L(rms)}^2 R_w = 0.1324^2 \times 0.282 = 4.943 \text{ mW}. \tag{6.44}$$

The ac resistance R_w is calculated by quality factor in the the data sheet

$$R_w = \frac{\omega L}{Q_d} = \frac{2\pi \times 20 \times 10^6 \times 219 \times 10^{-9}}{120} = 0.228\ \Omega. \tag{6.45}$$

The power winding loss in the inductor is

$$P_L = I_{L(rms)}^2 R_w = 0.1324^2 \times 0.228 = 4 \text{ mW}. \tag{6.46}$$

The ac resistance R_w is obtained by measuring the quality factor

$$R_w = \frac{\omega L}{Q_m} = \frac{2\pi \times 20 \times 10^6 \times 219 \times 10^{-9}}{97} = 0.283\ \Omega. \tag{6.47}$$

The power winding loss in the inductor is

$$P_L = I_{L(rms)}^2 R_w = 0.1324^2 \times 0.283 = 4.96 \text{ mW}. \tag{6.48}$$

6.5 Conclusions

An analytical approach of air-cor inductor as a function of frequency has been presented. The model allows to investigate the behavior of the air-core inductor at high frequencies. The dc and ac characteristics for the air-core inductor has been evaluated. For high frequencies, the air-core inductor is preferred because its quality factor is high. The ac power loss is significantly higher than dc power loss. Thus, the dc winding loss can be neglected in the air-core inductor. The power loss in the air-core inductor is carried out in terms of ac resistance and quality factor as a function of frequency.

7 Conclusions and Future Work

7.1 Summary

The following topics have been discussed in this dissertation. The main characteristics for Chapter 3 high-frequency single-switch gate driver, Chapter 4 high-frequency single-switch ZVS gate driver based on a class Φ_2 resonant inverter, and Chapter 5 class-D resonant gate driver are:

1. The steady-state waveforms have been analyzed.
2. The expressions for the gate-source voltage and gate current waveforms have been derived.
3. The expressions for the power losses have been derived.
4. The gate drivers are simulated on SaberRD. The design procedure for each gate-drive circuit is presented.
5. The performance of new topologies is also demonstrated via experimental results.

For Chapter 6 high-frequency inductor analysis, the main features are:

1. An appropriate model for the air-core inductor is introduced to represent the inductor behavior operating at high frequencies.
2. A detailed design methodology is presented to predict the dc and ac characteristic of the air-core inductor.
3. An expression to estimate the power loss in the inductor is introduced.
4. A design example of the air-core inductor is given for switch-mode power gate driver operating at high frequencies.

7.2 Conclusions

1. New resonant gate drivers have been introduced.
2. They have low component count and low complexity.
3. The turn-on and turn-off transitions of the driven switches were fast.
4. The proposed circuits were analyzed, designed, simulated, and tested.
5. Lower losses of the gate driver qualify the circuit to operate over a wide range of switching frequencies.
6. The results from the analytical expressions and SaberRD simulations have confirmed the concept and the operation of the gate-drive circuits.
7. The experimental results of the proposed gate-drive circuits are in a good agreement with the the theoretical results.
8. The proposed gate drivers are suitable for telecom and RF applications that operate in the switching-mode from a few MHz to tens of MHz.

7.3 Contributions

The main contributions in this dissertation are:

- New resonant gate drivers have been introduced.
- Detailed analysis of the proposed gate drivers has been performed.
- Expressions for steady-state waveforms and the component values of the proposed gate-drive circuits were derived.
- Expressions for power loss analysis of the gate driver circuits were introduced.
- The theoretical analysis of the gate-drive circuits was validated by simulation results.
- The presented analytical approach of the gate-drive circuits was tested by experimental results.

- The behavior of air-core inductor versus high-frequency and ac-dc characteristics was investigated.

7.4 Future Work

To improve the performance of gate drivers, some aspects can be included in the future:

1. Semiconductor

   Today, semiconductors, especially MOSFETs, are used in low frequency converters. Gate charge and on-resistance are two important design parameters that need to be optimized to achieve high performance in the gate driver. Gallium Nitride is used widely in power converters because it has high electron mobility enabling the switch to make quick transitions. Therefore, GaN can be used in the gate-drive circuit to perform a significant improvement.

2. Non-Linearity

   Analysis of nonlinear behavior of parasitic capacitances in power MOSFETs is important. Detailed analysis of nonlinear parasitic capacitance achieves high accurate design.

3. Thermal Management

   Thermal management is a big challenge when the circuit operates at high switching frequencies. Further efficiency improvement can be achieved when thermal management is considered. Thus, getting heat away is important, such as heat sink and new technologies that can be utilized in the gate drivers.

4. Integration

   Integrating gate-drive circuit with the converter makes the converter low noise, more performance, and high reliability.

5. Electromagnetic Interference (EMI)

   Since high-frequency inductors are used in the gate-drive circuits, it is necessary to study the effect of EMI on the performance of the circuits.

Appendix

This appendix contains the PSPICE library files which are used in MOSFET modeling of the resonant gate drivers. Each file is referred to as class.lib in the simulation.

1. VRF148A

```
**********************************************
*SRC=VRF148;VRF148;MOSFETs N;Enh;170V 6.0A 1.20ohms PPG Microsemi RF
MOSFET
*SYM=POWMOSN * 10-15-09 Rev A GJK PPG Microsemi
.SUBCKT VRF148 10 20 30
* TERMINALS: D G S
M1 1 2 3 3 DMOS L=1U W=1U
LD 10 11 .5n
RD 11 1 1.2
LG 20 19 .88n
RG 19 2 .3
D1 5 1 DGD
D2 5 2 DGD
CGS 2 3 160p
DSD 3 1 DSUB
RS 29 3 2.25m
LS 30 29 .63n
.MODEL DMOS NMOS(LEVEL=3 VMAX=1.04Meg THETA=100.0m ETA=5.00m
VTO=2.90 KP=3.2)
.MODEL DSUB D (IS=99.6n N=1.50 RS=10.4m BV=170 CJO=228p VJ=0.800
M=0.420 TT=300n)
.MODEL DGD D (IS=100n N=1.5 RS=10m BV=170 CJO=12.8p M=.5 VJ=.700
TT=1n)
.ENDS
```

2. MRF136

```
**********************************************
*SRC=MRF136;MRF136;MOSFETs N;RF;28V 500mA Power
*SYM=POWMOSN
* MOTOROLA MRF136 28 V 500 MA
* RF POWER MOSFET
.SUBCKT MRF136 1 2 3
LD 1 9 0.010E-9
```

```
LG 2 7 1.009E-9
LS 3 8 0.921E-9
CC 4 3 13.95E-12
CF 7 9 0.123E-12
RD 4 9 0.08
RG 6 7 0.67
RS 5 8 0.70
DB 5 4 DDB
M1 4 6 5 5 N99 W=1.6 L=0.625
.MODEL N99 NMOS ( KP=0.13E+00 LAMBDA=0.50E-01 PB=0.75 VTO=0.242E+01
+ PHI=0.65 MJ=0.5 IS=0.375E-15 CGDO=3.12E-12 CGSO=35.64E-12 )
.MODEL DDB D ( IS=0.250E-15 CJO=106.5E-12 M=0.5 VJ=0.75 TT=10E-9 )
.ENDS
```

References

[1] M. K. Kazimierczuk, *Radio-Frequency Power Amplifiers*, 2nd. Ed., Wiley, Chichester, UK, 2015.

[2] K. Nagaoka, K. Chikamatsu, A. Yamaguchi, K. Nakahara, and T. Hikihara, "High-speed gate drive circuit for SiC MOSFET by GaN HEMT," *IEICE Electron. Exp.*, vol. 12, no. 11, pp. 1-8, June 2015.

[3] J. Chennu, R. Maheshwari, and H. Li, "New resonant gate drive circuit for high frequency application of silicon carbide MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8277-8287, Oct. 2017.

[4] K. Yao and F. Lee, "A novel resonant gate driver for high frequency synchronous buck converters," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 180-186, March 2002.

[5] Z. Zhang, W. Eberle, P. Lin, Y. Liu, and P. Sen, "A new hybrid gate drive scheme for high frequency buck voltage regulators," in *Proc. IEEE Power Electron. Specialist Conf.,* Rhodes, Greece, June 2008, pp. 2498-2504.

[6] H. Fujita, "A resonant gate-drive circuit capable of high-frequency and high-efficiency operation," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 962-969, Apr. 2010.

[7] S. Yin, K. Tseng, C. Tong, and R. Simanjorang, "Design of high-speed gate driver to reduce switching loss and mitigate parasitic effects for SiC MOSFET," *IET Power Electron.*, vol. 10, no. 10, pp. 1183-1189, Aug. 2017.

[8] Y. Chen, F. Lee, L. Amoroso, and H. Wu, "A resonant MOSFET gate driver with efficient energy recovery," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 470-477, Mar. 2004.

[9] W. Eberle, Y. Liu, and P. Sen, "A new resonant gate-drive circuit with efficient energy recovery and low conduction loss," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 2213-2221, May 2008.

[10] I. Mashhadi, E. Ovaysi, E. Adib, and H. Farzanehfard, "A novel current-source gate driver for ultra-low-voltage applications," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4796-4804, Aug. 2016.

[11] Y. Chen, F. Lee, L. Amoroso, and H. Wu, "A resonant MOSFET gate driver with efficient energy recovery," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 470-477, Mar. 2004.

[12] D. Maksimovic, "A MOS gate drive with resonant transitions," in *Proc. IEEE Power Electron. Specialist Conf.*, Cambridge, MA, 1991, pp. 527-532.

[13] J. Strydom, M. Rooij, and J. Wyk, "A comparison of fundamental gate-driver topologies for high frequency applications," *IEEE Applied Power Electron. Conf. and Expo.*, Anaheim, CA, 2004, pp. 1045-1052.

[14] L. Balogh, "Fundamentals of MOSFET and IGBT gate driver circuits," *Application Report*, Texas Instrument, pp. 1-47, March 2017.

[15] M. Theodoridis and S. Mollov, "Robust MOSFET driver for RF, class-D inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 731-740, Feb. 2008.

[16] K. Peng and E. Santi, "Class E resonant inverter optimized design for high frequency (MHz) operation using eGaN HEMTs," in *Proc. IEEE Appl. Power Electron. Conf. and Expo.*, Charlotte, NC, March 2015, pp. 2469-2473.

[17] F. Raab, "Class-E, class-C, and class-F power amplifiers based upon a finite number of harmonics," *IEEE Trans. Microw. Theory and Techn.*, vol. 49, no. 8, pp. 1462-1468, Aug. 2001.

[18] J. Rivas, Y. Han, O. Leitermann, A. Sagneri, and D. Perreault, "A high-frequency resonant inverter topology with low-voltage stress," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1759-1771, July 2008.

[19] A. Juhas and L. Novak, "Comments on class-E, class-C, and class-F power amplifier based upon a finite number of harmonics", *IEEE Trans. Micro. Theo. and Techn.*, vol. 23, no. 4, June 2009.

[20] K. Lee, E. Chung, Y. Han, and J. Ha, "A family of high-frequency single-switch DC-DC converters with low switch voltage stress based on impedance networks," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2913-2924, Apr. 2017.

[21] M. K. Kazimierczuk, "Exact analysis of class E tuned power amplifier with only one inductor and one capacitor in load network," *IEEE J. Solid-State Circuits*, vol. 18, no. 2, pp. 214-221, Apr. 1983.

[22] M. K. Kazimierczuk, "Class E tuned power amplifier with nonsinusoidal output voltage," *IEEE J. Solid-State Circuits*, vol. 21, no. 4, pp. 575-581, Aug. 1986.

[23] S. Aldhaher, D. Yates, and P. Mitcheson, "Modeling and analysis of class EF and class E/F inverters with series-tuned resonant networks," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3415-3430, May 2016.

[24] J. Burkhart, R. Korsunsky, and D. Perreault, "Design methodology for a very high frequency resonant boost converter," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1929-1937, Apr. 2013.

[25] R. Podgurski, A. Sagneri, J. Rivas, D. Anderson, and D. Perreault, "Very-high-frequency resonant boost converters," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1654-1665, June 2009.

[26] M. K. Kazimierczuk, "High-efficiency class E, EF_2, and E/F_3 inverters," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1584-1593, Oct. 2006.

[27] X. Ren, Y. Zhou, D. Wang, X. Zou, and Z. Zhang, "A 10-MHz isolated synchronous class-Φ_2 resonant converter," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8317-8328, Dec. 2016.

[28] J. Xue and H. Lee, "A 2-MHz 60-W zero-voltage-switching synchronous non-inverting buck-boost converter with reduced component values," *IEEE Trans. Circuit and Syst.*, vol. 62, no. 7, pp. 716-720, July 2015.

[29] G. Hua and F. C. Lee, "Soft-switching techniques in PWM converters," *IEEE Trans. Indus. Electron.*, vol. 42, no. 6, pp. 595-603, Dec. 1995.

[30] X. Li, A. Huang, S. Guo, X. Deng, B. Zhang, and X. She, "A SiC power MOSFET loss model suitable for high-frequency applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8268-8276, Oct. 2017.

[31] M. Swamy, T. Kume, and N. Takada, "An efficient resonant gate-drive scheme for high-frequency applications," *IEEE Trans. Ind. Applications*, vol. 48, no. 4, pp. 1418-1431, July-Aug. 2012.

[32] M. K. Kazimierczuk, *Pulse-width Modulated DC-DC Power Converters*, John Wiley and Sons, 2nd Ed., Chichester, UK, 2015.

[33] K. Gopalakrishna, *Frequency Characterization of Si, SiC, and GaN MOSFETs Using Buck Converter in CCM as an application*, M.S. Thesis, Wright State University, Dayton, USA, 2013.

[34] A. Goldberg and J. Kassakian, "The application of power MOSFETs at 10 MHz," in *Proc. IEEE Power Electron. Specialist Conf.*, June 1985, pp. 91-100.

[35] D. Reusch and J. Strydom, "Evaluation of gallium nitride transistors in high frequency resonant and soft-switching DC-DC converters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5151-5158, Sep. 2015.

[36] K. Rajagopalan, J. Abrokwah, R. Droopad, and M. Passlack, "Enhancement-mode GaAs n-channel MOSFET," *IEEE Electron Device Let.*, vol. 27, no. 12, pp. 959-962, Dec. 2006.

[37] S. Musumeci, "Gate charge control of high-voltage silicon-carbide (SiC) MOSFET in power converter applications," in *Proc. IEEE Power Electron. Specialist Conf.*, Taormina, June 2015, pp. 709-715.

[38] M. K. Kazimierczuk, *Resonant Power Converters*, John Wiley and Sons, 2nd Ed., Chichester, UK, 2011.

[39] Y. Kuwata, Y. Ohashi, and K. Yotsumoto, "Characteristics of a new series-resonant converter with a parallel resonant circuit," in *Proc. IEEE Int. Telecom. Energy Conf.*, Stockholm, Sweden, 1987, pp. 204-210.

[40] J. Warren, K. Rosowski, and D. Perreault, "Transistor selection and design of a VHF DC-DC power converter," *IEEE Trans. Power Electron.*, vol. 23, pp. 27-37, Jan. 2008.

[41] J. Rivas, O. Leitermann, Y. Han, and D. Perreault, "A very high frequency dc-dc converter based on a class Φ_2 resonant inverter," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2980-2992, Oct. 2011.

[42] B. Wang, N. Tipirneni, M. Riva, A. Monti, G. Simin, and E. Santi, "An efficient high-frequency drive circuit for GaN power HFETs," *IEEE Trans. Ind. App.*, vol. 45, no. 2, pp. 843-853, April 2009.

[43] S. Yin, K. Tseng, C. Tong, and R. Simanjorang, "Design of high-speed gate driver to reduce switching loss and mitigate parasitic effects for SiC MOSFET," *IET Power Electron.*, vol. 10, no. 10, pp. 1183-1189, Aug. 2017.

[44] D. Saini, A. Ayachit, A. Reatti, and M. K. Kazimierczuk, "Analysis and design of choke inductors for switched-mode power inverters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2234-2244, March 2018.

[45] A. Knott, T. Andersen, P. Kamby, J. Pedersen, M. Madsen, M. Kovacevic, and M. Andersen, "Evolution of very high frequency power supplies," *IEEE J. Power Electron.*, vol. 2, no. 3, pp. 386-394, Sep. 2014.

[46] R. Chen and F. Peng, "A high-performance resonant gate-drive circuit for MOSFETs and IGBTs," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4366-4373, Aug. 2014.

[47] A. Ayachit and M. K. Kazimierczuk, "Self-capacitance of single-layer inductors with separation between conductor turns," *IEEE Trans. Electromagn. Compat.*, vol. 59, no. 5, pp. 1642-1645, Oct. 2017.

[48] M. K. Kazimierczuk, "*High-Frequency Magnetic Components*, 2nd. Ed. Chichester, U.K.: Wiley, 2014.

[49] H. Nagaoka, "The inductance coefficients of solenoids," *J. Coll. Sci.*, vol. 27, no. 3, pp. 1-33, Aug. 1909.

[50] U. Reggiani, G. Grandi, G. Sancineto, and G. Serra, "Comparison between air-core and laminated iron-core inductors in filtering applications for switching converters," in *Proc. IEEE Int. Power Electron. Conf.*, Acapulco, Mexico, 2000, pp. 9-14.