2019

Tapped-Inductor Buck DC-DC Converter

Ankit Chadha
Wright State University

TAPPED-INDUCTOR BUCK DC-DC CONVERTER

A dissertation submitted in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

By

ANKIT CHADHA

M.S.E.E., Wright State University, 2015

B.Tech., Koneru Lakshmaiah University, India, 2013

2019

Wright State University

WRIGHT STATE UNIVERSITY
GRADUATE SCHOOL

December 06, 2019

I HEREBY RECOMMEND THAT THE DISSERTATION PREPARED UNDER MY SUPERVISION BY Ankit Chadha ENTITLED Tapped-Inductor Buck DC-DC Converter BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Doctor of Philosophy.

Marian K. Kazimierczuk, Ph.D.
Dissertation Director

Fred D. Garber, Ph.D.
Interim Chair, Department of Electrical Engineering, College of Engineering and Computer Science

Barry Milligan, PhD.
Interim Dean of the Graduate School

Committee on Final Examination:

Yan Zhuang, Ph.D.

Lavern Alan Starman, Ph.D.

Michael A. Saville, Ph.D., P.E.

Saiyu Ren, Ph.D.

ABSTRACT

Chadha, Ankit., Ph.D., Department of Electrical Engineering, Wright State University, 2019. *Tapped-Inductor Buck DC-DC Converter.*

There is a high demand for low step-down dc voltage conversions. Many conventional power converters that are currently being used have a moderate conversion ratio and this may not be sufficient to meet the demand. This can be achieved by either cascading power converters or using converters with a low step-down conversion ratio. Cascading the convertors increases the power conversion stage complexity and increase the order of the system, while also effecting the stability. Using converters with high conversion ratio seem to be a more intelligent option to root. This dissertation tackles to analyze one such converter, called tapped-inductor buck dc-dc converter.

A tapped-inductor buck dc-dc converter, capable to produce higher conversion ratios compared to the conventional converters is used. An analysis describing a detailed steady-state operation of the converter is provided. The expected voltage and current waveforms across different components at different point of time during the entire operation of the converter are analytically derived. Design equations for the converter have also been provided. Power lost across various converter components are predicted. The overall converter efficiency is calculated.

The dynamics of the system are predicted. For this a model of the tapped-inductor buck dc-dc converter is derived using circuit averaging technique. Transfer functions relating the output to the input and the control voltages are derived. Various poles and zeros effecting the system magnitude and phase plots were analytically defined.

A controller closed-loop system is implemented. Various time and frequency domain parameters effecting the system response are measured and compared to the open-loop system.

All the theoretically obtained responses are implemented using MATLAB and verified using saber circuit simulator. The verified model responses from the simulations are also validated through hardware implementation.

Contents

List of Figures

Acknowledgement

To start of, I would like to express my immense gratitude to my advisor Dr. Marian K. Kazimierczuk, whose support, motivation and wisdom has helped me through out my research. I would also like to thank my committee members Dr. Yan Zhuang, Lavern Alan Starman, Dr. Mike Saville and Dr. Saiyu Ren for their insightful comments and suggestions. I am grateful to the Department of Electrical Engineering and the Department Chair, for giving me this opportunity to obtain my Ph.D degree at Wright State University. Last but not the least I would like to thank my family, who stood by me on every decision I made and who have always showed me the right path.

1 Introduction

Obtaining a sustainable energy production at lowered costs has always been a global priority. This has lead to many improvements in technologies. Power electronic converters with their many available topologies, which help interface different energy sources is an example of one such technology. Power electronic converters use MOSFETs, driven by pulse width modulated (PWM) pulses, as switches to produce output voltage. Hence, they are named switch-mode dc-dc converters. The turn-on time and the turn-off time of these switches play an important role deciding the characteristics of the converter as they provide conversion ratio for these converters.

Since power electronic converters provide good conversion ratio, a proper regulation of the duty cycle can help in controlling the output voltage. A controller can be employed for such application. The main task of a controller is to sense a change in a required quantity and provide proper compensation, when the situations asks for it. Power electronic converters like, a dc-dc buck or a dc-dc boost converter employ such controllers to keep the output voltage in desired range. In this proposal the converter in question in tapped-inductor current dc-dc converter. A type III controller will be designed and implemented on this converter and analyzed through the remainder of this document.

1.1 Motivation

Power convertors are rapidly used in many industries. My first hand experience for the design and implementation of one such power converter would come to me during internship at Delphi, Kokomo. The goal of our project was to develop a power supply for a fully functional electrical vehicle. Multiple power converter topologies were used for stepping up and down the voltages for different requirements. A single supply in the form of a battery is used to run the vehicle and serve the remaining entertainment

and convenience in the vehicle. For the different levels of power conversions based on the requirements are made. Even for charging the battery the power converters are used for fast and efficient charging. Most of the converters in the project used were conventional buck and boost converter which provide a good voltage conversions. But the voltage conversion in these converters are linear in nature . If higher conversion ratios are required, cascading the converters could help us achieve the task at hand. This not only makes the power conversion complex but also adds to the circuit density. As each convertor stage will require its own driver and control stage. But there are many other topologies available in the market which can provide better conversion ratios. One such converter is a tapped-inductor buck dc-dc converter. Having this knowledge became a motivation for me to provide a good analytical background to the scientific community to support the use of tapped-inductor buck dc-dc converter and make it more convenient and easily available converter in the market.

1.2 Dissertation Objectives

- Analyse the operation and derive the design equations for tapped-inductor buck dc-dc converter.
- Model the converter and characterize the tapped-inductor buck dc-dc converter by deriving input voltage-output voltage transfer function (M_v) and control-to-output voltage transfer function (T_p)
- Design and implement a controller for a designed converter. This helps obtain a tuned and controlled output.
- Use SABER circuit simulator to implement the designed converter along with controller and verify the obtained theoretical responses.
- Using hardware implementation to verify the SABER simulations.

1.3 Overview

The following proposal has been divided in to seven different chapters

- **Chapter** 2**:** Steady-state analysis of the tapped-inductor buck dc-dc converter running in continuous-conduction mode (CCM) has been presented. The gain offered by the converter is calculated. Design equations have been derived. Mathematical equations to represent the converter waveforms have been presented. Power lost across each and every parasitic is calculated. An equation representing the over all efficiency of the converter is derived. Design example has been used to verify the designed converter using a circuit simulator and hardware implementation.

- **Chapter** 3**:** Steady-state analysis of the tapped-inductor buck dc-dc converter running in discontinuous-conduction mode (DCM) has been presented. The gain offered by the converter is calculated. The effect of load on the dc gain has also been represented. Mathematical equations to represent the converter waveforms have been presented. Power lost across each and every parasitic is calculated. An equation representing the over all efficiency of the converter is derived. Design example has been used to verify the designed converter using a circuit simulator and hardware implementation.

- **Chapter** 4**:** In this chapter a linearized-averaged model to analyze the converter has been derived using circuit averaging technique.

- **Chapter** 5**:** The characteristics of the converter is presented. Frequency-domain transfer functions have been derived for the same. MATLAB and circuit simulations are used to obtain and verify the model. The model was also verified by using the switching circuit during the hardware implementation.

- **Chapter 6:** Here the voltage mode control has been introduced. Loop-gain of the converter in question is using to design the required controller. The closed-loop was designed to satisfy common industrial standards for a controlled converter.

- **Chapter 7:** The responses obtained from the over all closed-loop system namely, the closed-loop input-to-output voltage response (M_{vcl})and closed-loop control-to-output voltage responses (T_{pcl}) were analytically derived and verified using MATLAB, SABER circuit simulator and hardware implementation

2 Steady-State Analysis of the Power Stage in CCM

Wide voltage conversion ratio power electronic converters are in great demand, especially in applications such as data centers, point-of-load power supplies, renewable energy sources, and battery-operated portable devices. The tapped-inductor buck converter is capable of providing a much wider step-down than that produced by a conventional buck converter[1]-[10]. Here a complete steady-state analysis for converter operation in continuous-conduction mode is presented. The main objectives of this chapter are:

1. To analyze the steady-state converter current and voltage waveforms during the switch ON and OFF intervals.

2. To determine the expressions required to design the converter components.

3. To derive the expression for the total power loss and hence the overall efficiency of the converter.

Using a design example of a tapped-inductor buck converter, the theoretical predictions are validated through circuit simulations performed on SABER simulation software.

2.1 Principle of Operation

The principle of operation of the tapped-inductor buck converter is similar to that of a conventional buck converter. A circuit representing a tapped-inductor buck dc-dc converter can be seen in Fig. 2.1. The tapped-inductor network provides a wide voltage step down depending on the selected turns ratio n[1]. The input and the output terminals of the tapped-inductor are hereby referred to as primary and secondary, respectively. The magnetizing inductance is placed across the secondary winding of the tapped-inductor. The magnetizing inductance performs the same task

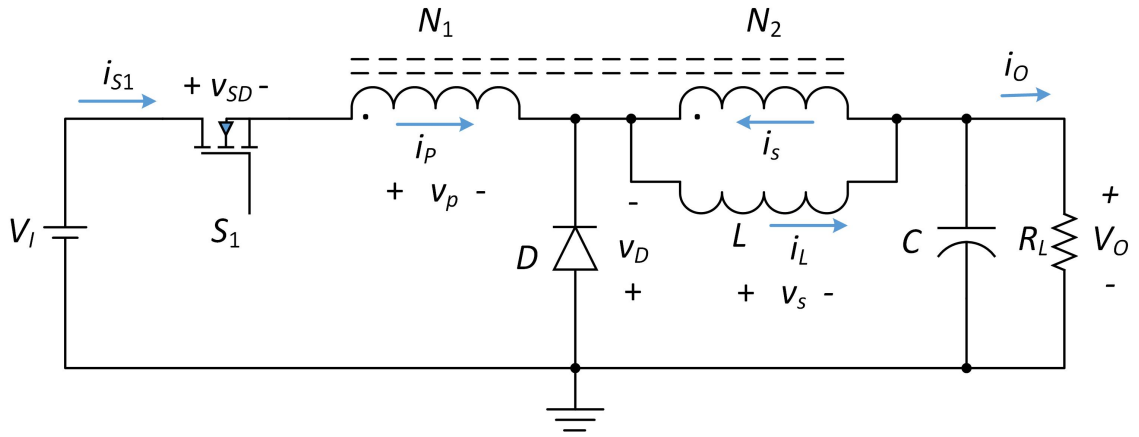

Figure 2.1: Circuit of a PWM tapped-inductor buck converter.

as the filter inductor in traditional buck converter. The primary and the secondary voltages and currents of the tapped-inductor are related as[1]

$$\frac{v_p}{v_s} = \frac{i_s}{i_p} = n - 1 = \frac{N_1}{N_2}, \tag{2.1}$$

where the turns ratio

$$n = \frac{N_1}{N_2} + 1. \tag{2.2}$$

In (2.1), v_p is the primary-winding voltage, v_s is the secondary-winding voltage, N_1 is the number of primary turns, and N_2 is the number of secondary turns.

2.1.1 Time Interval: $0 < t \leq DT$

In this time interval, the switch S_1 is ON the diode is OFF. The sub-circuit relevant to this time interval is shown in Fig. 2.2. The input voltage is in series with the magnetizing inductance L of the tapped-inductor. Fig. 2.4 represents the idealized theoretical waveforms of PWM tapped buck dc-dc converter running in CCM. Applying Kirchhoff's voltage law, the voltage across L is

$$v_L = v_s = V_I - V_O - v_p. \tag{2.3}$$

Since $v_p = (n-1)v_s$,

$$v_s = V_I - V_O - (n-1)v_s. \tag{2.4}$$

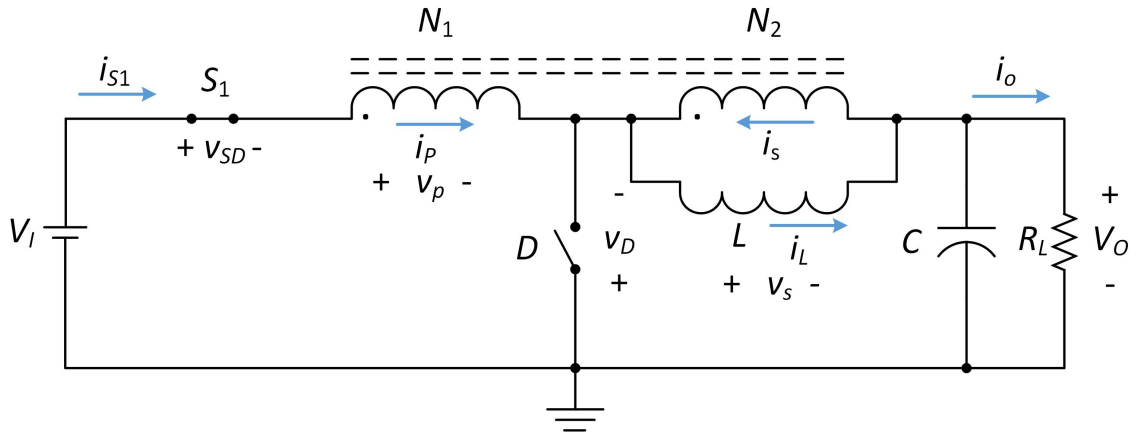

Figure 2.2: Equivalent circuit of the tapped-inductor buck converter for the interval $0 < t \leq DT$.

Solving (2.4) for the secondary side voltage or the inductor voltage produces

$$v_s = v_L = \frac{V_I - V_O}{n}. \tag{2.5}$$

The current through the inductance L is

$$i_L(t) = \frac{1}{L}\int_0^t v_L dt = \frac{V_I - V_O}{nL}t + i_L(0). \tag{2.6}$$

Therefore, the peak-to-peak value of the current through L is

$$\Delta i_L = i_L(DT) - i_L(0) = \frac{V_I - V_O}{nL}DT. \tag{2.7}$$

Applying Kirchhoff's current law, the relationship between the switch current, inductor current and the secondary side current is given by

$$i_{S1}(t) = i_L(t) - i_s(t). \tag{2.8}$$

Since $i_p = i_{S1}$ and $i_s = (n-1)i_p$, the secondary side current is related to the switch current as

$$i_s = (n-1)i_{S1}. \tag{2.9}$$

Substituting (2.9) into (2.84) produces

$$i_{S1}(t) = i_L(t) - (n-1)i_{S1}(t) = \frac{i_L(t)}{n}. \tag{2.10}$$

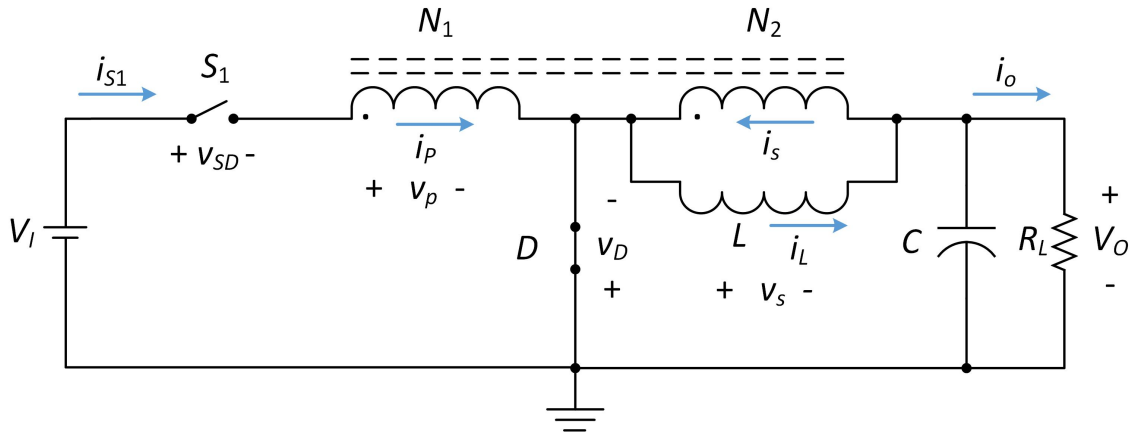

Figure 2.3: Equivalent circuit of the tapped-inductor buck converter for the interval $DT < t \leq T$.

Substituting (2.6) into (2.10), the instantaneous switch current is

$$i_{S1}(t) = \frac{i_L(t)}{n} = \frac{V_I - V_O}{n^2 L} t + \frac{i_L(0)}{n} \tag{2.11}$$

and the peak-to-peak value of switch current is

$$\Delta i_{S1} = i_{S1}(DT) - i_{S1}(0) = \frac{V_I - V_O}{n^2 L} DT. \tag{2.12}$$

The voltage across the switch v_{S1} and the current through the diode i_D are zero. The voltage across the diode v_D is

$$v_D = -(v_s + V_O). \tag{2.13}$$

Substituting (2.5) into (2.13) produces

$$v_D = -\left(\frac{V_I - V_O}{n} + V_O\right) = -\frac{V_I + (n-1)V_O}{n}. \tag{2.14}$$

2.1.2 Time Interval: $DT < t \leq T$

In this time interval, the switch S_1 is OFF and the diode is ON. The sub-circuit relevant to this time interval is shown in Fig. 2.3. The magnetizing inductance current flows to the output and charges the capacitor. Using Kirchhoff's voltage law, the voltage

across the secondary winding is

$$v_{S1} = V_I - (v_P + v_S + V_O). \tag{2.15}$$

Using KVL on the output side loop to get

$$v_S = -V_O. \tag{2.16}$$

Substitute (2.1) and (2.15) into (2.16) to get

$$v_{S1} = V_I - (-(n-1)V_O - V_O + V_O) = V_I + (n-1)V_O \tag{2.17}$$

and the current through the switch i_{S1} is zero. The voltage across the inductor is given by

$$v_L = -V_O. \tag{2.18}$$

The current through the diode i_D is equal to the sum of magnetizing inductance current i_L and secondary side cirrent i_S.

$$i_D(t) = i_L(t) + i_s(t). \tag{2.19}$$

Since the MOSFET switch is off the current flowing through the primary is zero. This results in the current flowing through the secondary of the tapped-inductor buck to also be equal to zero.

$$i_s(t) = 0. \tag{2.20}$$

Therefore, the diode current flows through the inductor and is given by

$$i_D(t) = i_L(t) = \frac{1}{L}\int_{DT}^{t} v_L dt = -\frac{V_O}{L}(t - DT) + i_L(DT). \tag{2.21}$$

Therefore, the the peak-to-peak value of diode current is

$$\Delta i_D = i_D(T) - i_D(DT) = -\frac{V_O}{L}(1 - D)T. \tag{2.22}$$

The voltage across the diode v_D is equal to zero.

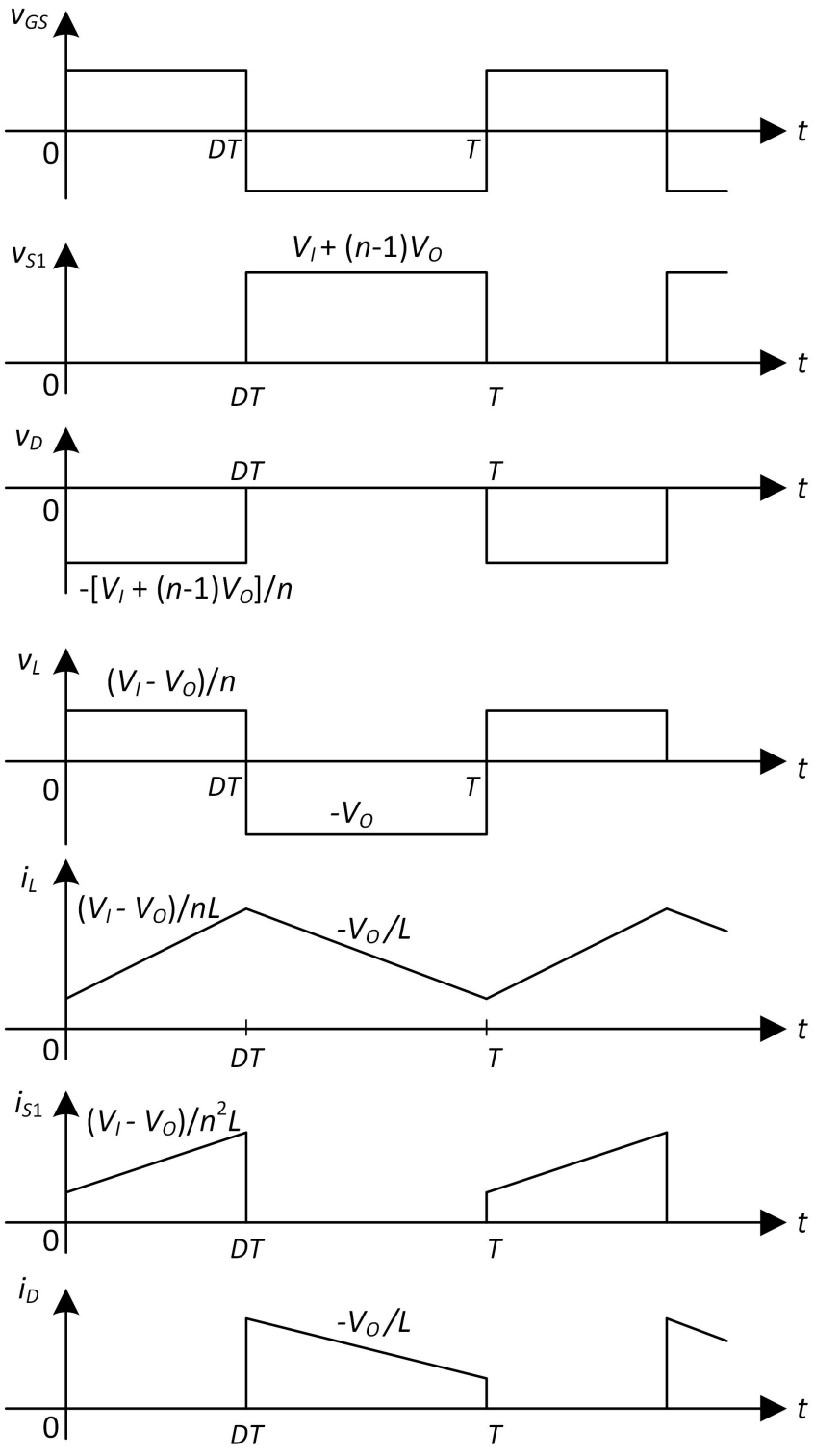

Figure 2.4: Key current and voltage waveforms of the tapped-inductor buck converter.

2.2 DC Voltage and current Ratios

The principle of volt-second balance states that the average steady-state dc voltage across the inductor is equal to zero. Applying this theory to L gives

$$\int_0^{DT} v_L dt = \int_{DT}^{T} v_L dt. \tag{2.23}$$

From (2.5), (2.18) and (2.23), we get

$$\frac{V_I - V_O}{n} D = V_O(1 - D). \tag{2.24}$$

Therefore, the dc input-to-output voltage transfer function of the tapped-inductor buck converter in CCM is

$$M_{VDC} = \frac{V_O}{V_I} = \frac{D}{D + n(1 - D)}. \tag{2.25}$$

Fig. 2.5 shows the plot representing the variation in dc voltage gain with respect to duty cycle. For an ideal converter, the input power is equal to the output power

$$V_O I_O = V_I I_I. \tag{2.26}$$

Therefore, the dc input-to-output current transfer function is

$$M_{IDC} = \frac{I_O}{I_I} = \frac{D + n(1 - D)}{D}. \tag{2.27}$$

2.3 Minimum Inductance

At the boundary between CCM and DCM, the maximum value of inductor current for the converter to be in CCM as obtained from (2.6) is

$$\Delta i_{Lmax} = \frac{V_I - V_O}{nL_{min}} DT = V_O \frac{1 - M_{VDC}}{nL_{min} M_{VDC}}. \tag{2.28}$$

The dc currents through the load can be obtained as

$$I_{OB} = \frac{1}{T} \int_0^T i_L dt - I_S = \frac{\Delta i_{Lmax}}{2} - I_I(n - 1). \tag{2.29}$$

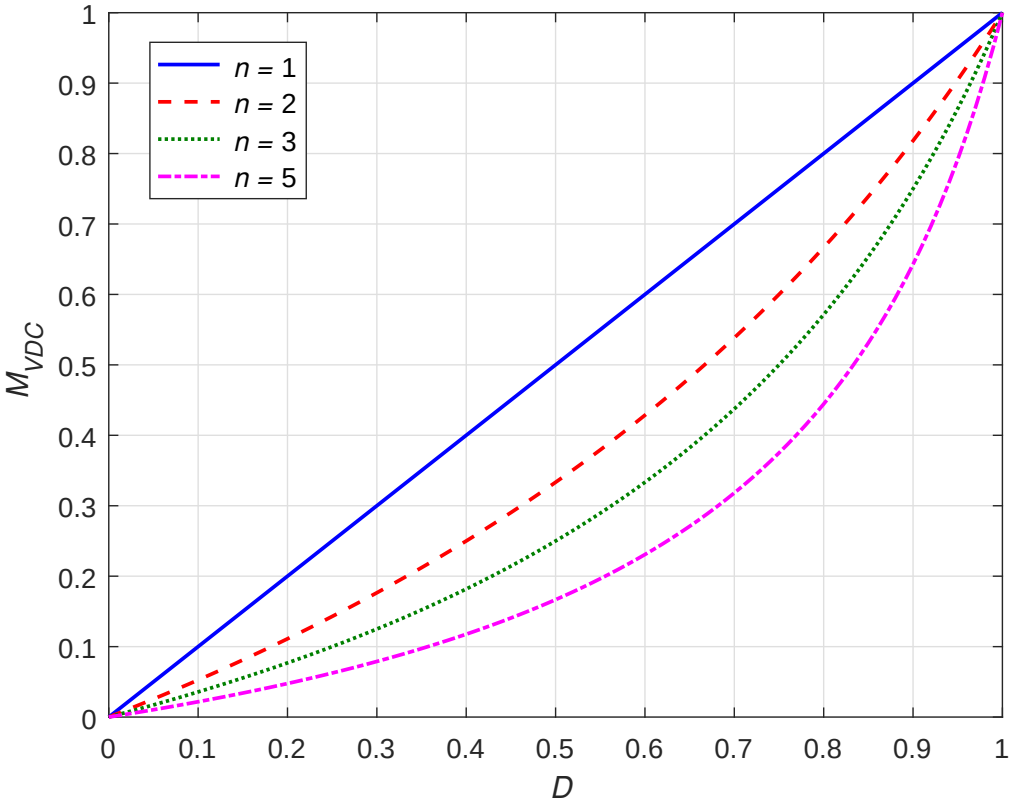

Figure 2.5: DC voltage gain as a function of duty cycle at selected turns ratios.

Equation (2.29) can be simplified for Δi_{Lmax} to get

$$\Delta i_{Lmin} = 2I_{Omin}\left[1 - M_{VDC}(n-1)\right]. \tag{2.30}$$

Equating (2.28) to (2.30), the maximum inductance the tapped-inductor can offer to maintain the converter in DCM is given by

$$L_{min}=\frac{R_L D\left(1 - M_{VDC}\right)}{2nf_s M_{VDC}[1+M_{VDC}\left(n-1\right)]}=\frac{R_L D(1-D)}{2nf_s M_{VDC}}. \tag{2.31}$$

A plot representing the boundary between CCM and DCM can be seen in Fig. 2.6

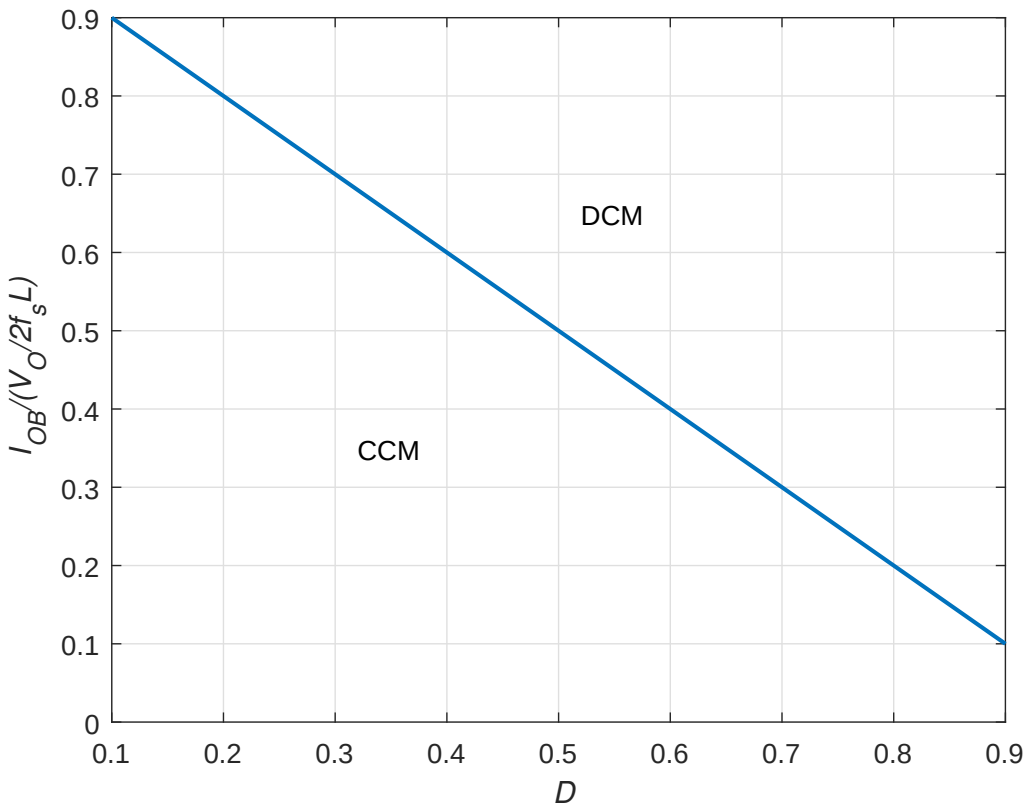

Figure 2.6: Normalized output current as a function of the duty cycle.

2.4 Filter Capacitance

The ac components of the currents through the secondary winding and the magnetizing inductance flow through the filter capacitor and expressed as

$$i_c = \frac{\Delta i_O}{dt} t - \frac{\Delta i_O}{2}. \tag{2.32}$$

Assuming r_C is the equivalent series resistance of the filter capacitor, the voltage across r_C is given by

$$v_{rc} = r_C i_C = r_C \Delta i_O \left(\frac{t}{DT} - \frac{1}{2} \right). \tag{2.33}$$

The voltage across the capacitor is

$$v_c = \frac{1}{C} \int_0^t i_C dt + v_C(0) = \frac{\Delta i_O}{C} \int_0^t \left(\frac{t}{DT} - \frac{1}{2} \right) dt + v_c(0) = \frac{\Delta i_O}{2C} \left(\frac{t^2}{DT} - t \right) + v_c(0). \tag{2.34}$$

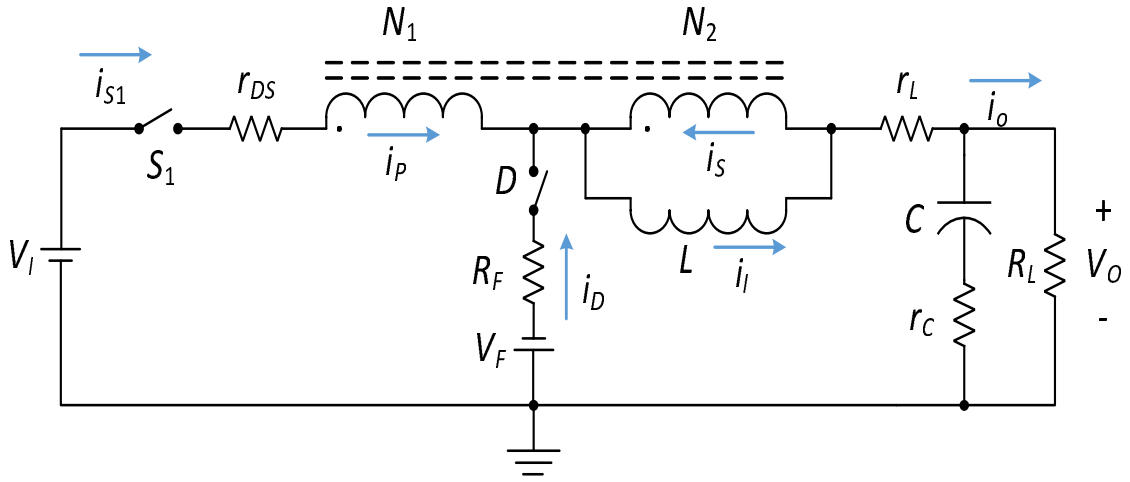

Figure 2.7: Circuit of tapped-inductor buck converter including the parasitic components.

In steady-state $v_c(DT) = v_(0)$ making the voltage waveform a parabolic function. As the ac component is responsible for the ripple. The total voltage across the filter capacitor is expressed as

$$v_o = v_{rc} + v_c = \Delta i_O \left[\frac{t^2}{2CDT} + \left(\frac{r_C}{DT} - \frac{1}{2C} \right) t - \frac{r_C}{2} \right] + v_c(0). \tag{2.35}$$

The rate of change of capacitor voltage is

$$\frac{dv_o}{dt} = \Delta i_O \left(\frac{t}{CDT} + \frac{r_C}{DT} - \frac{1}{2C} \right). \tag{2.36}$$

Setting this to zero. The minimum ac output voltage occurs at

$$t_{min} = \frac{DT}{2} - r_C C. \tag{2.37}$$

Therefore, the minimum filter capacitance is

$$C_{min} = \frac{D}{2 f_s r_C}. \tag{2.38}$$

2.5 Power Losses and Efficiency

An equivalent circuit representing a lossy tapped-inductor buck dc-dc converter is shown in Fig. 2.7. The resistor r_{DS} represents the MOSFET on-resistance, R_F is the

diode forward resistance, V_F is the diode threshold voltage, and r_L and r_C are ESRs of the tapped-inductor and the filter capacitor, respectively. During the time interval $0 < t \leq DT$, from Fig. 2.7, the inductor current on the primary winding is

$$i_L = i_{S1} + i_S \tag{2.39}$$

and the secondary winding current is

$$i_L = i_O + i_S. \tag{2.40}$$

Using (2.1), (2.39), and (2.40), the switch current is

$$i_{S1} = \begin{cases} I_O & 0 < t \leq DT \\ 0 & DT < t \leq T. \end{cases} \tag{2.41}$$

The rms value of switch current is

$$I_{S1rms} = \sqrt{\frac{1}{T}\int_0^T i_{S1}^2 dt} = \sqrt{\frac{1}{T}\int_0^T I_O^2 dt} = I_O\sqrt{D}. \tag{2.42}$$

The conduction loss in the switch is

$$P_{rDS} = r_{DS} I_{S1rms}^2 = r_{DS} I_O^2 D = \frac{r_{DS} D}{R_L} P_O. \tag{2.43}$$

The switching loss is expressed as

$$P_{sw} = \frac{f_s C_o V_o^2}{M_{VDC}^2} = \frac{f_s C_o R_L}{M_{VDC}} P_O, \tag{2.44}$$

where C_o is the transistor output capacitance. Therefore, the total switch power loss is

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2}, \tag{2.45}$$

By substituting (2.43) and (2.44) into (2.45) results in

$$P_{FET} = \left[\frac{r_{DS}(n-1)^2 D}{R_L} + \frac{f_O C_O R_L}{2M_{VDC}^2}\right] P_O. \tag{2.46}$$

The diode current is

$$i_D = \begin{cases} 0 & 0 < t \leq DT \\ I_O & DT < t \leq T. \end{cases} \tag{2.47}$$

The rms diode current is

$$I_{Drms} = \sqrt{\frac{1}{T}\int_0^T i_D^2 dt} = \sqrt{\frac{1}{T}\int_0^T I_O^2 dt} = I_O\sqrt{1-D}. \tag{2.48}$$

The power loss in R_F is

$$P_{RF} = R_F I_{Drms}^2 = (1-D)R_F I_O^2 = \frac{(1-D)R_F}{R_L}P_O. \tag{2.49}$$

The average diode current is

$$I_D = \frac{1}{T}\int_0^T i_D dt = \frac{1}{T}\int_{DT}^T I_O dt = (1-D)I_O. \tag{2.50}$$

The power loss associated with the forward diode voltage V_F is

$$P_{VF} = V_F I_D = V_F(1-D)I_O = \frac{(1-D)V_F}{V_O}P_O. \tag{2.51}$$

The total power loss in the diode is

$$P_D = P_{RF} + P_{VF} = (1-D)\left(\frac{V_F}{V_O} + \frac{R_F}{R_L}\right)P_O. \tag{2.52}$$

The magnetizing inductance current during each switching sub-interval is

$$i_L = \begin{cases} \dfrac{n}{D+(1-D)n}I_O & 0 < t \le DT \\ I_O & DT < t \le T. \end{cases} \tag{2.53}$$

The rms magnetizing inductance current is

$$\begin{aligned} I_{Lrms} &= \sqrt{\frac{1}{T}\int_0^T i_L^2 dt} = \sqrt{\frac{1}{T}\left(\int_0^{DT}\frac{n^2}{(D+(1-D)n)^2}I_O^2 dt + \int_{DT}^T I_O^2 dt\right)} \\ &= I_O\sqrt{\left(\frac{n^2}{(D+(1-D)n)^2} - 1\right)D + 1}. \end{aligned} \tag{2.54}$$

The power loss in r_L is

$$P_{rL} = r_L I_{Lrms}^2 = r_L\left[\left(n^2-1\right)D+1\right]I_O^2 = r_L\left(\left(\frac{n^2}{D+(1-D)n} - 1\right)D + 1\right)\frac{P_O}{R_L}. \tag{2.55}$$

The current through the capacitor is

$$i_C = \begin{cases} \dfrac{\Delta i_o}{DT}t - \dfrac{\Delta i_o}{2} & 0 < t \leq DT \\ \dfrac{\Delta i_o (t - DT)}{(1-D)T} - \dfrac{\Delta i_o}{2} & DT < t \leq T. \end{cases} \tag{2.56}$$

The rms capacitor current is

$$I_{Crms} = \sqrt{\frac{1}{T}\int_0^T i_C^2 dt} = \frac{\Delta i_o}{\sqrt{12}}. \tag{2.57}$$

The ac component of the magnetizing inductance and the secondary winding currents flow through the filter capacitor power resulting in its conduction loss given by

$$P_{rC} = r_C i_{Crms}^2 = r_C \frac{\Delta i_o^2}{12} = r_C \frac{[\Delta i_L - (n-1)\Delta i_{S1}]^2}{12}. \tag{2.58}$$

Substituting (2.7) and (2.12) into (2.58), we get

$$P_{rC} = \frac{r_C R_L (1-D)^2}{12 L^2 f_o^2} P_O. \tag{2.59}$$

The total power loss is

$$P_{LS} = P_{r_{DS}} + P_{sw} + P_D + P_{rL} + P_{rC}. \tag{2.60}$$

Substituting (2.43), (2.44), (2.52), (2.55), and (2.59) into (2.60) yields the total power loss as a function of the output power as

$$\begin{aligned} P_{LS} = \Bigg\{ & \frac{r_{DS} D}{R_L} + \frac{f_s C_o R_L}{M_{VDC}} + (1-D)\left(\frac{V_F}{V_O} + \frac{R_F}{R_L}\right) \\ & + \frac{r_L \left[\left(\dfrac{n^2}{(D+(1-D)n)^2} - 1\right) D + 1\right]}{R_L} + \frac{r_C R_L (1-D)^2}{12 L^2 f_o^2} \Bigg\} P_O. \end{aligned} \tag{2.61}$$

Therefore, the overall efficiency of the converter is

$$\eta = \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \dfrac{P_{LS}}{P_O}}. \tag{2.62}$$

The voltage gain of the non-ideal converter is given by

$$M_{VDClossy} = \frac{\eta D}{D + n(1-D)}. \tag{2.63}$$

2.6 Simulation Validation of the Analysis of the Power Stage Running in CCM in Time-Domain

A tapped-inductor buck converter with the following specifications is considered: $V_I = 12$ V, $f_s = 100$ kHz, $P_O = 2.5$ W, and $V_O = 5$ V. The tapped-inductor turns ratio is $n = 2$. The parasitic of the components are $r_L = 0.5\ \Omega$, $r_{DS} = 55$ mΩ, $R_F = 25$ mΩ, and $V_F = 0.7$ V.

The load resistance is

$$R_L = \frac{V_O^2}{P_O} = 10\ \Omega. \tag{2.64}$$

The required voltage gain from the specification is

$$M_{VDC} = \frac{V_O}{V_I} = 0.42. \tag{2.65}$$

The duty cycle required for this gain can be calculated from (2.25)

$$D = \frac{nM_{VDC}}{1 + (n-1)M_{VDC}} = 0.59. \tag{2.66}$$

The minimum inductance required for the converter to run in CCM can be calculated from (2.31)

$$L_{min} = \frac{R_L(1-D)D}{2nf_sM_{VDC}} = 14.38\ \mu\text{H}. \tag{2.67}$$

Let $L = 115\ \mu$H/500 mΩ

The maximum inductor ripple current is

$$\Delta i_{Lmax} = \frac{V_O(1-D)}{2f_sL} = 0.13\ \text{A}. \tag{2.68}$$

The ripple voltage is assumed to be 2% of V_O

$$V_r = \frac{V_O}{100} = 0.5\ \text{mV}. \tag{2.69}$$

The maximum ESR of the filter capacitor is given by

$$r_{Cmax} = \frac{V_r}{\Delta i_{Lmax}} = 0.72\ \Omega. \tag{2.70}$$

The minimum filter capacitor is given by

$$C_{min} = \frac{D}{2f_s r_C} = 29.41\ \mu\text{F} \tag{2.71}$$

Let $C = 160\ \mu\text{F}/r_C = 50\ \text{m}\Omega$. The selected MOSFET and diode were IRF540 and MBR10100 by vishay semiconductors.

The conduction loss in the switch is

$$P_{rDS} = \frac{r_{DS} D}{R_L} P_O = 8.25\ \text{mW}. \tag{2.72}$$

The switching loss is expressed as

$$P_{sw} = \frac{f_s C_o R_L}{M_{VDC}} P_O = 0.72\ \text{mW}, \tag{2.73}$$

where $C_o = 100$ pF is the transistor output capacitance.

The total power loss in the diode is

$$P_D = (1 - D)\left(\frac{V_F}{V_O} + \frac{R_F}{R_L}\right) P_O = 0.1496\ \text{W}. \tag{2.74}$$

The power loss in r_L is

$$P_{rL} = r_L \left(\left(\frac{n^2}{D + (1 - D)n} - 1\right) D + 1\right) \frac{P_O}{R_L} = 0.20\ \text{W}. \tag{2.75}$$

The power loss in the filter capacitor is

$$P_{rC} = \frac{r_C R_L (1 - D)^2}{12 L^2 f_o^2} P_O = 6.07\ \mu\text{W}. \tag{2.76}$$

The total power loss is

$$P_{LS} = P_{r_{DS}} + P_{sw} + P_D + P_{rL} + P_{rC} = 0.35\ \text{W}. \tag{2.77}$$

Therefore, the overall efficiency of the converter is

$$\eta = 100 \times \frac{P_O}{P_O + P_{LS}} = 87.55\%. \tag{2.78}$$

The voltage gain of the non-ideal converter

$$M_{VDClossy} = \eta M_{VDC} = 0.37. \tag{2.79}$$

Thus, the output voltage under loss operation is $V_O = 4.59$ V. The new duty cycle to achieve $V_O = 5$ V is $D = 0.62$. The theoretical results were verified using SABER circuit simulator. Fig. 2.8 shows the dc voltage transfer function M_{VDC} as a function of duty cycle using (2.63) and was verified through simulations. Fig. 2.9 shows the simulated waveforms of the gate-to-source voltage, drain-to-source voltage, magnetizing inductance current, and output voltage. Fig. 2.10 shows the simulated waveforms of the drain-to-source voltage, switch current, diode current, and diode voltage. The average output voltage is $V_O = 4.49$ V. The maximum switch and diode voltage stresses were $V_{S1} = 17.6$ V and $V_D = -8.35$ V, respectively. The inductor voltage, when the switch is ON was $V_L = 3.57$ V. The peak-to-peak switch current was $\Delta i_{S1} = 87$ mA. The peak-to-peak value of the diode current was $\Delta i_{D1} = 189$ mA. The peak-to-peak value of the magnetizing inductance current was $\Delta i_L = 185$ mA. The theoretical and simulation results were in good agreement with each other. Fig. 2.11 shows the simulated input power and output power waveforms of the tapped-inductor buck converter. The average input power was $P_I = 2.36$ W and the average output power was $P_O = 2.11$ W. Therefore, the overall efficiency was $\eta = 0.89$, which was in agreement with the theoretical calculations.

The steady-state analysis of the pulse-width modulated (PWM) tapped-inductor buck dc-dc converter in continuous-conduction mode has been performed. The steady-state waveforms have been analyzed and the expressions to design the converter components have been derived. The expressions for the total power loss and the overall converter efficiency have been derived. An example tapped-inductor buck converter was designed and simulated using SABER simulation software. The tapped-inductor provides a much wider step-down than the traditional buck topology in single-stage

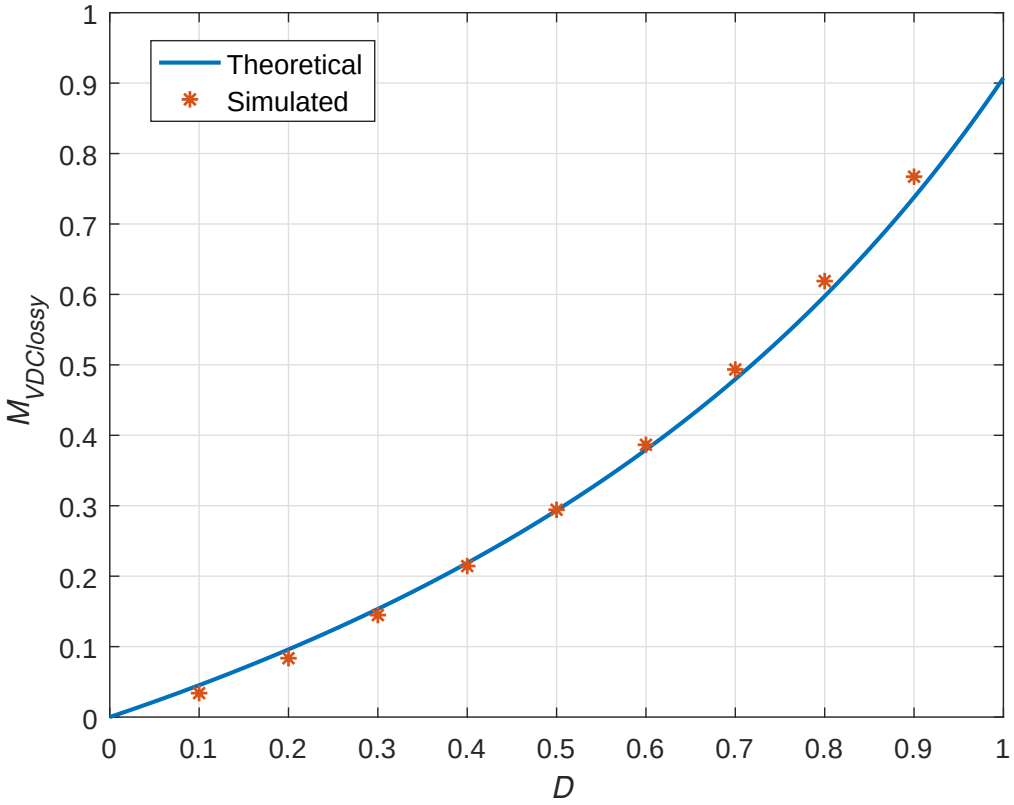

Figure 2.8: Comparison of theoretical and simulated dc voltage gain as functions of duty cycle.

voltage conversion.

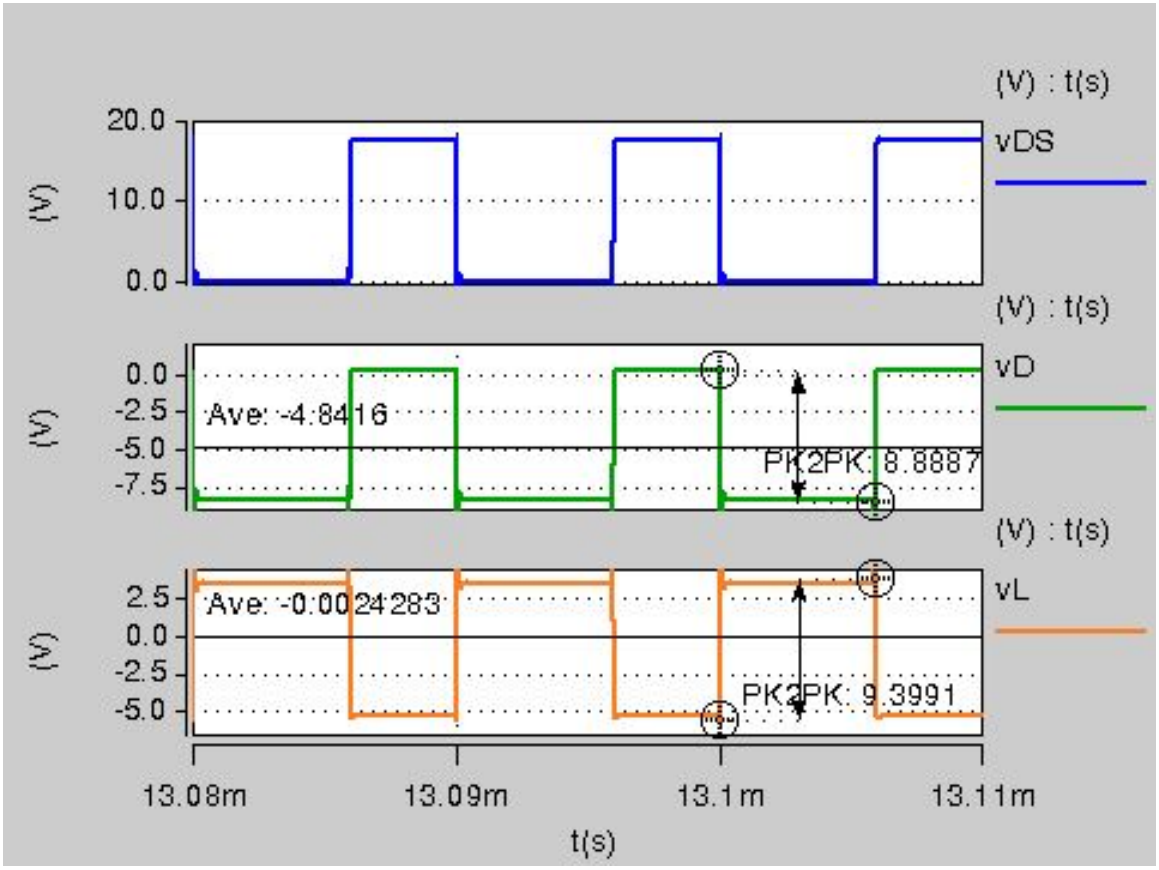

Figure 2.9: Simulated waveforms of the gate-to-source voltage, drain-to-source voltage, inductor current, and output voltage.

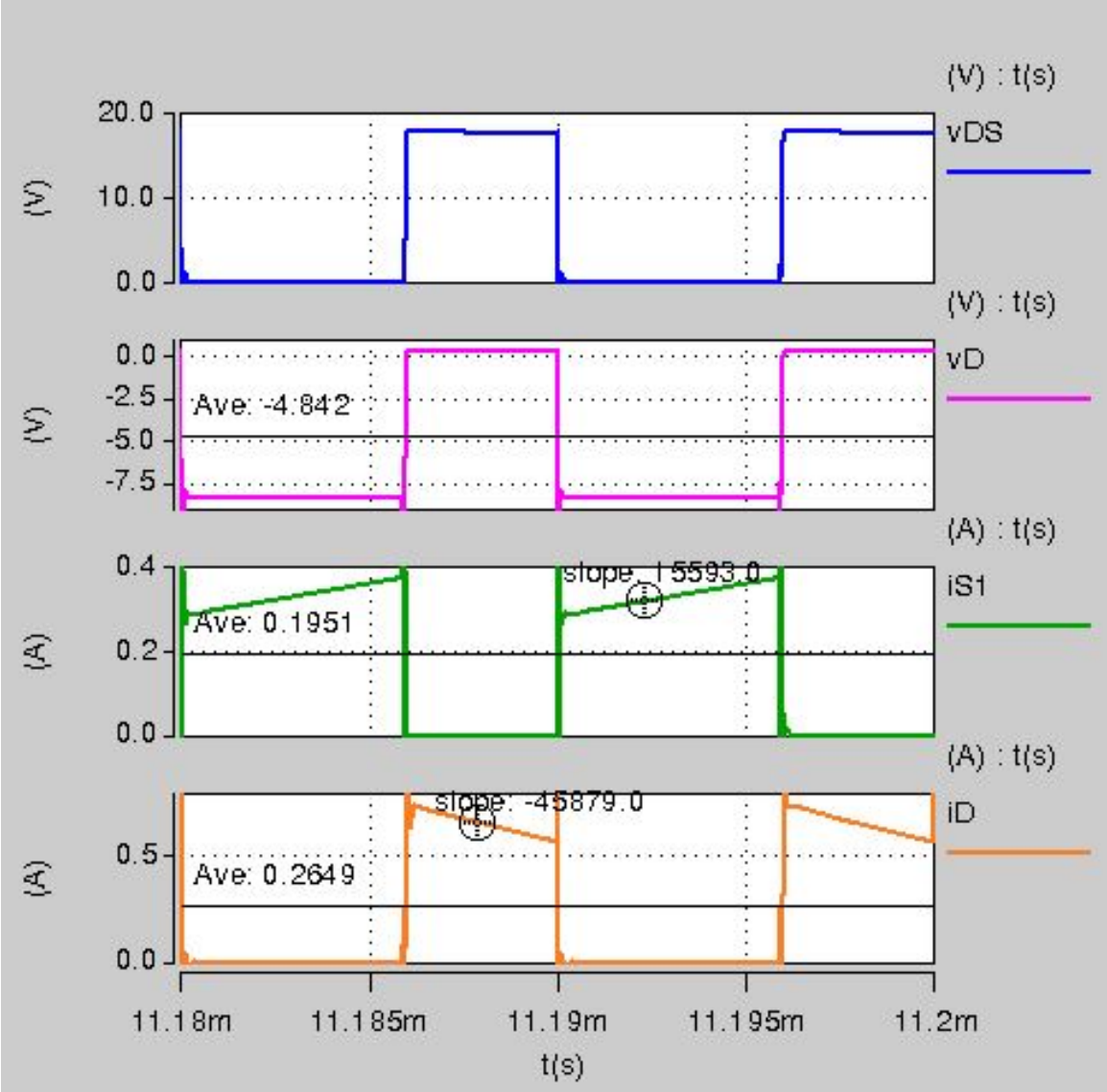

Figure 2.10: Simulated waveforms of the drain-to-source voltage, switch current, diode current, and diode voltage.

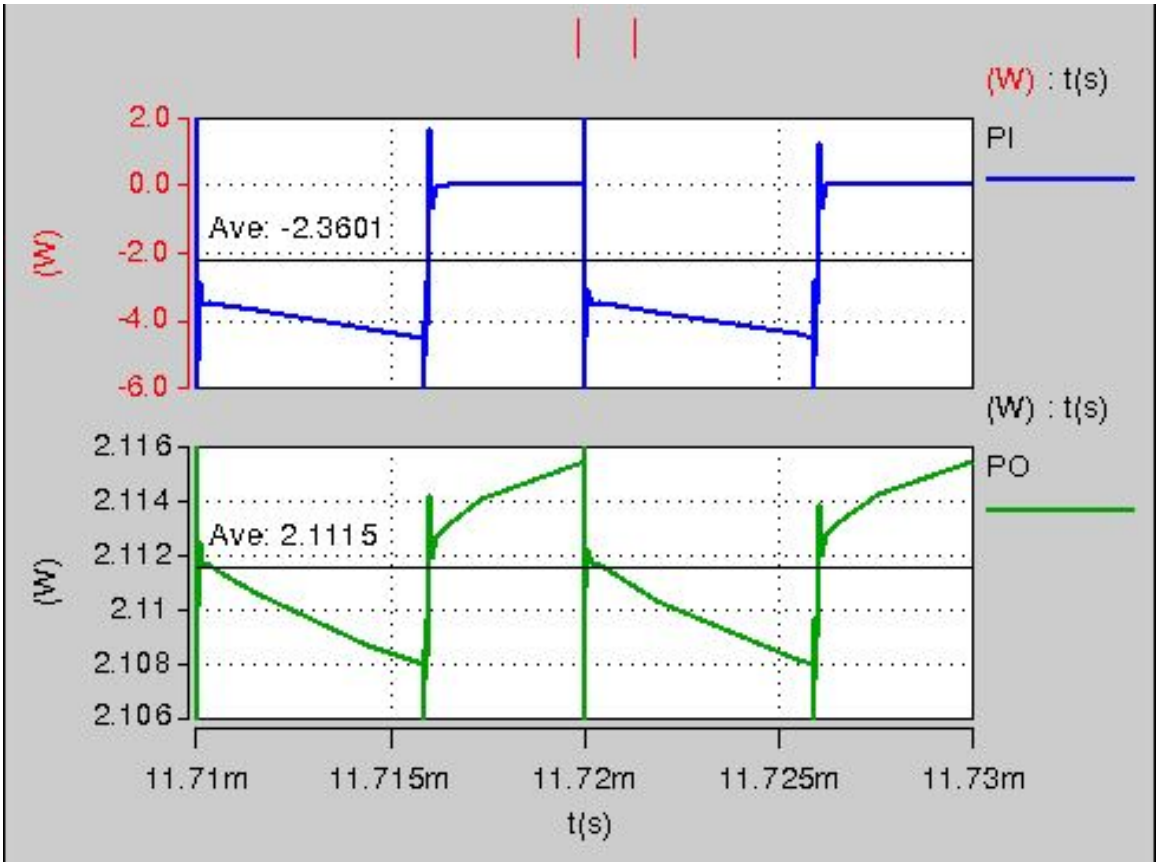

Figure 2.11: Simulated waveforms of input and output powers.

2.7 Experimental Validation of the Analysis of the Power Stage Running in CCM in Time-Domain.

For the validation of the theoretical findings in previous section a tapped inductor buck dc-dc converter was design and implemented for an input voltage of $V_I = 12$ V, switching frequency of $f_s = 100$ kHz, output power of $P_O = 2.5$ W and output voltage $V_O = 5$ V. The measured parasitic resistances across the capacitor, MOSFET drain-to-source and the tapped-inductor are $r_C = 0.5\ \Omega$, $r_L = 0.5\ \Omega$, $r_{DS} = 55$ mΩ. The tapped-inductor is designed for a turns ratio of $n = 2$. Knowing the gain required from the converter the required duty cycle can be obtained by using (2.25). The minimum capacitance required to make sure that the ripples are well with in the 1% of the output voltage can be obtained from (2.38). The selected capacitor has a capacitance of $C = 150\ \mu$F. The Inductance required from the tapped-inductor for the converter to run in continuous-conduction mode can be obtained from (2.31). To obtain this required inductance from the tapped-inductor 0_42515IC has been selected. The type of coil used is AWG20, with a total of 36 turns in the primary and the secondary. The test set up can be seen in Fig. 2.12. The dc output voltage can be measured by using a multimeter and is measured to be equal to $V_O = 4.5$ V. at $D = 0.59$. A dc current probe can be used to measure dc values of output current, input current and diode current and are measured to be $I_I = 0.21$ A, $I_O = 0.45$ A and $I_D = 0.24$ A. From (2.17), the voltage across the switch is given by

$$v_{S1} = V_I + (n-1)V_O = 16.5 \text{ V}. \tag{2.80}$$

As seen in Fig. 2.13, the experimental results are in good agreement with theoretical results. From (2.14), the voltage across the diode is given by

$$v_D = -\frac{V_I + (n-1)V_O}{n} = 8.25 \text{ V}. \tag{2.81}$$

As seen in Fig. 2.14, the experimental results are in good agreement with theoretical results. When the switch is on, the voltage across the magnetizing inductance as seen

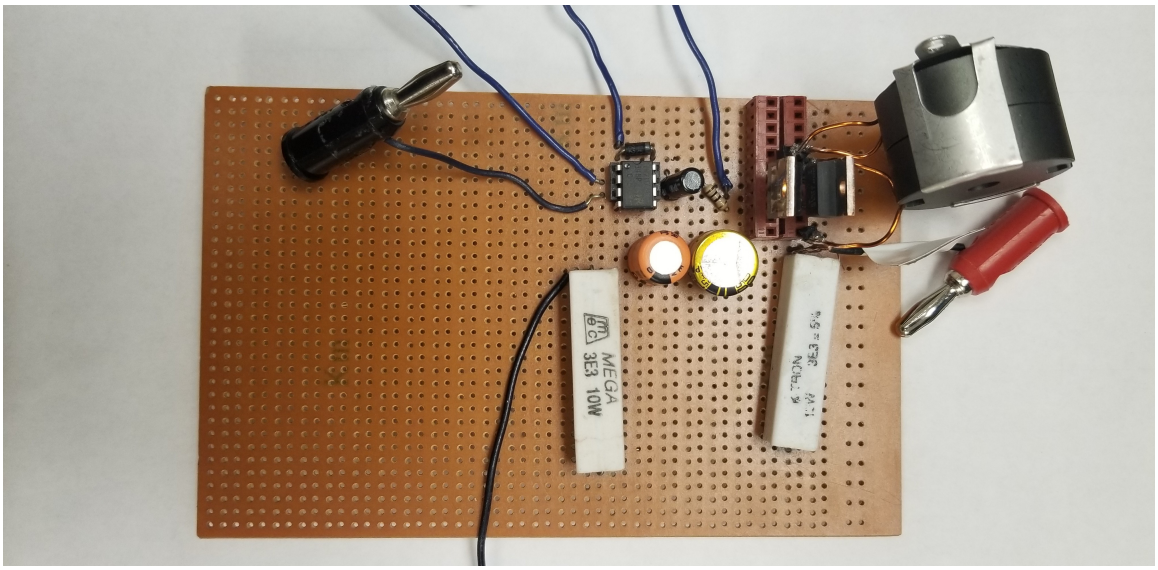

Figure 2.12: Tapped-inductor buck dc-dc converter on zero board to test its steady-state characteristics.

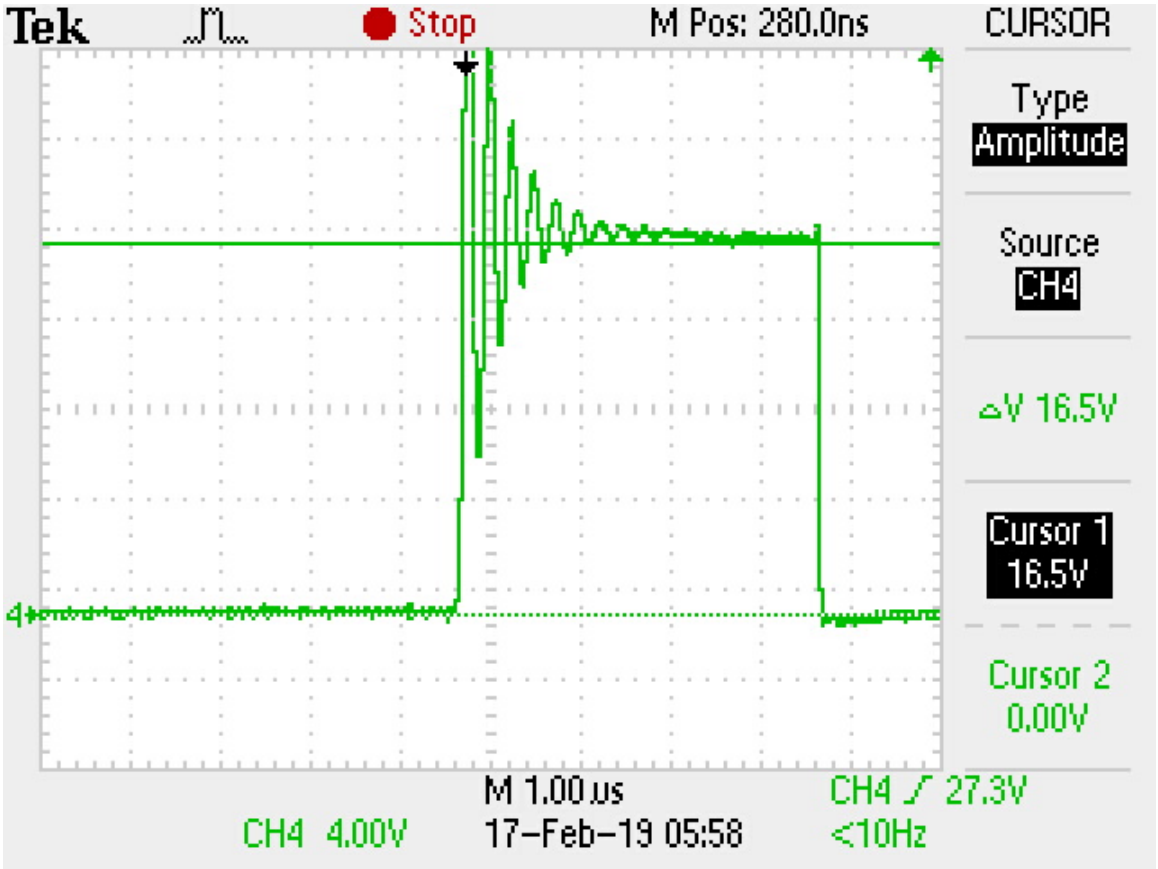

Figure 2.13: Steady-state plots of switch voltage v_{S1} .

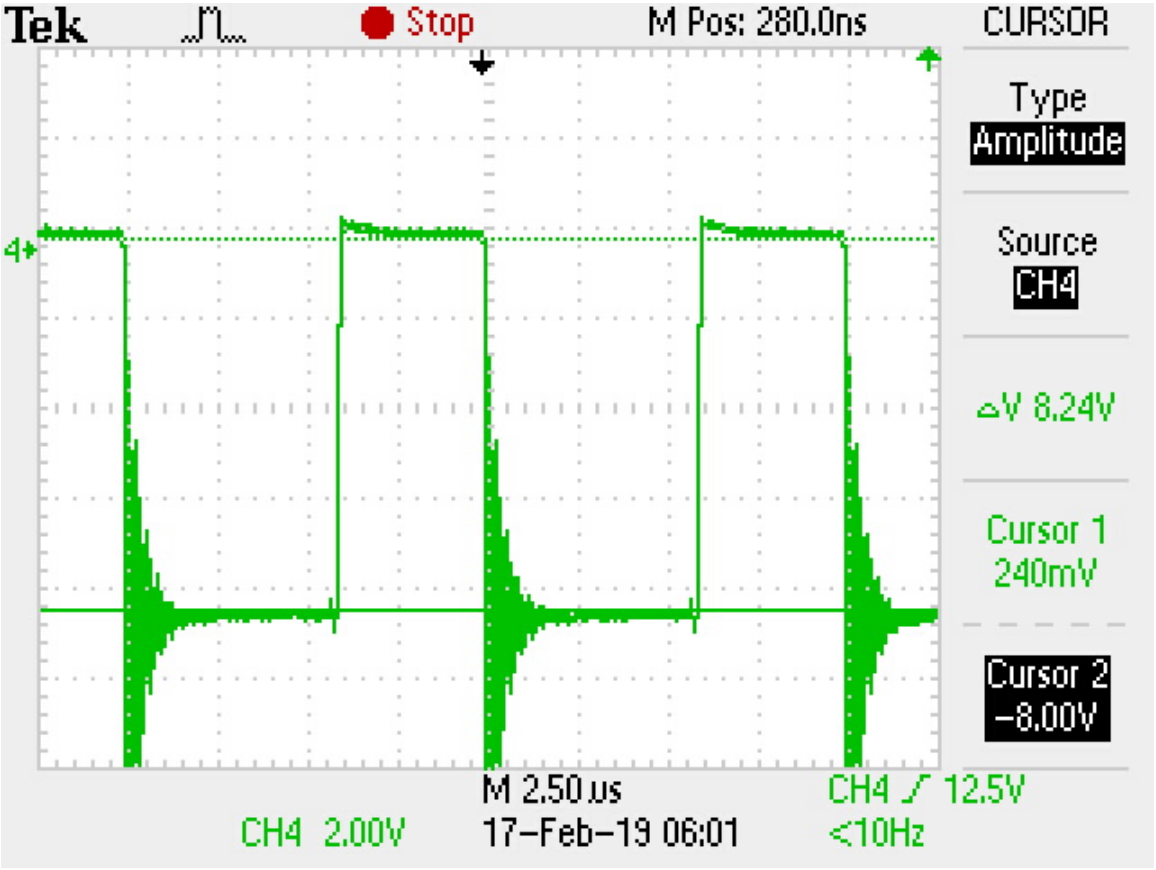

Figure 2.14: Steady-state plots of diode voltage v_D .

in (2.5) is

$$v_L = \frac{V_I - V_O}{n} = 3.75 \text{ V}. \tag{2.82}$$

When the switch is off the voltage across the magnetizing inductance as seen in (2.16) is

$$v_S = -V_O = -4.5 \text{ V}. \tag{2.83}$$

As seen in Fig. 2.15, the experimental results are in good agreement with theoretical results. From (2.11), the slope of the switch current is given by

$$i_{S1slope} = \frac{V_I - V_O}{n^2 L} = 16 \times 10^3. \tag{2.84}$$

As seen in Fig. 2.16, change in current over 1 μs is 16 mA. Therefore, the slope is 16×10^3, which is in good agreement with the theoretical calculations. From (2.21),

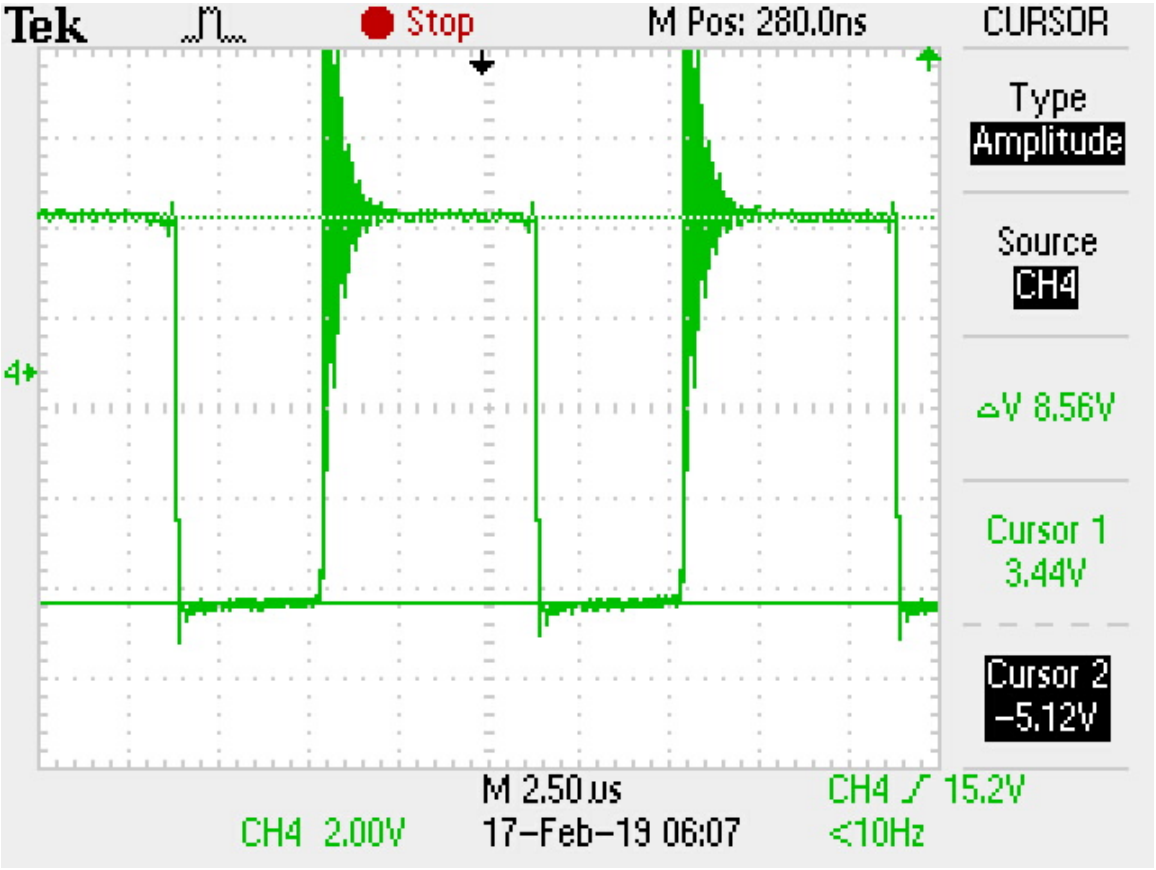

Figure 2.15: Steady-state plots of voltage across magnetizing inductor v_L .

the slope of the switch current is given by

$$i_{Dslope} = -\frac{V_O}{L} = 40 \times 10^3. \tag{2.85}$$

As seen in Fig. 2.17, change in current over 1 μs is 50 mA. Therefore, the slope is 50×10^3, which is in good agreement with the theoretical calculations.

$$P_{rDS} = \frac{r_{DS} D}{R_L} P_O = 22 \text{ mW}. \tag{2.86}$$

The switching loss is expressed as

$$P_{sw} = \frac{f_s C_o R_L}{M_{VDC}} P_O = 4.4 \text{ mW}, \tag{2.87}$$

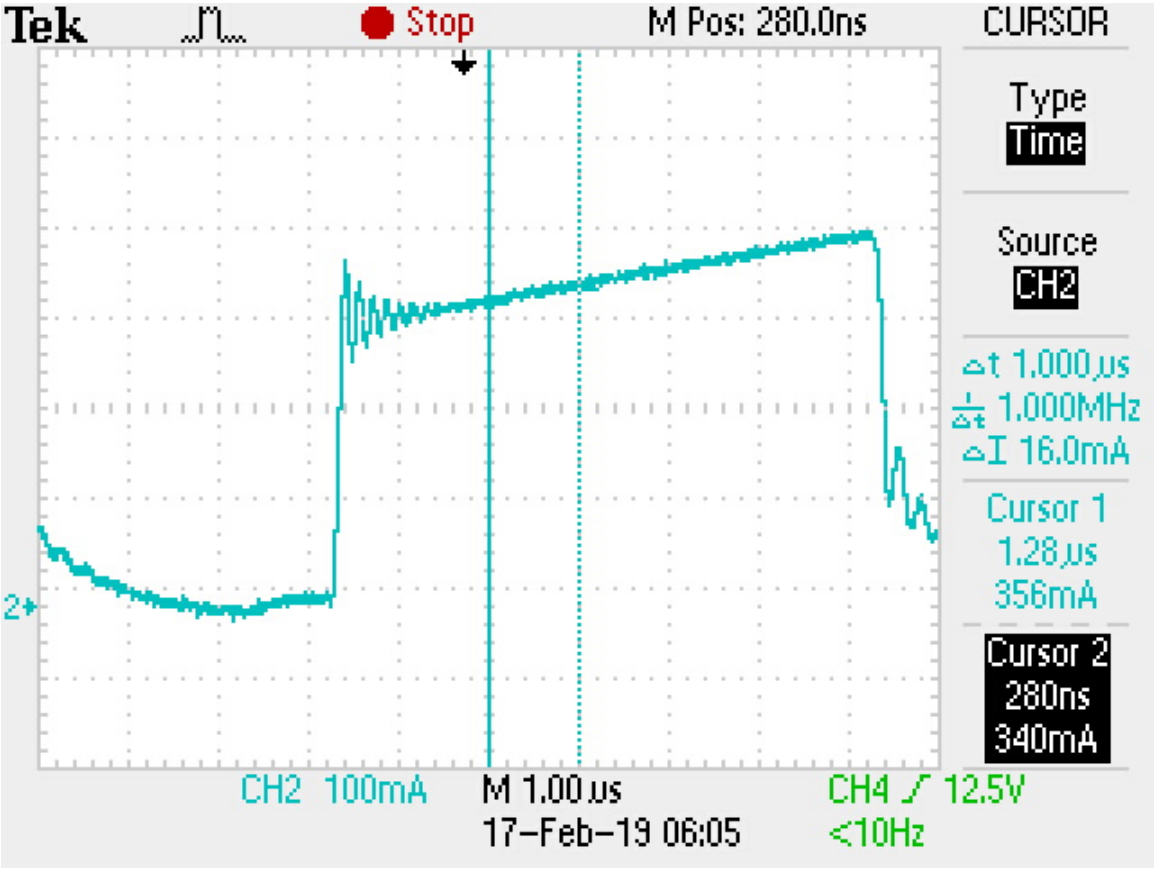

Figure 2.16: Steady-state plots of switch current i_{S1}.

where $C_o = 180$ pF is the transistor output capacitance.

The total power loss in the diode is

$$P_D = (1 - D)\left(\frac{V_F}{V_O} + \frac{R_F}{R_L}\right) P_O = 0.720 \text{ W}. \tag{2.88}$$

The power loss in r_L is

$$P_{rL} = \frac{r_L\left(\left(\dfrac{n^2}{D + (1 - D)n} - 1\right) D + 1\right)}{R_L} \frac{P_O}{R_L} = 0.20 \text{ W}. \tag{2.89}$$

The power loss in the filter capacitor is

$$P_{rC} = \frac{r_C R_L (1 - D)^2}{12 L^2 f_o^2} P_O = 0.77 \text{ mW}. \tag{2.90}$$

The total power loss is

$$P_{LS} = P_{r_{DS}} + P_{sw} + P_D + P_{rL} + P_{rC} = 947.17 \text{ mW}. \tag{2.91}$$

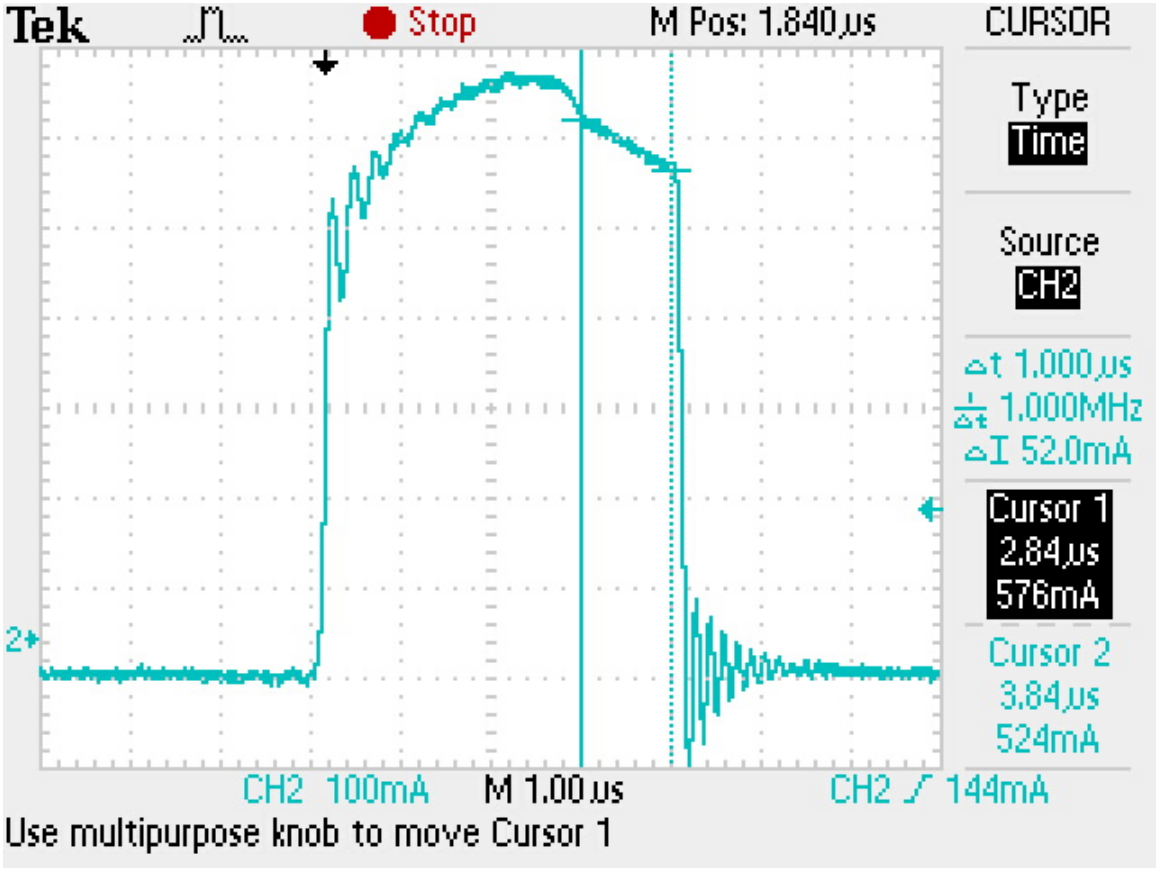

Figure 2.17: Steady-state plot of diode current i_D.

Therefore, the overall efficiency of the converter is

$$\eta = 100 \times \frac{P_O}{P_O + P_{LS}} = 84\%. \tag{2.92}$$

From the measured values of input and output voltages and current the measured efficiency of the converter is 80 % The plot representing the variation of lossy voltage gain $M_{VDClossy}$ for the change in duty cycle can be seen in Fig. 2.18. The practical, simulation and the theoretical results are in good agreement with each other. It can also be noted that even thought the simulation and experimental results are in good agreement with each other the experimental results have high ringing due to the non-ideal inductance of the tapped-inductor. This could be compensated by using a snubber circuit for a more practical implementations.

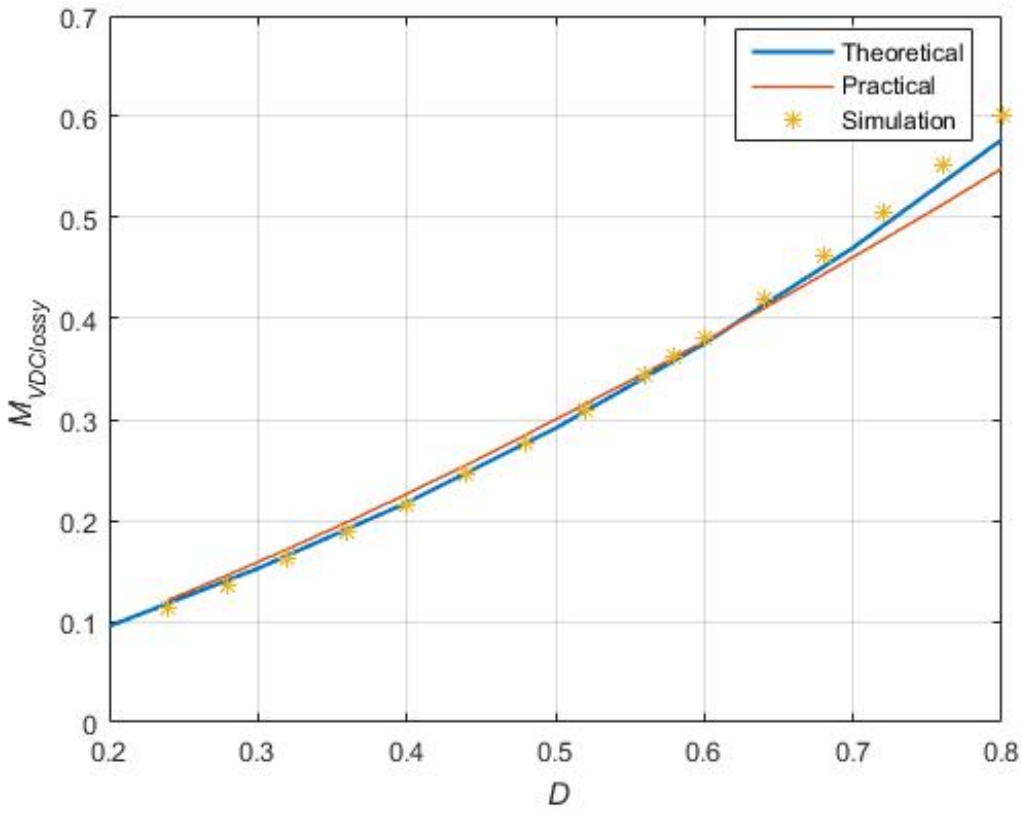

Figure 2.18: Plot representing lossy voltage gain as obtained from theoretical equations, practical implementation and circuit simulation.

3 Steady-State Analysis of the Power Stage in DCM

For applications which do not require a continuous flow of the inductor current or for low loads, discontinuous-conduction mode can be a good option for power conversion. In this scenario the required inductance to maintain the required output power can be low. This helps build small compact components with lower losses. This chapter is sorted with following the objectives in mind

1. To perform steady-state analysis of the converter in DCM and produce its current and voltage waveforms

2. To derive the design equations for the converter components.

3. To determine the expression for the total power loss and hence the overall efficiency of the converter.

4. To validate the converter operation and derived equations through SABER circuit simulation.

5. To validate the converter operation and derived equations through hardware implementation.

3.1 Principle of Operation

The circuit representing a tapped-inductor buck dc-dc converter working in DCM can be seen in Fig. 3.1. An input voltage V_I provides a input current I_I. The converter produces an output voltage V_O across the load resistance R_L, with load current I_O flowing through it. The tapped-inductor used for storing energy has a secondary side inductance of L. The turns on the primary and secondary sides are N_1 and N_2 respectively. The voltages across the primary and secondary are v_p and v_s respectively. The currents flowing through the primary and secondary side of the

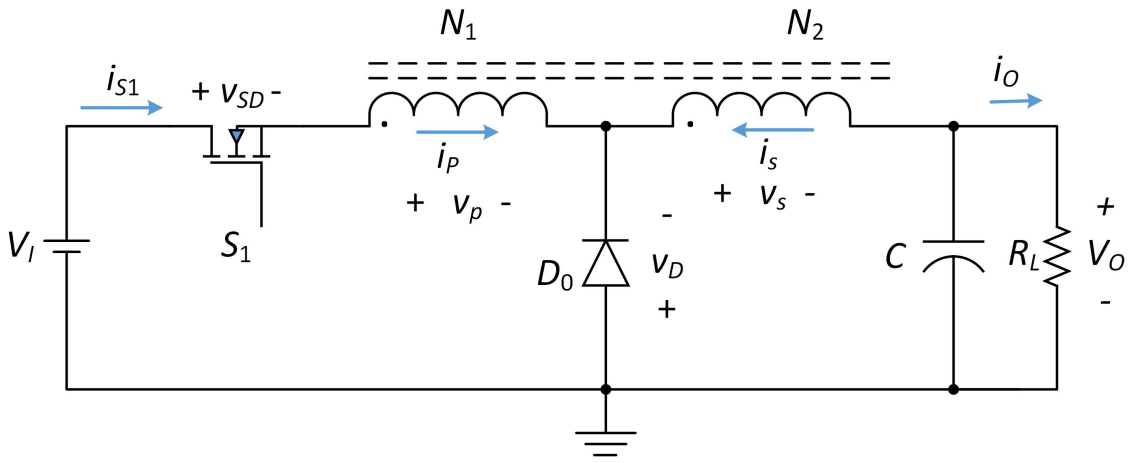

Figure 3.1: Circuit of a tapped-inductor buck PWM dc-dc converter.

tapped-inductor are i_p and i_s respectively. The relationship between the voltages, currents and the turns ratio is given by

$$\frac{v_p}{v_s} = \frac{i_s}{i_p} = n - 1. \tag{3.1}$$

The converter also has semi-conductive switches like MOSFET S_1 and diode D_0. These semi-conductive switches along with the tapped-inductor help in the power conversion. To understand and analyze the working of the converter in DCM, the converter operation is broken down into three different time intervals. These time intervals are divided based on the operating states of the two MOSFET and diode switches. The following section help breakdown the operation of the convertor in different time intervals

3.1.1 Time Interval: $0 < t \leq DT$

During this time interval the gate-to-source voltage to the MOSFET switch S_1 is high. Therefore, the switch is in ON-state. As the MOSFET is shorted the voltage across it is zero. This also leaves the cathode of the diode with high voltage, while the anode is grounded. This causes the diode to reverse bias. The diode switch is

now in OFF-state. The circuit representing the convertor during this time interval can be seen in Fig. 3.2. Applying the Kirchhoff's voltage low the voltage across the inductor L is given by

$$v_L = v_s = V_I - V_O - v_p = \frac{V_I - V_O}{n}. \tag{3.2}$$

The current flowing through the magnetizing inductance L is

$$i_L(t) = \frac{1}{L}\int_0^t v_L dt = \frac{V_I - V_O}{nL}t,\ i_L(0) = 0. \tag{3.3}$$

The peak-to-peak value of the inductance current is

$$\Delta i_L = i_L(DT) - i_L(0) = \frac{V_I - V_O}{nL}DT. \tag{3.4}$$

Since the switch is in ON-state during this time interval, the voltage across the MOSFET v_{S1} is zero. The instantaneous value of switch current is

$$i_{S1}(t) = \frac{i_L(t)}{n} = \frac{V_I - V_O}{n^2 L}t,\ i_{S1}(0) = 0, \tag{3.5}$$

and the peak-to-peak value of the current through the switch is

$$\Delta i_{S1} = i_{S1}(DT) - i_{S1}(0) = \frac{V_I - V_O}{n^2 L}DT. \tag{3.6}$$

Applying Kirchhoff's voltage law, the voltage across the diode D_0 is

$$v_D = -(v_s + V_O) = \frac{V_I + (n-1)V_O}{n}. \tag{3.7}$$

Since the diode switch is open, no current flows through it. Therefore, $i_D = 0$.

3.1.2 Time Interval: $DT < t \leq (D + D_1)T$

During this time interval the gate-to-source voltage of the MOSFET switch S_1 is low. Therefore, the switch is in OFF-state. As the MOSFET is open no current will be flowing through it therefore, the current $i_{S1} = 0$. The diode is for forward biased and this causes the cathode to ground. Now the diode is shorting and the voltage

across the diode is zero. The circuit representing the converter in this time interval can be seen in Fig. 3.3. Applying the Kitchhoff's voltage law across the inductor.

$$v_L = -V_O. \tag{3.8}$$

Since, the MOSFET is open, no current flows through the primary and the secondary turns of the tapped-inductor buck. The current flowing through the magnetizing inductor is equal to the current flowing through the diode and is given by

$$i_D(t) = i_L(t) = \frac{1}{L}\int_{DT}^{t} v_L dt = -\frac{V_O}{L}(t - DT) + i_L(DT). \tag{3.9}$$

The peak value of inductance current for the converter in DCM can be measured at time $t=DT$ and is equal to the initial or peak value of diode current. Substituting (3.4) into (3.9).

$$i_D(t) = i_L(t) = -\frac{V_O}{L}(t - DT) + \frac{V_I - V_O}{nL}DT. \tag{3.10}$$

The peak-to-peak value of diode current is

$$\Delta i_D = \Delta i_L = \frac{V_O}{L}D_1 T. \tag{3.11}$$

Since the diode is in ON-state and the MOSFET is in OFF-state, the voltage v_D across the diode is zero and the current flowing through the MOSFET i_{S1} is zero. Applying Kirchhoff's voltage law, the voltage across S_1 is

$$v_{S1} = V_I - (v_P + v_S + V_O) = V_I + (n-1)V_O. \tag{3.12}$$

3.1.3 Time Interval: $(D + D_1)T < t \leq T$

During this time interval the gate-to-source voltage across the MOSFET continues to stay low. The current in the inductor drains completely to the output side of the

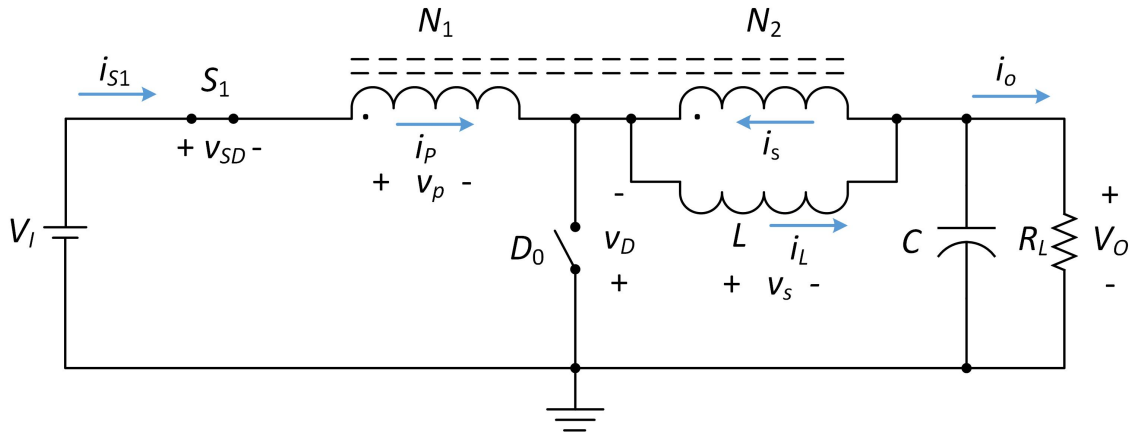

Figure 3.2: Sub-circuit of the tapped-inductor buck converter for the interval $0 < t \leq DT$.

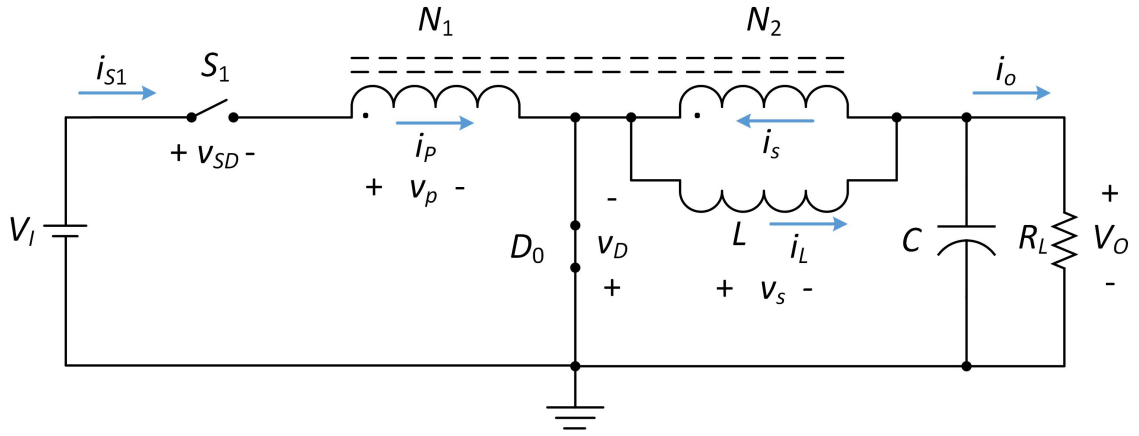

Figure 3.3: Sub-circuit of the tapped-inductor buck converter for the interval $DT < t \leq (D + D_1)T$.

converter and no current flows through the inductor nor the diode. This discontinuity in the inductor current lead to the discontinuous conduction mode of the converter. Both the MOSFET and diode switches are open and no current flows through them. Kirchhoff's voltage law can be used to calculate the voltage across the switch.

$$v_{S1} = V_I - V_O. \tag{3.13}$$

The voltage cross the diode v_D is

$$v_D = -V_O. \tag{3.14}$$

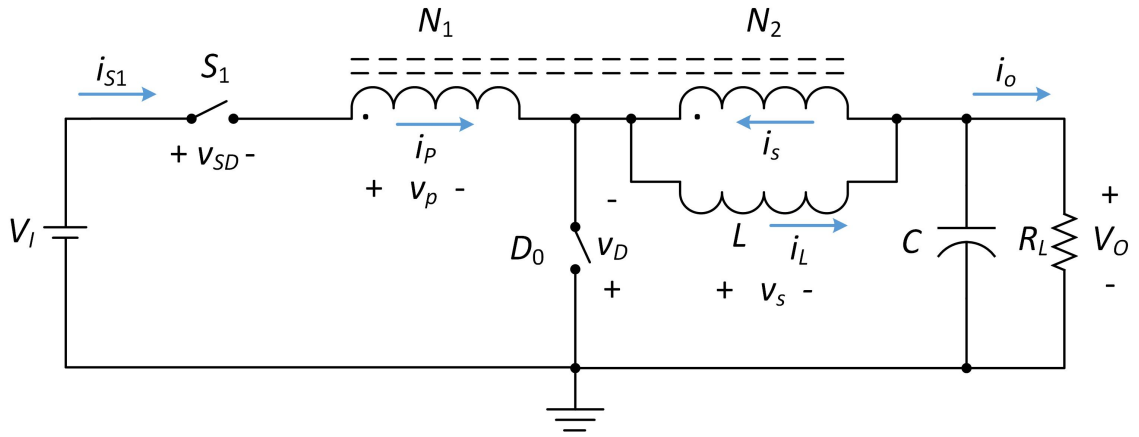

Figure 3.4: Sub-circuit of the tapped-inductor buck converter for the interval $(D + D_1)T < t \leq T$.

Using the derived equations, the voltage and current waveforms of the tapped-inductor buck dc-dc converter can be predicted as seen in Fig. 3.5.

3.2 DC Voltage and Current Ratios

The average steady-state voltage across an inductor is zero, as stated by the principle of volt-second balance.

$$\int_0^{DT} v_L dt = \int_{DT}^{(D+D_1)T} v_L dt. \tag{3.15}$$

From (3.2) and (3.8), we get

$$\frac{V_I - V_O}{n} D = V_O D_1. \tag{3.16}$$

Therefore, the dc input-to-output voltage transfer function of the tapped-inductor buck converter in DCM is

$$M_{VDC} = \frac{V_O}{V_I} = \frac{D}{D + nD_1}. \tag{3.17}$$

For an ideal converter, the input power is equal to the output power

$$V_O I_O = V_I I_I. \tag{3.18}$$

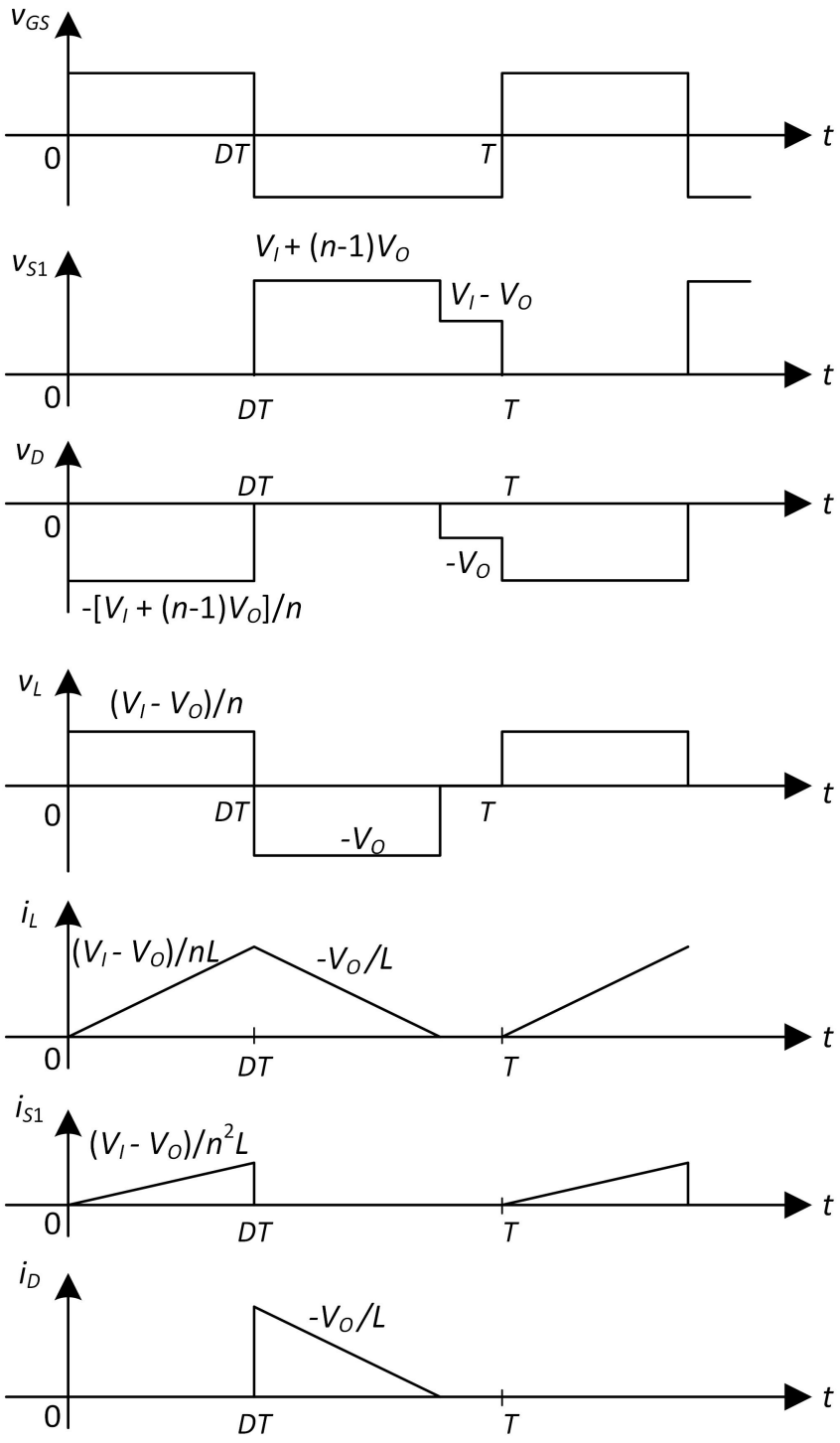

Figure 3.5: Key current and voltage waveforms of the tapped-inductor buck converter.

Therefore, the dc input-to-output current transfer function for a tapped-inductor buck in DCM is

$$M_{IDC} = \frac{I_O}{I_I} = \frac{D + nD_1}{D}. \tag{3.19}$$

Applying Kirchhoff's current law, at the output node of the tapped-inductor current

$$I_O = \frac{1}{T}\int_0^T i_L dt - I_S = \frac{(D + D_1)\Delta i_L}{2} - I_I(n-1). \tag{3.20}$$

Substituting (3.4), (3.17), and (3.19) into (3.20), I_O is obtained as

$$I_O = \frac{V_O D^2(1 - M_{VDC})}{2n^2 L f_s M_{VDC}^2}. \tag{3.21}$$

This can be rearranged to form

$$D = \sqrt{\frac{2n^2 L f_s M_{VDC}^2 I_O}{(1 - M_{VDC})V_O}}. \tag{3.22}$$

At the boundary between CCM and DCM[13].

$$M_{VDCB} = \frac{D_B}{D_B + n(1 - D_B)}. \tag{3.23}$$

Substituting (3.23) into (3.22), the duty cycle at boundary condition is a quadratic equation given by

$$(n-1)D_B^2 - (2n-1)D_B + n\left(1 - \frac{2f_s L}{R_L}\right) = 0. \tag{3.24}$$

The duty cycle at boundary condition is

$$D_B = \frac{2n - 1 - \sqrt{(2n-1)^2 + 4n(n-1)\left(\frac{2f_s L}{R_L} - 1\right)}}{2(n-1)}. \tag{3.25}$$

A plot on the effect of the normalized load on the duty cycle to maintain the required voltage gain can be seen in Fig. 3.6. As can be noted unlike in the continuous conduction mode, the output is no longer independent of the load in discontinuous conduction mode. The increase in load requires a increase in duty cycle to maintain the required voltage gain.

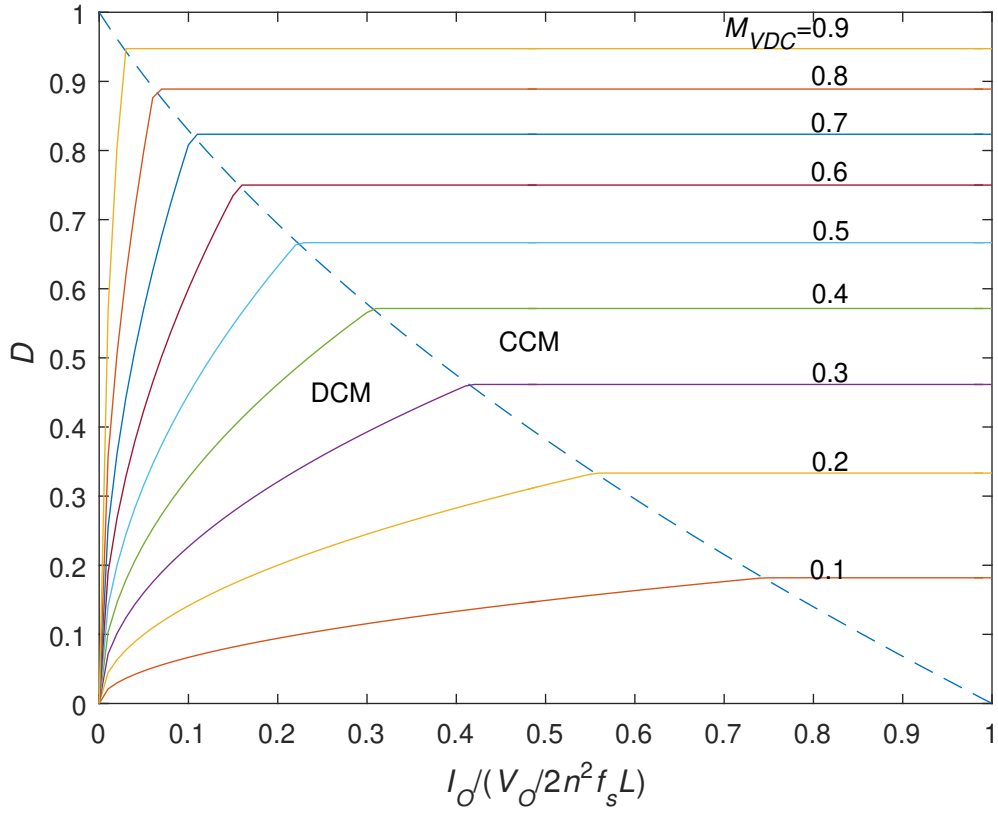

Figure 3.6: Duty cycle as a function of normalized load $I_O/(V_O/2n^2 f_s L)$ at different valuers of M_{VDC}.

3.3 Power Losses and Efficiency

To calculate the overall power lost in the converter, the parasitic losses across the components are represented as seen in Fig. 3.7. The parasitic on-resistance of the MOSFET is r_{DS}. The parasitic resistive loss in the tapped-inductor is r_L. The ESR of the filter capacitor is represented as r_C. The parasitic resistance of the diode D_0 is R_F and the forward diode voltage is V_F. The power lost across each and every component can be calculated by first calculating the rms value of the current flowing through these parasitic. The power is then calculated as the product of squared current flowing through the parasitic and the resistance offered by each of them. The

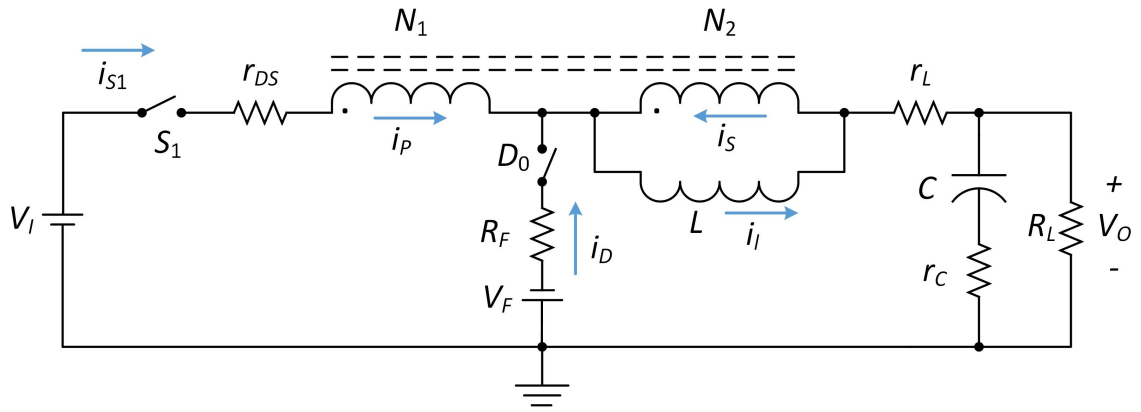

Figure 3.7: Circuit of tapped-inductor buck converter including the parasitic components.

rms value of switch current is

$$\begin{aligned} I_{S1rms} &= \sqrt{\frac{1}{T}\int_0^T i_{S1}^2 dt} \\ &= \frac{V_O DT}{n^2 L}\left(\frac{1}{M_{VDC}-1}\right)\sqrt{\frac{D}{3}}. \end{aligned} \tag{3.26}$$

Substituting (3.6) into (3.26), we obtain

$$I_{S1rms} = I_O\sqrt{\frac{2R_L M_{VDC}}{3n}\sqrt{\frac{2\left(1-M_{VDC}\right)}{Lf_s R_L}}}. \tag{3.27}$$

The conduction loss in the switch is

$$P_{rDS} = r_{DS} I_{S1rms}^2 = \frac{2r_{DS} M_{VDC}}{3n}\sqrt{\frac{2\left(1-M_{VDC}\right)}{Lf_s R_L}} P_O. \tag{3.28}$$

The switching loss is expressed as

$$P_{sw} = \frac{f_s C_o V_o^2}{M_{VDC}^2} = \frac{f_s C_o R_L}{M_{VDC}} P_O, \tag{3.29}$$

where C_o is the transistor output capacitance. Therefore, the total switch power loss is

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2}. \tag{3.30}$$

Substituting (3.27) and (3.29) into (3.30) results in

$$P_{FET} = \left[\frac{2R_L M_{VDC}}{3n}\sqrt{\frac{2\left(1-M_{VDC}\right)}{Lf_s R_L}} + \frac{f_O C_O R_L}{2M_{VDC}^2}\right] P_O. \tag{3.31}$$

Using (3.10), the rms value of diode current is

$$I_{Drms} = \sqrt{\frac{1}{T}\int_{D}^{(D_1+D)T} i_D^2 dt} = \frac{V_O D_1}{L f_s}\sqrt{\frac{D_1}{3}}. \tag{3.32}$$

Substituting (3.19) and (3.21) into (3.32)

$$I_{Drms} = V_O \sqrt{\frac{1}{3R_L}\sqrt{\frac{8(1-M_{VDC})^3}{L f_s R_L}}}. \tag{3.33}$$

The power loss across R_F is

$$P_{RF} = R_F I_{Drms}^2 = \frac{R_F}{3}\sqrt{\frac{8(1-M_{VDC})^3}{L f_s R_L}} P_O. \tag{3.34}$$

The average diode current is

$$I_D = \frac{1}{T}\int_{DT}^{(D+D_1)T} i_D dt = \frac{V_O D^2}{2n^2 f_s L}\left(\frac{1}{M_V DC} - 1\right)^2. \tag{3.35}$$

Substituting (3.21) into (3.35), we get

$$I_D = I_O(1 - M_{VDC}). \tag{3.36}$$

The power loss associated with the diode forward voltage V_F is

$$P_{VF} = V_F I_D = \frac{V_F}{V_O}(1 - M_{VDC}) P_O. \tag{3.37}$$

The total power loss in the diode is

$$\begin{aligned} P_D = P_{RF} + P_{VF} = \Bigg[& \frac{R_F}{3}\sqrt{\frac{8(1-M_{VDC})^3}{L f_s R_L}} \\ & + \frac{V_F}{V_O}(1 - M_{VDC}) \Bigg] P_O. \end{aligned} \tag{3.38}$$

The rms value of current flowing through the inductor parasitic is

$$\begin{aligned} I_{L1rms} &= \sqrt{\frac{1}{T}\left(\int_0^{DT} i_{S1}^2 dt + \int_{DT}^{(D+D_1)T} i_L^2 dt\right)} \\ &= \Delta i_L \sqrt{\frac{nD + D_1}{3}}. \end{aligned} \tag{3.39}$$

Substituting (3.19) and (3.21) into (3.39), we obtain

$$I_{L1rms} = V_O \sqrt{\frac{(n^2-1)M_{VDC}+1}{R_L}} \sqrt{\frac{8(1-M_{VDC})}{9f_sLR_L}}. \tag{3.40}$$

The power loss in r_L is

$$\begin{aligned} P_{rL} &= r_L I_{Lrms}^2 \\ &= r_L \left[(n^2-1)M_{VDC}+1\right] \sqrt{\frac{8(1-M_{VDC})}{9f_sLR_L}} P_O. \end{aligned} \tag{3.41}$$

The total power loss is

$$P_{LS} = P_{r_{DS}} + P_{sw} + P_D + P_{rL}. \tag{3.42}$$

Therefore, the overall efficiency of the converter is

$$\eta = \frac{P_O}{P_I} = \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \dfrac{P_{LS}}{P_O}}. \tag{3.43}$$

The average value of input current is

$$I_I = \frac{1}{T}\int_0^{DT} i_{S1} dt = \frac{D^2(V_I - V_O)}{2n^2 f_s L} = \frac{D^2 V_O}{2n^2 f_s L}\left(\frac{1}{M_{VDC}} - 1\right). \tag{3.44}$$

The required power from the input is

$$P_I = V_I I_I = \frac{D^2 V_O I_I}{2n^2 f_s L}\left(\frac{1}{M_{VDC}} - 1\right). \tag{3.45}$$

The reflected power at the output is

$$P_O = \frac{V_O^2}{R_L}. \tag{3.46}$$

The efficiency can now be defined as

$$\eta = \frac{P_O}{P_I} = \frac{2n^2 f_s L M_{VDC}^2}{D^2 R_L (1 - M_{VDC})}. \tag{3.47}$$

For a lossy converter, the required duty cycle is

$$D = \sqrt{\frac{2n^2 L f_s M_{VDC}^2 I_O}{\eta(1 - M_{VDC})V_O}}. \tag{3.48}$$

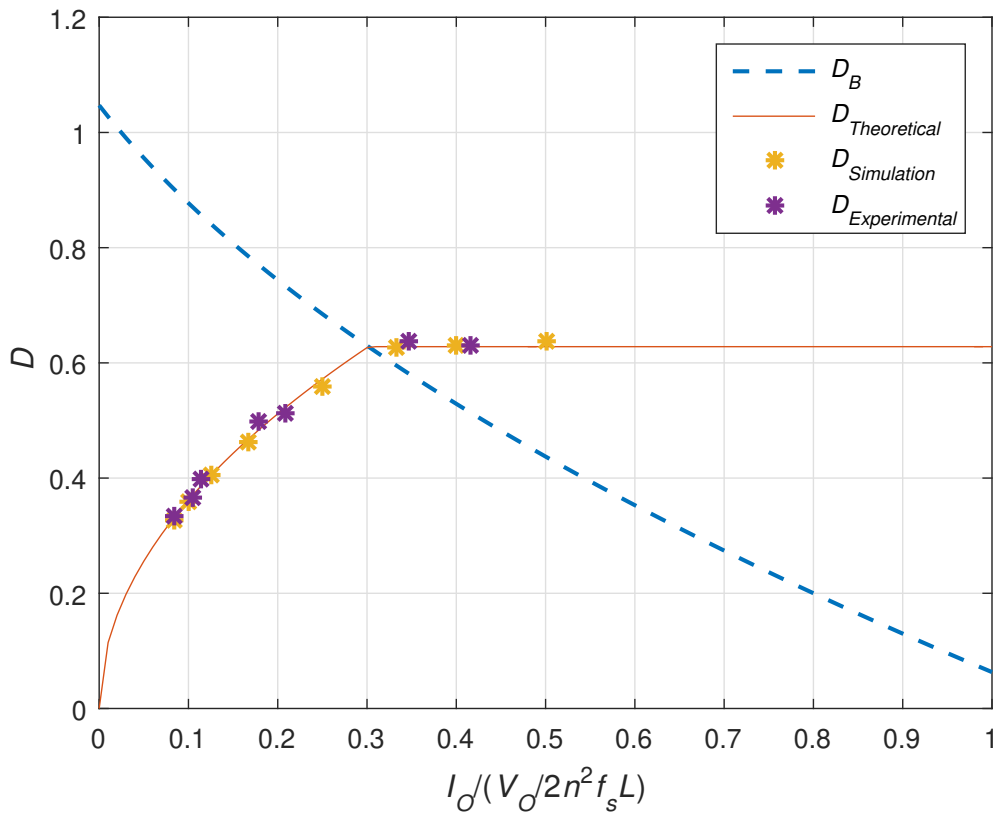

Figure 3.8: Duty cycle as a function of normalized load $I_O/(V_O/2n^2f_sL)$ for a lossy converter.

For a lossy converter, the duty cycle at boundary condition is

$$D_B = \frac{2n+\eta-2-\sqrt{\eta^2+[n^2+n\,(\eta-2)-\eta+1]\,\dfrac{8Lf_s\eta}{R_L}}}{2\left(n+\eta-2-\dfrac{\eta}{n}+\dfrac{1}{n}\right)}. \tag{3.49}$$

A plot representing the effect of the normalized load on the duty cycle for a lossy converter is shown in Fig. 3.8.

3.4 Simulation Validation of the Analysis of the Power Stage Running in DCM in Time-Domain.

To validate the obtained theoretical results a SABER circuit simulator was used. A tapped-inductor buck for the following specification was considered: An input voltage of $V_I = 12$ V, converter switching frequency $f_s = 100$ kHz, output power $P_O = 2.5$ W and output voltage of $V_O = 5$ V. The tapped-inductor turns ratio is $n = 2$. The parasitic of the components are $r_L = 0.5\ \Omega$, $r_{DS} = 55\ \text{m}\Omega$, $R_F = 25\ \text{m}\Omega$, and $V_F = 0.7$ V.

The load resistance is

$$R_L = \frac{V_O^2}{P_O} = 10\ \Omega. \tag{3.50}$$

The required voltage gain from the specification is

$$M_{VDC} = \frac{V_O}{V_I} = 0.42. \tag{3.51}$$

The maximum duty cycle required at the boundary between CCM and DCM for this gain can be calculated from (2.25)

$$D_B = \frac{nM_{VDCB}}{1 + (n-1)M_{VDCB}} = 0.59. \tag{3.52}$$

The maximum inductance required for the converter to run in DCM can be calculated from (2.31)

$$L_{max} = \frac{R_L(1-D)D}{2nf_sM_{VDC}} = 14.38\ \mu\text{H}. \tag{3.53}$$

Let $L = 5\ \mu\text{H}/55\ \text{m}\Omega$

The duty cycle required for the required normalized load and for an efficiency $\zeta = 0.9$ is

$$D = \sqrt{\frac{2n^2Lf_sM_{VDC}^2I_O}{\eta(1-M_{VDC})V_O}} = 0.37. \tag{3.54}$$

The maximum inductor ripple current is

$$\Delta i_{Omax} = \frac{(V_I - V_O)D}{n^2Lf_s} = 1.3\ A. \tag{3.55}$$

The ripple voltage is assumed to be 1% of V_O

$$V_r = \frac{V_O}{100} = 50 \text{ mV}. \tag{3.56}$$

The maximum ESR of the filter capacitor is given by

$$r_{Cmax} = \frac{V_r}{\Delta i_{Omax}} = 0.04 \ \Omega. \tag{3.57}$$

The minimum filter capacitor is given by

$$C_{min} = \frac{D}{2 f_s r_C} = 46.25 \ \mu\text{F} \tag{3.58}$$

Let $C = 47 \ \mu\text{F}/r_C = 30 \ \text{m}\Omega$. The selected MOSFET and diode were IRF540 and MBR10100 by vishay semiconductors.

The conduction loss in the switch is

$$P_{rDS} = \frac{2 r_{DS} M_{VDC}}{3n} \sqrt{\frac{2\left(1 - M_{VDC}\right)}{L f_s R_L}} P_O = 9.27 \text{ mW}. \tag{3.59}$$

The switching loss is expressed as

$$P_{sw} = \frac{f_s C_o R_L}{M_{VDC}} P_O = 0.59 \text{ mW}, \tag{3.60}$$

where $C_o = 100$ pF is the transistor output capacitance.

The total power loss in the diode is

$$P_D = \left[\frac{R_F}{3} \sqrt{\frac{8(1 - M_{VDC})^3}{L f_s R_L}} + \frac{V_F}{V_O} (1 - M_{VDC}) \right] P_O = 0.215 \text{ W}. \tag{3.61}$$

The power loss in r_L is

$$P_{rL} = r_L \left[(n^2 - 1) M_{VDC} + 1 \right] \sqrt{\frac{8(1 - M_{VDC})}{9 f_s L R_L}} P_O = 1.726 \text{ mW}. \tag{3.62}$$

The total power loss is

$$P_{LS} = P_{r_{DS}} + P_{sw} + P_D + P_{rL} = 0.23 \text{ W}. \tag{3.63}$$

Therefore, the overall efficiency of the converter is

$$\eta = 100 \times \frac{P_O}{P_O + P_{LS}} = 91\%. \tag{3.64}$$

The voltage gain of the non-ideal converter

$$M_{VDClossy} = \eta M_{VDC} = 0.38. \tag{3.65}$$

Thus, the output voltage under loss operation is $V_O = 4.56$ V. The new duty cycle to achieve $V_O = 5$ V is $D = 0.62$. The obtained simulated drain-to-source voltage, diode voltage and voltage across inductor waveforms can be seen in Fig. 3.9. The measured value of the voltages across the MOSFET drain-to-source, diode and the magnetizing inductor during the first time interval are zero, $v_D = -8.49$ V and $v_L = 3.42$ V respectively. The calculated values from equation (3.7) and (3.2) are zero $v_D = -8.5$ V and $v_L = 3.5$ V. During the second time interval the voltages are $v_{S1} = 16.89$ V, zero and $v_L = -5.35$ V respectively. The calculated values as obtained from equations (3.12) and (3.8) are $v_{S1} = 17$ V, zero and $v_L = -5$ V respectively. During the third time interval the measured values of voltages are $v_{S1} = 6.87$ V, $v_D = -5.07$ V and zero respectively. The calculated values as obtained from equations (3.13) and (3.14) are $v_{S1} = 7$ V, $v_D = -5$ V and zero respectively. The inductor current, MOSFET and diode switch currents can be seen in Fig. 3.10. During the first time interval the measured slope of the current flowing through the MOSFET, diode and the inductance are 0.345 A/μs, zero and 0.679 A/μs respectively. The calculated values as obtained from equations (3.6) and (3.4) are 0.345 A/μs, zero and 0.679 A/μs respectively. During the second time interval the current slopes are zero, 1.063 A/μs, 1.097 A/μs respectively. The calculated values as obtained from equation (3.11) are zero, 1.063 A/μs, 1.097 A/μs respectively In the third time interval no current flows through any of the switch nor the inductance and thus, they are zero in all the three cases. The measured efficiency of the converter is 90 %. The obtained simulated results are in good agreement with the theoretical calculations

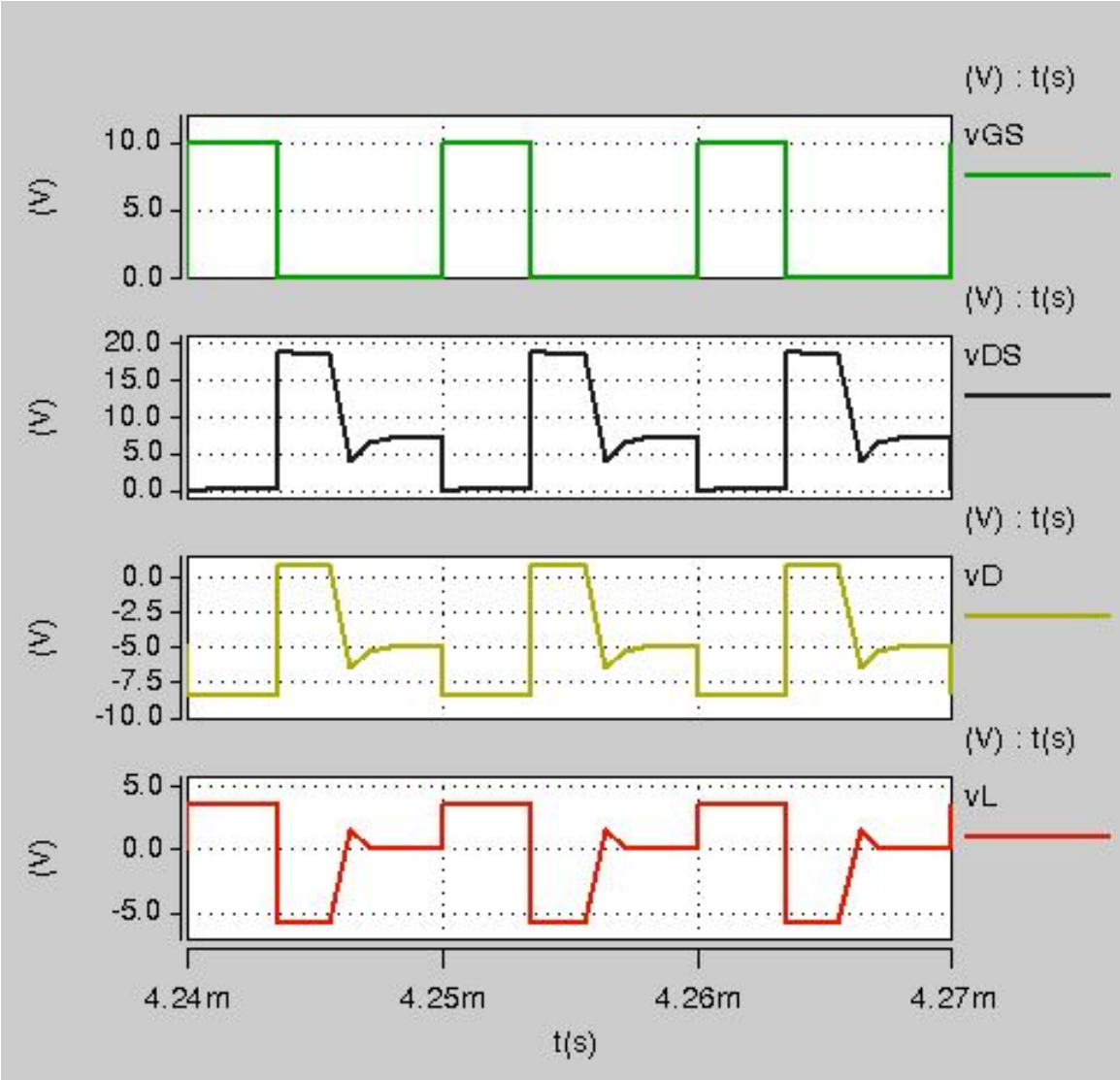

Figure 3.9: Simulated waveforms of the drain-to-source voltage, gate-to-source voltage, diode voltage, and voltage across inductance.

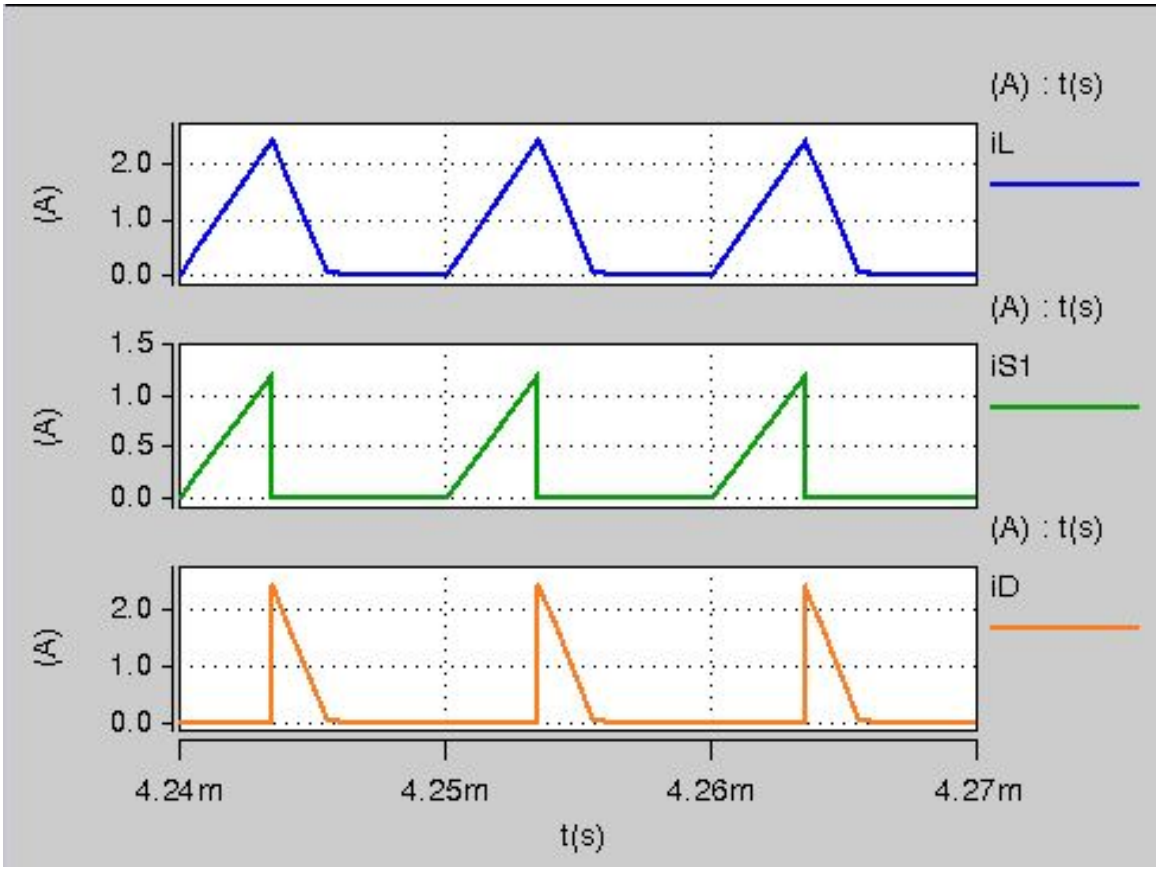

Figure 3.10: Simulated waveforms of the inductor current, switch current, and diode current.

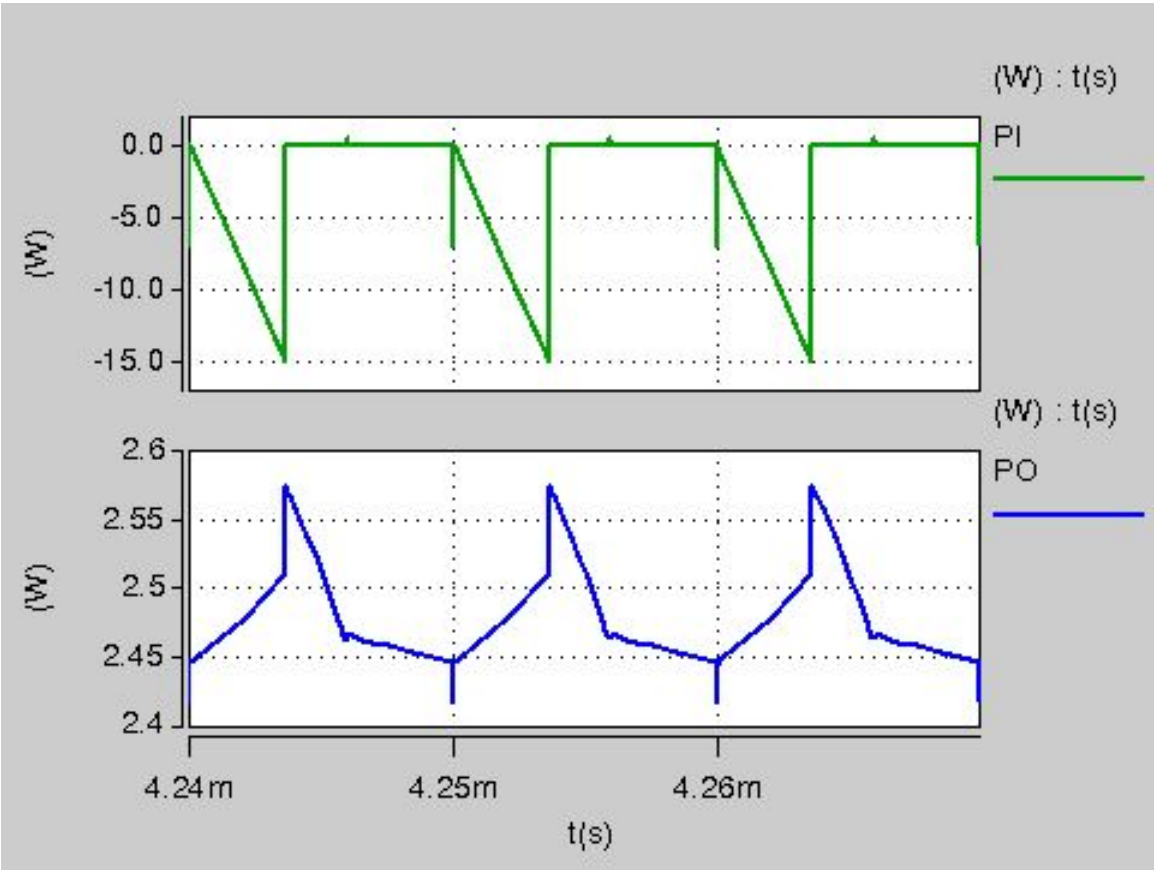

Figure 3.11: Simulated waveforms of input and output powers.

3.5 Experimental Validation of the Analysis of the Power Stage Running in DCM in Time-Domain.

For the experimental validation of the converter running in DCM the similar specification from the previous section is used. To maintain the converter in DCM a tapped-inductor is designed for 5 μH inductance. To maintain the required amount of current a P-type 18/11 core ferrite core was used. The primary to secondary turns ratio was maintained at $N_1/N_2 = 1$. The measured DC parasetic was $r_L = 0.5\ \Omega$. The selected capacitor to maintain the output ripple is 47 μF. The measured DC parasitic across the capacitor is $r_C = 0.5\ \Omega$. To withstand the stresses across the switches the selected semi conductive switches are IRF640 and MUR10100. A high bandwidth driver IR2117 was used for switching the MOSFET. HP6266B DC power supply was to power up the the converter and can be used to provide input voltage between 0-40 V and currents between 0-5 A. A Tektronix AFG3251 function generator was used to produce pulses for the driver input and HP E3631A power supply was used to power up the driver. The voltage and current profile can now be verified as seen in Figs. 3.13, 3.14 and 3.15. The voltages and current profile in the first time interval are as follow. From (3.7), the voltage across the diode is given by

$$v_D = -\frac{V_I + (n-1)V_O}{n} = -8.5\ \text{V}. \tag{3.66}$$

Since the diode is in off state the current flowing though it is zero. When the MOSFET switch is on the voltage across the switch is zero. The slope of the current flowing through the MOSFET is given by

$$i_{S1slope} = \frac{V_I - V_O}{n^2 L} = 0.35\ \text{A}/\mu\text{s}. \tag{3.67}$$

Voltage across the magnetizing inductance as seen in (3.2) is

$$v_L = \frac{V_I - V_O}{n} = 3.42\ \text{V}. \tag{3.68}$$

The slope of the current flowing through the magnetizing inductor is

$$i_{Lslope} = \frac{V_I - V_O}{nL} = 0.7 \text{ A}/\mu\text{s}. \tag{3.69}$$

During the second time interval the MODFET is off and the diode is on. Therefore, the voltage across the diode and the current flowing through the MOSFET are zero. The voltage across the MOSFET switch is given by

$$v_{S1} = V_I + (n-1)V_O = 17 \text{ V}. \tag{3.70}$$

The slope of the current flowing through the diode and the magnetizing inductance is given by

$$i_{Lslope} = i_{Dslope} = -\frac{V_O}{L} = 1 \text{ A}/\mu\text{s}. \tag{3.71}$$

During the third time interval both the MOSFET and the diode switches are off. No current flows thoug the switches. The voltage across the MOSFET is

$$v_{S1} = V_I - V_O = 7 \text{ V} \tag{3.72}$$

and the voltage across diode is

$$v_D = -V_O = -5 \text{ V}. \tag{3.73}$$

The bench setup required for the measurements can be seen in Fig. **??**. The measured voltage profiles can be seen in Fig. **??**. The measured profiles of the current flowing through the MOSFET switch and the output load can be sen in Figs. 3.14 and 3.15 respectively. The output current profile is also a representation of current flowing through the inductor and the diode during different time intervals. During the first time interval the measured values of voltages across MOSFET, diode and magnetizing inductor are zero, -8.4 V and 3.2 V respectively. The slope of the currents flowing through the MOSFET and diodes are 0.30 A/μs and zero respectively. During the second time period the measured values of voltages across MOSFET, diode

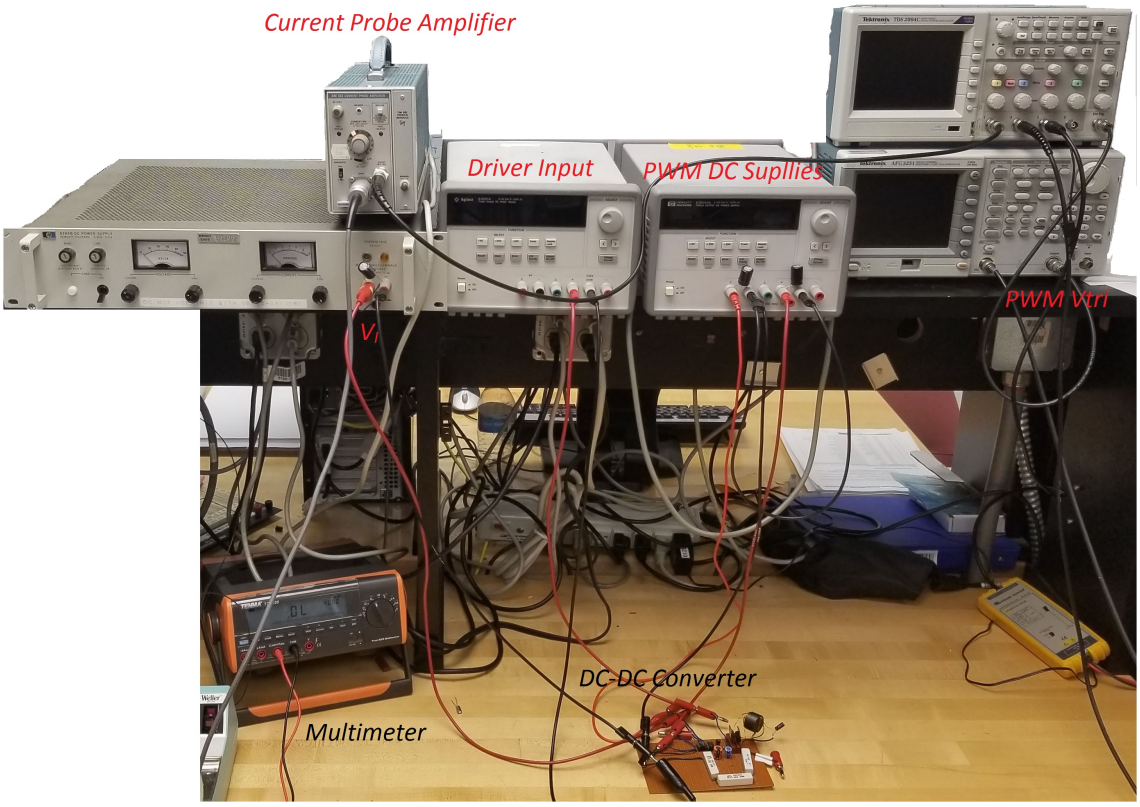

Figure 3.12: Experimental setup.

and magnetizing inductor are 7.2 V, zero and 0.4 V respectively. The measured slope of the currents flowing through the MOSFET and diodes are zero and 0.88 A/μs respectively. During the third time interval, the voltages across the MOSFET and diode switches are 7.2 V and -5 V respectively. The measured efficiency of the converter can be calculated by measuring the output power by using a multimeter. It was observed to be equal to 90 %. The measured values are in good agreement with

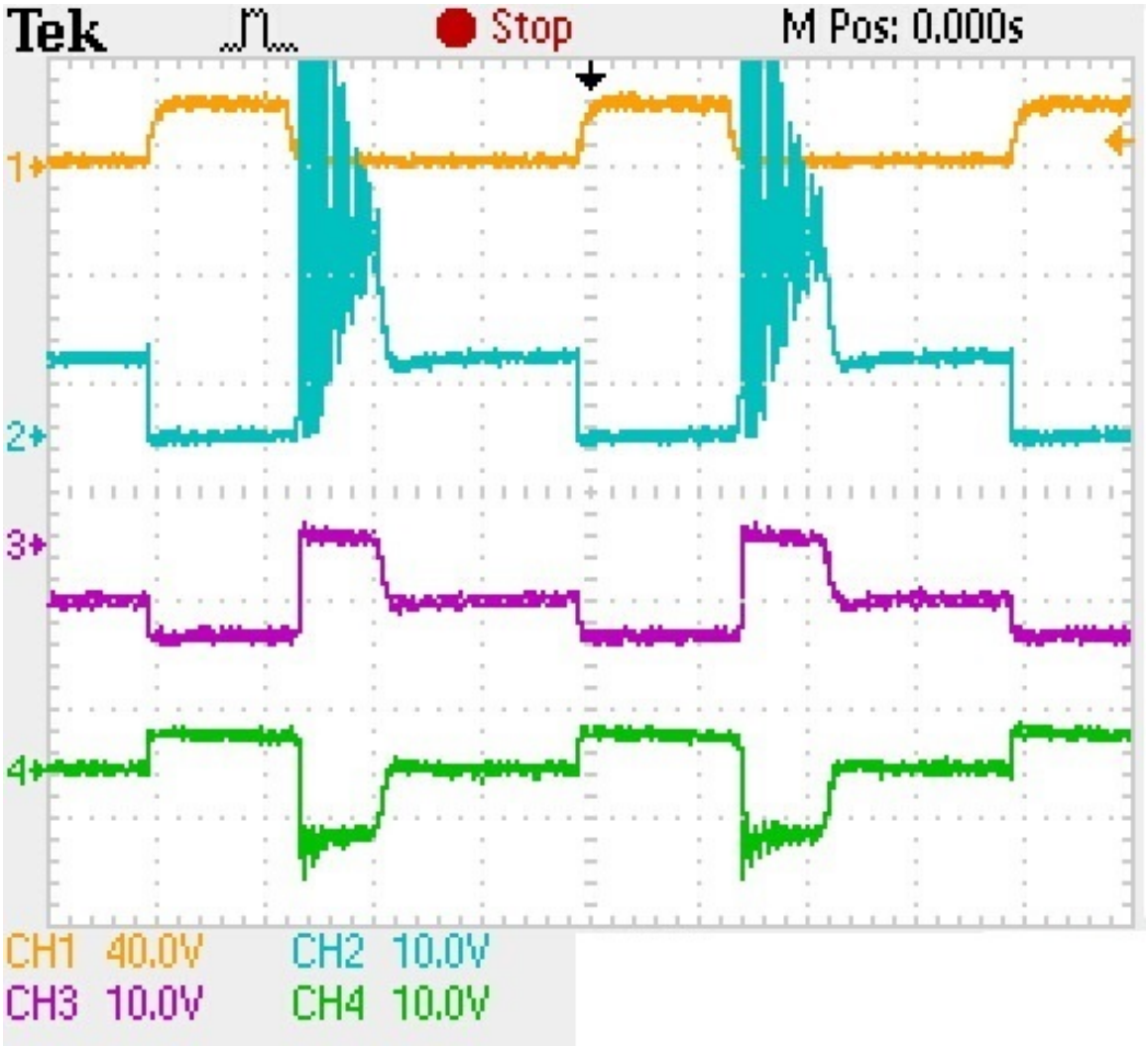

Figure 3.13: Experimental waveforms of the drain-to-source voltage, gate-to-source voltage, diode voltage, and voltage across inductance.

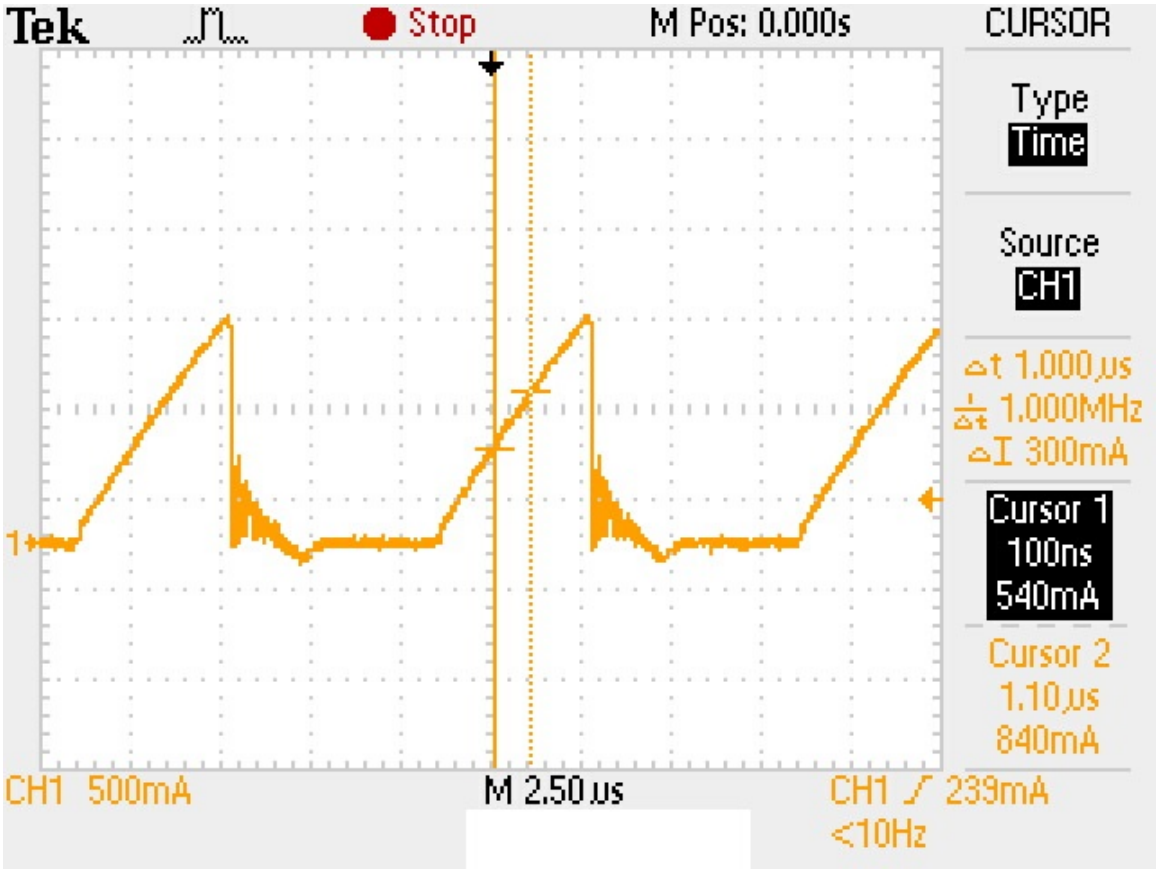

Figure 3.14: Experimental waveforms of the current flowing through MOSFET.

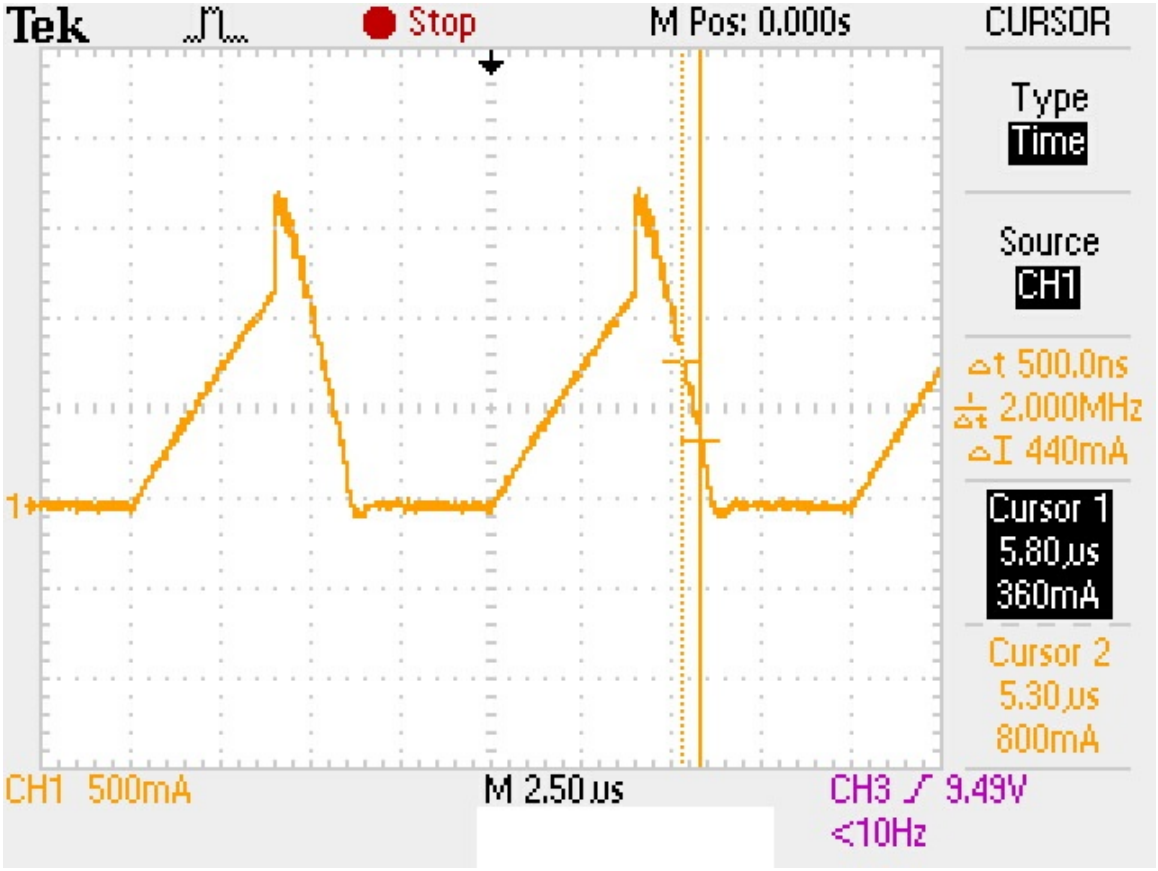

Figure 3.15: Experimental waveforms of the current flowing to the output of the converter

4 Small-Signal Modeling of Power Stage in CCM

This chapter presents the small-signal analysis of the power stage of a tapped-inductor pulse-width modulated (PWM) buck dc-dc converter operating in continuous-conduction mode(CCM). Using circuit averaging technique, the small-signal model of the power stage is derived. The derivation of duty cycle-to-output voltage and input-to-output voltage transfer functions are presented. An example tapped inductor buck dc-dc converter is considered. The time-domain and frequency-domain characteristics of the converter are analyzed and discussed. The theoretical results are validated using circuit simulations.

The steady-state analysis of the common-diode tapped-inductor buck converter was analyzed in previous chapter. Here the derivation of its small-signal model and subsequently, its power stage transfer functions such as duty cycle-to-output voltage and input voltage-to-output voltage. The small-signal model of the converter has been derived using circuit averaging technique, where the nonlinear switching network is replaced by a linearized two-port network of controlled voltage and current sources. The transient and frequency-domain characteristics of the converter are analyzed using the design of an example tapped-buck circuit topology and are verified circuit simulations.

4.1 Average Model

4.1.1 Average Switch Model

The relationship between the dc input and the dc output side current as seen in (2.27) is given by

$$I_I = \frac{D}{D + n(1-D)} I_O. \tag{4.1}$$

The average value of switch current is the dc input current, while the value of the current flowing though the output impedance is equal to the dc output current.

$$I_{S1} = \frac{D}{D + n(1-D)} I_{Z_2}. \tag{4.2}$$

The non-linear large-signal equation that can be represented from the dc equation

$$i_{S1} = \frac{d_T i_{Z_2}}{d_T + n(1-d_T)}, \tag{4.3}$$

where

$$i_{S1} = I_{S1} + i_{s1}, \tag{4.4}$$

$$i_{Z_2} = I_{Z_2} + i_{z_2}, \tag{4.5}$$

and

$$d_T = D + d. \tag{4.6}$$

The non-linear larger-signal model of the switch can now be represented as seen in Fig. 4.1. Substituting (4.4), (4.5) and (4.6) into (4.3), the non-linear equation can be represented as

$$I_{S1} + i_{s1} = \frac{(D+d)(I_{Z_2} + i_{z_2})}{D + d + n(1-D-d)}. \tag{4.7}$$

Rearranging the equation produces

$$(I_{S1} + i_{s1})[D + d + n(1-D-d)] = (D+d)(I_{Z_2} + i_{z_2}). \tag{4.8}$$

Simplification yields

$$\begin{aligned} DI_{S1} + nI_{S1} - nDI_{S1} + I_{S1}d - nI_{S1}d + i_{s1}D + i_{s1}d + ni_{s1} - nDi_{s1} - ni_{s1}d \\ = DI_{Z_2} + Di_{z_2} + I_{Z_2}d + i_{z_2}d. \end{aligned} \tag{4.9}$$

The above mentioned equation is non-linear in nature due to the presence of higher order small-signal ac components. This can be linearized by considering the following

$$i_{s1}d \ll I_{S1}d, \tag{4.10}$$

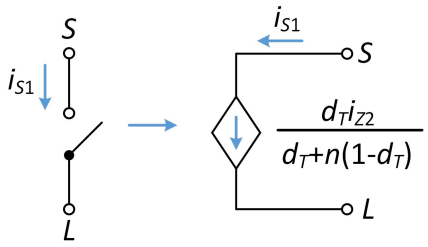

Figure 4.1: Non-linear large-signal model of the MOSFET switch used in PWM tapped-inductor buck converter.

$$i_{s1}d \ll Di_{s1}, \tag{4.11}$$

$$i_{s1}d \ll ni_{s1}, \tag{4.12}$$

$$i_{s1}d \ll Di_{z_2}, \tag{4.13}$$

$$i_{s1}d \ll I_{Z_2}d, \tag{4.14}$$

$$i_{z_2}d \ll I_{S1}d, \tag{4.15}$$

$$i_{z_2}d \ll Di_{s1}, \tag{4.16}$$

$$i_{z_2}d \ll ni_{s1}, \tag{4.17}$$

$$i_{z_2}d \ll Di_{z_2}, \tag{4.18}$$

and

$$i_{z_2}d \ll I_{Z_2}d. \tag{4.19}$$

The linear equation obtained by using the above inequality is

$$\begin{aligned} \underbrace{DI_{S1} + nI_{S1} - nDI_{S1}}_{dc} + \underbrace{I_{S1}d - nI_{S1}d + Di_{s1} + ni_{s1} - nDi_{s1}}_{ac} \\ = \underbrace{DI_{Z_2}}_{dc} + \underbrace{Di_{z_2} + I_{Z_2}d}_{ac}. \end{aligned} \tag{4.20}$$

The circuit representing the above mentioned equation can be seen in Fig. 4.2. Since this equation is linear in nature theory of superposition can be used to split the dc and ac equations to get

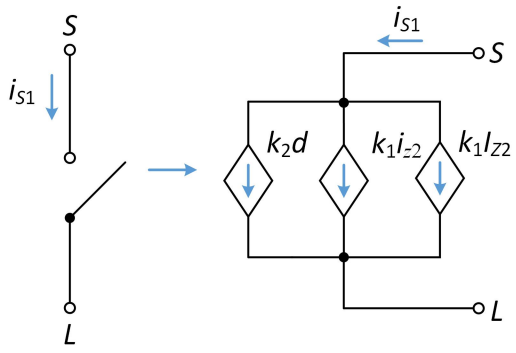

Figure 4.2: Linear large-signal model of the MOSFET switch used in PWM tapped-inductor buck converter.

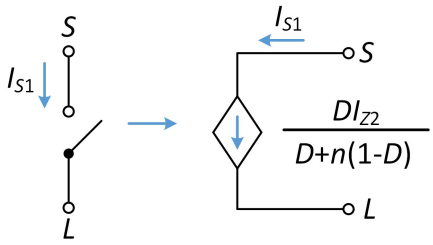

Figure 4.3: Dc model of the MOSFET switch used in PWM tapped-inductor buck converter.

$$DI_{S1} + nI_{S1} - nDI_{S1} = DI_{Z_2}. \tag{4.21}$$

The obtained relationship between the dc quantities is

$$I_{S1} = \frac{I_{Z_2} D}{D + n(1-D)} = k_1 I_{Z_2}, \tag{4.22}$$

where

$$k_1 = \frac{D}{D + n(1-D)}. \tag{4.23}$$

The circuit representation of the above mentioned equation can be seen in Fig. 4.3 and is called the dc model. The other part of the equations (4.20) can be used to obtain the relationship between the ac quantities

$$I_{S1} d - nI_{S1} d + Di_{s1} + ni_{s1} - nDi_{s1} = Di_{z_2} + I_{Z_2} d. \tag{4.24}$$

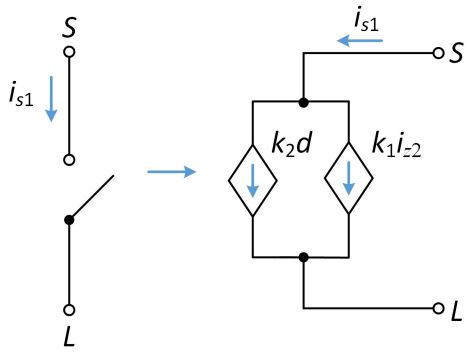

Figure 4.4: Small-signal model of the MOSFET switch used in PWM tapped-inductor buck converter.

Simplification helps obtain

$$i_{s1} = \frac{D}{D+(1-D)n} i_{z_2} + \frac{I_{Z_2}}{D+(1-D)n} d - \frac{I_{S1}(1-n)}{D+(1-D)n} d. \tag{4.25}$$

Substituting (4.22) into (4.25) and simplifying further produces the relationship between the ac components

$$i_{s1} = \frac{D}{D+(1-D)n} i_{z_2} + \frac{nI_{Z_2}}{[D+(1-D)n]^2} d = k_1 i_{z_2} + k_2 d, \tag{4.26}$$

where

$$k_1 = \frac{D}{D+(1-D)n}, \tag{4.27}$$

and

$$k_2 = \frac{nI_{Z_2}}{[D+(1-D)n]^2} = \frac{nI_O}{[D+(1-D)n]^2}, \tag{4.28}$$

where the average value of the current flowing through the output impedance is equivalent to the dc output current. The Fig. representing the small-signal model of the switch can be seen in Fig. 4.4.

4.1.2 Average Diode Model

From Fig. 2.1, when the switch is ON and the diode is OFF the kirchhoff's voltage law can be used to obtain

$$v_p + V_D = V_I \tag{4.29}$$

and

$$v_s + V_O = V_D. \tag{4.30}$$

From (2.1), (4.29) and (4.30), the diode voltage when the switch is on is given by

$$V_D = -\frac{V_I + (n-1)V_O}{n}. \tag{4.31}$$

From (2.25) and (4.31), the diode voltage is given by

$$V_D = -\frac{V_I}{D + n(1-D)}. \tag{4.32}$$

The voltage across the diode at different time intervals is

$$v_D = \begin{cases} \dfrac{V_I}{D + n(1-D)} & 0 < t \leq DT \\ \\ 0 & DT < t \leq T. \end{cases} \tag{4.33}$$

The average value of voltage across the diode is

$$V_D = -\frac{1}{T}\int_0^{DT} \frac{V_I}{D + n(1-D)} dt = -\frac{DV_I}{D + n(1-D)}. \tag{4.34}$$

The non-linear large-signal equation that can be represented from the DC equation are

$$v_D = -\frac{d_T v_I}{d_T + n(1-d_T)}, \tag{4.35}$$

where

$$v_D = V_D + v_d, \tag{4.36}$$

$$v_I = V_I + v_i, \tag{4.37}$$

and

$$d_T = D + d. \tag{4.38}$$

The non-linear larger-signal model of the diode can now be represented as seen in Fig. 4.5. Substituting (4.36), (4.38) and (4.38) into (4.35), the non-linear voltage equations can be represented as

$$V_D + v_d = -\frac{(D+d)(V_I + v_i)}{D + d + n(1-D-d)}. \tag{4.39}$$

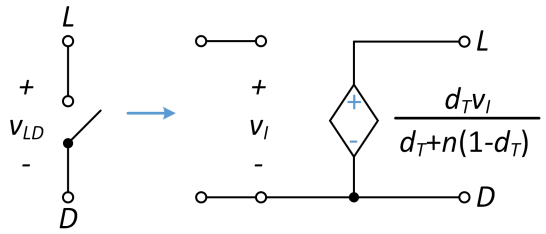

Figure 4.5: Non-linear large-signal model of diode used in PWM tapped-inductor buck converter.

Rearranging the equation produces

$$(V_D + v_d)[D + d + n(1 - D - d)] = -(D + d)(V_I + v_i). \tag{4.40}$$

Simplification yields

$$\begin{aligned} DV_D + nV_D - nDV_D + V_D d - nV_D d + v_d D + v_d d + nv_d - nDv_d - nv_d d \\ = -DV_I - Dv_i - V_I d - v_i d. \end{aligned} \tag{4.41}$$

The above mentioned equations are non-linear in nature due to the presence of higher order small-signal ac components this can be linearized by considering the following

$$v_d d \ll V_D d, \tag{4.42}$$

$$v_d d \ll D v_d, \tag{4.43}$$

$$v_d d \ll n v_d, \tag{4.44}$$

$$v_d d \ll D v_i \tag{4.45}$$

$$v_d d \ll V_I d. \tag{4.46}$$

$$v_i d \ll V_D d, \tag{4.47}$$

$$v_i d \ll D v_d, \tag{4.48}$$

$$v_i d \ll n v_d, \tag{4.49}$$

$$v_i d \ll D v_i \tag{4.50}$$

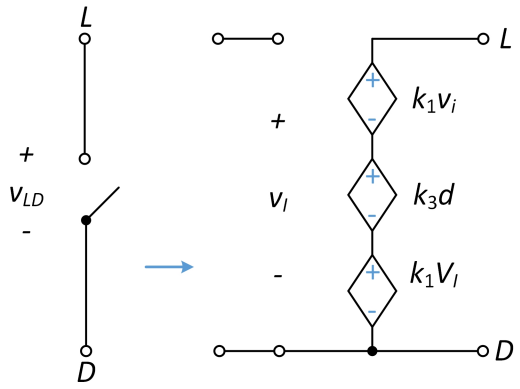

Figure 4.6: Linear large-signal model of diode used in PWM tapped-inductor buck converter.

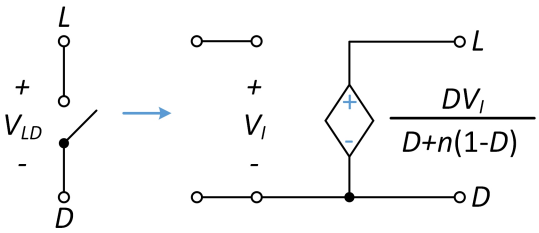

Figure 4.7: Dc model of diode used in PWM tapped-inductor buck converter.

and

$$v_i d \ll V_I d. \tag{4.51}$$

The linear equation obtained by using the above inequality is

$$\begin{aligned} \underbrace{DV_D + nV_D - nDV_D}_{dc} + \underbrace{V_D d - nV_D d + Dv_d + nv_d - nDv_d}_{ac} \\ = -\underbrace{DV_I}_{dc} - \underbrace{Dv_i - V_I d}_{ac}. \end{aligned} \tag{4.52}$$

The circuit representing the above mentioned equation can be seen in Fig. 4.6. Since the above mentioned equation is linear in nature theory of superposition can be used to split the dc and ac equations to get

$$DV_D - nDV_D + nV_D = -V_I D. \tag{4.53}$$

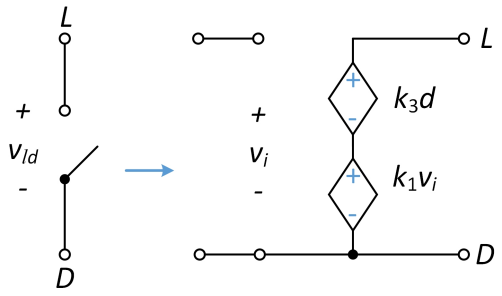

Figure 4.8: Small-signal model of diode used in PWM tapped-inductor buck converter.

The obtained relationship between the dc quantities is

$$V_D = -\frac{V_I D}{D + n(1-D)} = -k_1 V_I. \tag{4.54}$$

The circuit representing the above mentioned equation can be seen in Fig. 4.7and is called the dc model. The other part of the equations (4.52) can be used to obtain the relationship between the ac quantities

$$V_D d - nV_D d + v_d D + nv_d - nDv_d = -Dv_i - V_I d. \tag{4.55}$$

Simplifying it further for v_d gives us

$$v_d = -\frac{Dv_i}{D + (1-D)n} - \frac{V_I d}{D + (1-D)n} + \frac{V_D(1-n)d}{D + (1-D)n}. \tag{4.56}$$

Substituting (4.53) into (4.56) and simplifying further produces the relationship between the ac components

$$v_d = -\frac{D}{D + (1-D)n} v_i - \frac{nV_I}{[D + (1-D)n]^2} d = -k_1 v_i - k_3 d, \tag{4.57}$$

where

$$k_3 = \frac{nV_I}{[D + (1-D)n]^2} \tag{4.58}$$

The figure representing the small-signal model of the switch can be seen in Fig. 4.8.

4.1.3 Average Tapped-Inductor Model

The voltage across the primary winding at different time intervals as seen in equation (2.1), (2.4), and (2.18) is given by

$$V_P = \begin{cases} \dfrac{n-1}{n}(V_I + V_O) & 0 < t \leq DT \\ \\ -(n-1)V_O & DT < t \leq T. \end{cases} \tag{4.59}$$

The average value across the primary is given by

$$V_P = \frac{1}{T}\int_0^T v_P dt = \frac{1}{T}\int_0^{DT} \frac{n-1}{n}(V_I + V_O)dt + \frac{1}{T}\int_{DT}^T -(n-1)V_O dt \tag{4.60}$$

Simplifying the integration and substituting (2.25) into (4.60) produces

$$V_O(1-D)(n-1) - V_O(1-D)(n-1) = 0. \tag{4.61}$$

Since the average voltage across the primary of the tapped-inductor buck is zero, the average model can be represented as a short circuit.

$$v_p = (n-1)v_s. \tag{4.62}$$

The average value of current flowing through the MOSFET is equal to the average value of current in the primary of the tapped-inductor buck dc-dc conductor as seen in (4.26). The relationship between the primary and secondary current is given in (2.1). Using the above mentioned relationships the average value of current flowing through the secondary of the tapped-inductor buck is given by

$$I_S = \frac{(n-1)I_{Z_2}D}{D + n(1-D)} = k_1(n-1)I_{Z_2}, \tag{4.63}$$

For dc, the inductor in parallel to the secondary winding is a short circuit and thus leaving with just a wire representing the secondary. the dc model of the tapped-inductor can be seen in Fig. 4.9 A large-signal equation representing the transformer secondary given by

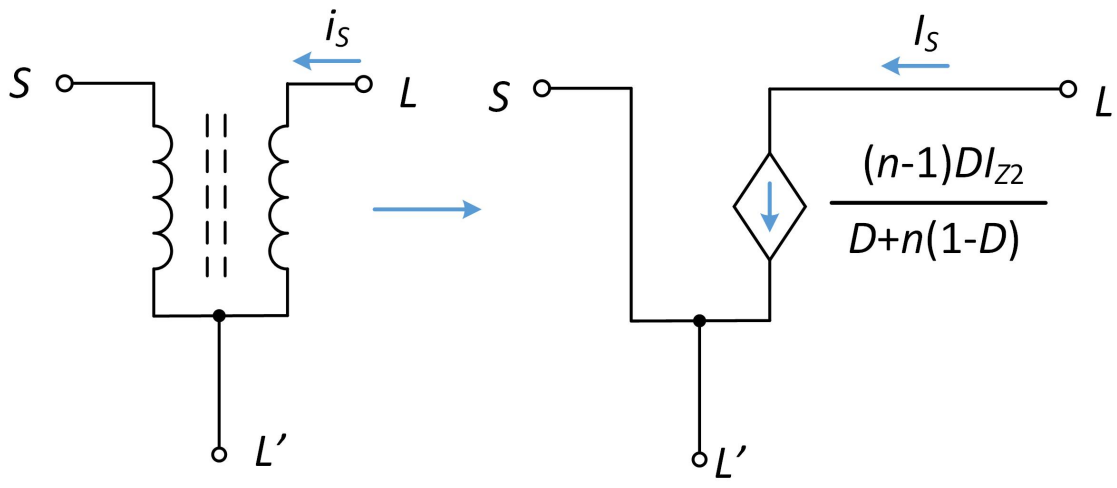

Figure 4.9: Dc model of the tapped-inductor used in the tapped-inductor buck converter.

$$i_S = \frac{(n-1)i_{Z_2}d_T}{d_T + n(1-d_T)}, \tag{4.64}$$

where

$$i_S = I_S + i_s, \tag{4.65}$$

$$i_{Z_2} = I_{Z_2} + i_{z_2}, \tag{4.66}$$

and

$$d_T = D + d. \tag{4.67}$$

The circuit representing non-linear large-signal model of a tapped-inductor can be seen in Fig. 4.10. The circuit representing a linear version can be seen in Fig. 4.11. The small-signal equation can be obtained from (4.26) as

$$\begin{aligned} i_s &= \frac{(n-1)D}{D+(1-D)n} i_{z_2} + \frac{n(n-1)I_{Z_2}}{[D+(1-D)n]^2} d \\ &= k_1(n-1)i_{z_2} + k_2(n-1)d. \end{aligned} \tag{4.68}$$

The circuit representing a small-signal model of a tapped-inductor as seen in Fig. 4.12 The equivalent averaged resistance r connected in series with the inductor is

$$r = Dr_{DS} + (1-D)R_F + r_L, \tag{4.69}$$

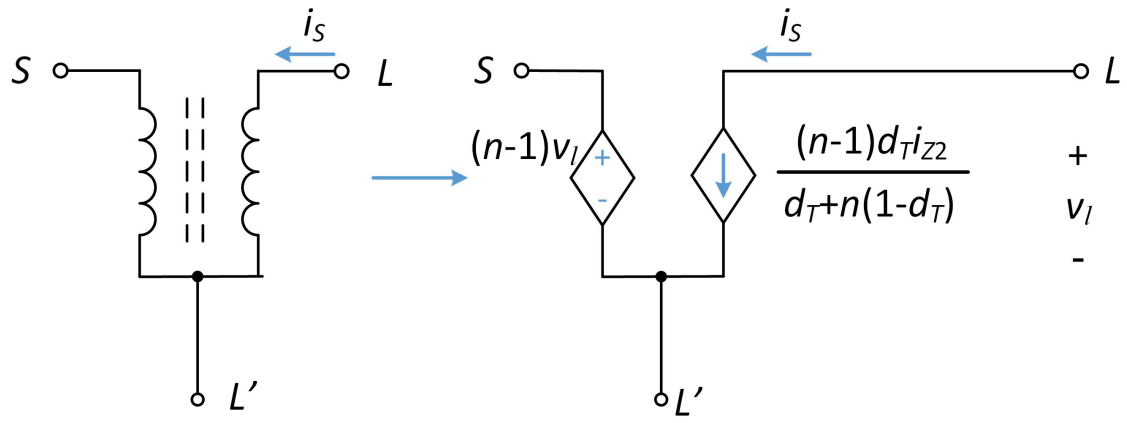

Figure 4.10: Non-linear large-signal model of the tapped-inductor used in PWM tapped-inductor buck converter.

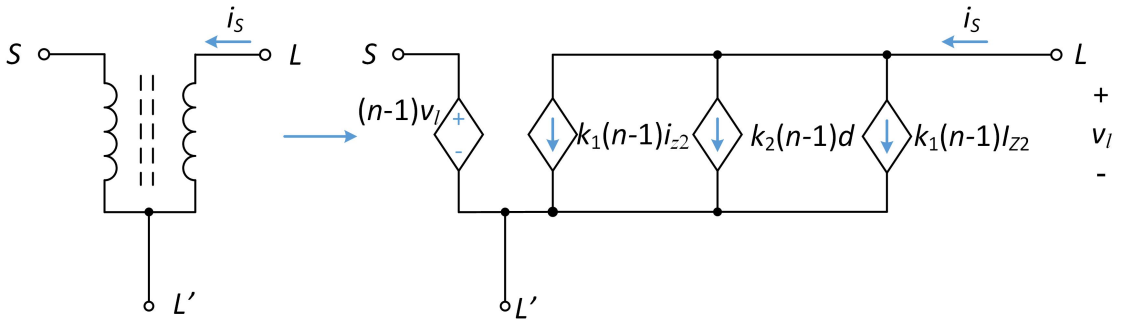

Figure 4.11: Linear large-signal model of the tapped-inductor used in PWM tapped-inductor buck converter.

where D is the duty cycle, r_{DS} is the ON-resistance of the switch, R_F is the diode forward resistance, and r_L is the parasitic resistance of the inductance. The non-linear large-signal model of the switch, the diode and the tapped-inductor as obtained in sub section 4.1.1, 4.1.2 and 4.1.3 can now be used to obtain the large signal model of the tapped-inductor buck dc-dc converter as seen in Fig. 4.13. This model can be reduced by using the linearized models of the switch and the diode to obtain the linear large-signal model of the converter as seen in Fig. 4.14. The equivalent dc and ac model can also be seen in Figs. 4.15 and 4.16 respectively.

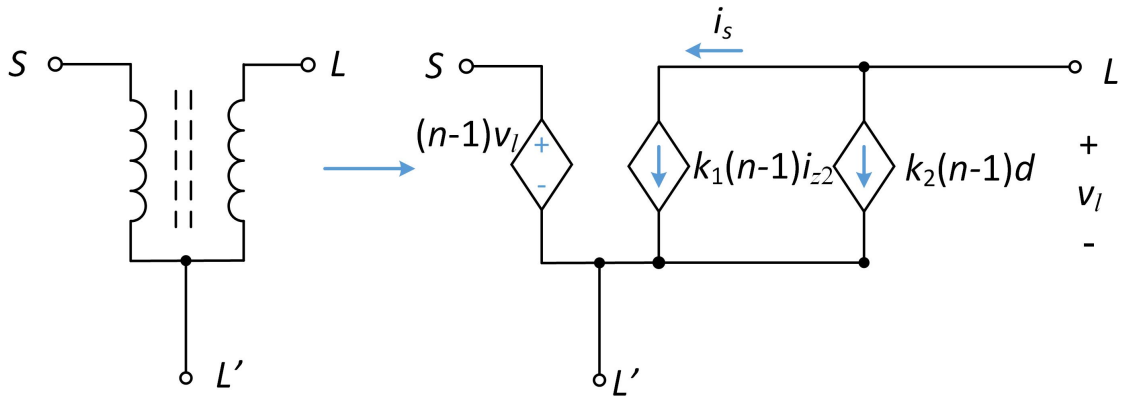

Figure 4.12: Small-signal model of the tapped-inductor used in PWM tapped-inductor buck converter.

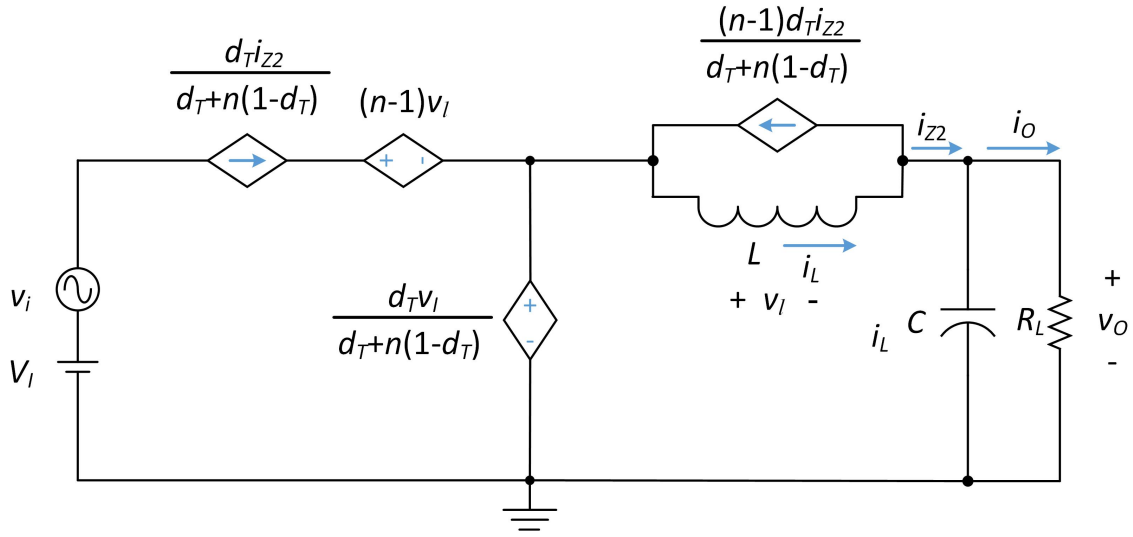

Figure 4.13: Non-linear large-signal model of a PWM tapped-inductor buck converter.

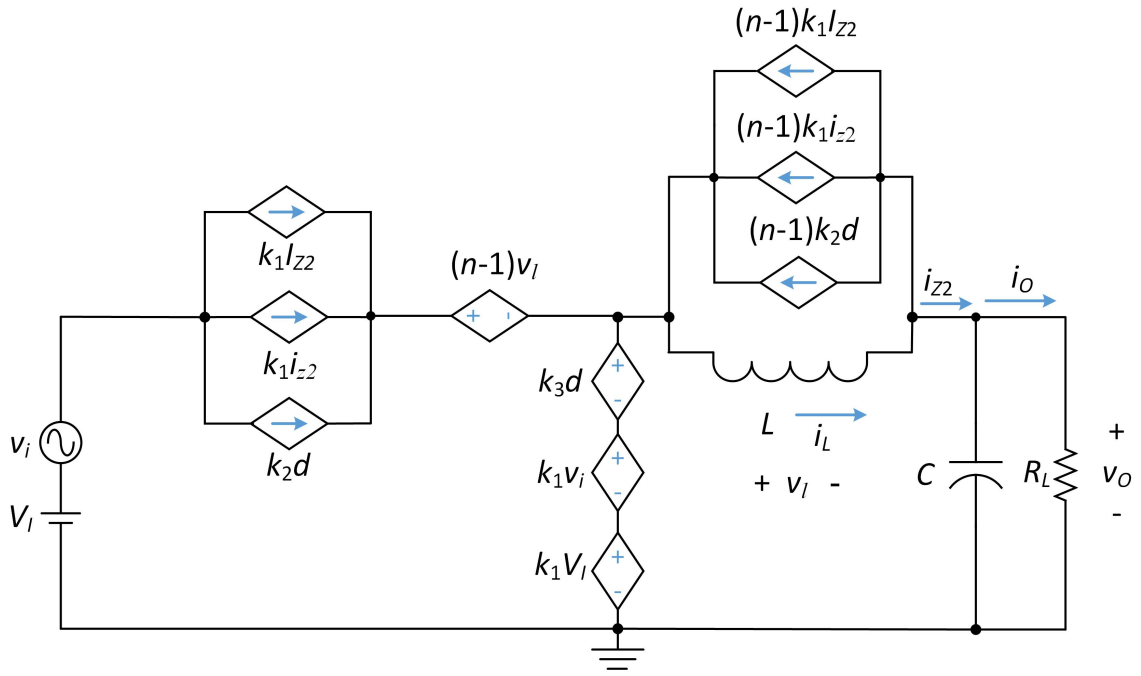

Figure 4.14: Linear large-signal model of a PWM tapped-inductor buck converter.

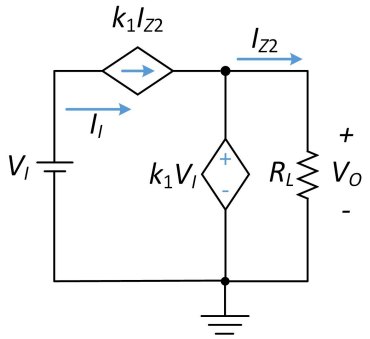

Figure 4.15: Dc model of a PWM tapped-inductor buck converter.

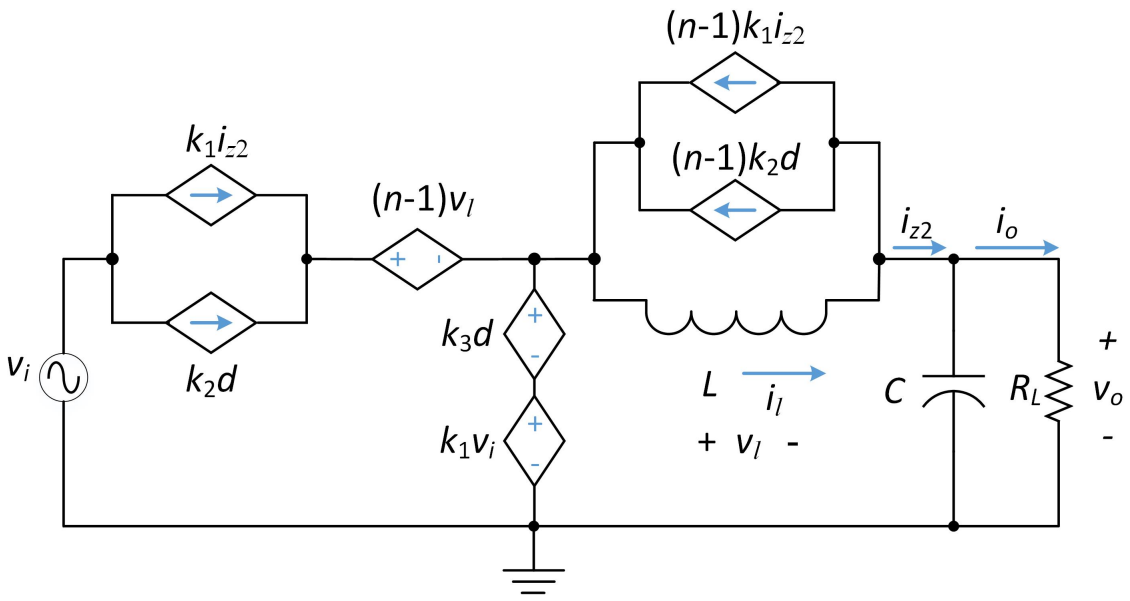

Figure 4.16: Small-signal model of a PWM tapped-inductor buck converter.

5 Derivation of Power Stage Transfer Functions in CCM

5.1 DC Transfer Functions

A dc model of a tapped-inductor buck dc-dc converter as seen in Fig. 4.15 is derived by replacing the switching components with averaged components. Since this is dc model the inductor is shorted and the capacitor is replaced with an open circuit. The kirchhoff's voltage law can be used to obtain

$$V_O = k_1 V_I = \frac{D}{D + (1-D)n} V_I. \tag{5.1}$$

The dc input-to-output voltage transfer function is given by

$$M_{VDC} = \frac{V_O}{V_I} = k_1 V_I = \frac{D}{D + (1-D)n}. \tag{5.2}$$

The dc control-to-output voltage transfer function is given by

$$T_{PDC} = \frac{V_O}{D} = k_1 V_I = \frac{V_O}{D + (1-D)n}. \tag{5.3}$$

5.2 Duty Cycle-to-Output Voltage Transfer Function T_p

The small-signal model of the PWM buck-boost converter is shown in Fig. 4.16. The resulting state equations required to derive the transfer functions are as follows. The impedance in the inductor and the capacitor branch are lumped and represented as

$$Z_1 = sL \tag{5.4}$$

and

$$Z_2 = R_L || \left(r_C + \frac{1}{sC} \right) = \frac{R_L \left(r_C + \frac{1}{sC} \right)}{R_L + r_C + \frac{1}{sC}}. \tag{5.5}$$

The duty cycle-to-output voltage transfer function is obtained by setting $v_i = 0$ in Fig. 4.16. The simplified circuit can be seen in Fig. 5.1. The current through the magnetizing inductance is

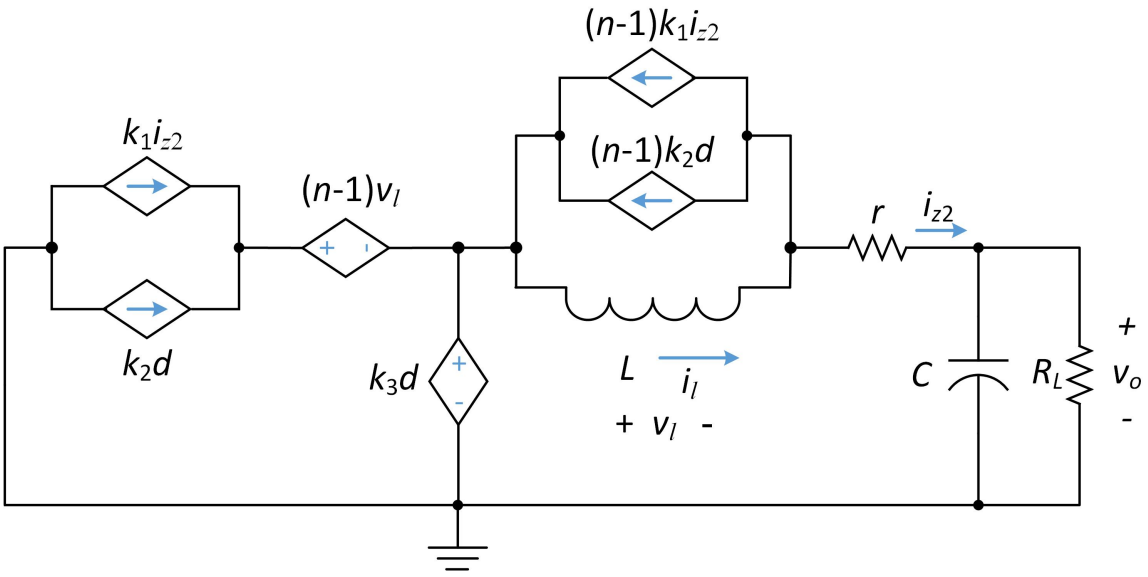

Figure 5.1: Simplified small-signal model of a PWM tapped-inductor buck converter to obtain transfer function T_p, when i_o=0 and v_i=0 .

$$i_l = i_{z_2} + (n-1)k_1 i_{z_2} + (n-1)k_2 d. \tag{5.6}$$

Applying Kirchof's voltage law

$$k_3 d = i_l Z_1 + i_{z_2}(r + Z_2). \tag{5.7}$$

This can be simplified to obtain i_l as

$$i_l = \frac{1}{Z_1}\left[k_3 d - \frac{v_o}{Z_2}(r + Z_2)\right]. \tag{5.8}$$

From (5.4), (5.5), (5.6), and (5.8), the control-to-inductor current transfer function in s-domain is

$$\begin{aligned} T_p(s) &= \frac{v_o(s)}{d(s)}|_{v_i=i_o=0} \\ &= -\frac{\left(\frac{k_2(n-1)R_Lr_C}{(R_L+r_C)(1+(n-1)k_1)}\right)\left(s-\frac{k_3}{L(n-1)k_2}\right)\left(s+\frac{1}{r_CC}\right)}{s^2+\frac{L(1+(n-1)k_1)+C(R_Lr+rr_C+R_Lr_C)}{LC(R_L+r_C)(1+(n-1)k_1)}s+\frac{(r+R_L)}{LC(R_L+r_C)(1+(n-1)k_1)}} \\ &= T_{px}\frac{(s+\omega_{zn})(s-\omega_{zp})}{s^2+2\xi\omega_0 s+\omega_0^2} = T_{po}\frac{\left(1+\frac{s}{\omega_{zn}}\right)\left(1-\frac{s}{\omega_{zp}}\right)}{\left(\frac{s}{\omega_0}\right)^2+\frac{2\xi s}{\omega_0}+1}, \end{aligned} \tag{5.9}$$

where the dc gain T_{po} is

$$T_{po} = \frac{R_Lk_3}{R_L+r} = \frac{R_LV_O}{R_L+r}\frac{n}{D[D+(1-D)n]}. \tag{5.10}$$

The gain T_{px} is

$$T_{px} = -\frac{k_2(n-1)R_Lr_C}{(R_L+r_C)\left[1+(n-1)k_1\right]} = -\frac{V_Or_C}{R_L+r_C}\frac{n-1}{[D+(1-D)n]}, \tag{5.11}$$

the angular corner frequency or the angular undamped natural frequency is

$$\omega_0 = \sqrt{\frac{(r+R_L)}{LC(R_L+r_C)(1+(n-1)k_1)}} = \sqrt{\frac{r+R_L}{LC(R_L+r_C)}\frac{D+(1-D)n}{n}}, \tag{5.12}$$

the damping ratio is

$$\begin{aligned} \xi &= \frac{L(1+(n-1)k_1)+C[rR_L+r_C(r+R_L)]}{2\sqrt{LC(R_L+r_C)(r+R_L)(1+(n-1)k_1)}} \\ &= \frac{Ln+C[rR_L+r_C(r+R_L)][D+(1-D)n]}{2\sqrt{nLC(R_L+r_C)(r+R_L)[D+(1-D)n]}}, \end{aligned} \tag{5.13}$$

the angular frequency of the left-half plane zero is

$$\omega_{zn} = \frac{1}{r_CC}, \tag{5.14}$$

and the angular frequency of the right-half plane zero is

$$\omega_{zp} = \frac{k_3}{L(n-1)k_2} = \frac{R_L}{L}\frac{D+(1-D)n}{D(n-1)}. \tag{5.15}$$

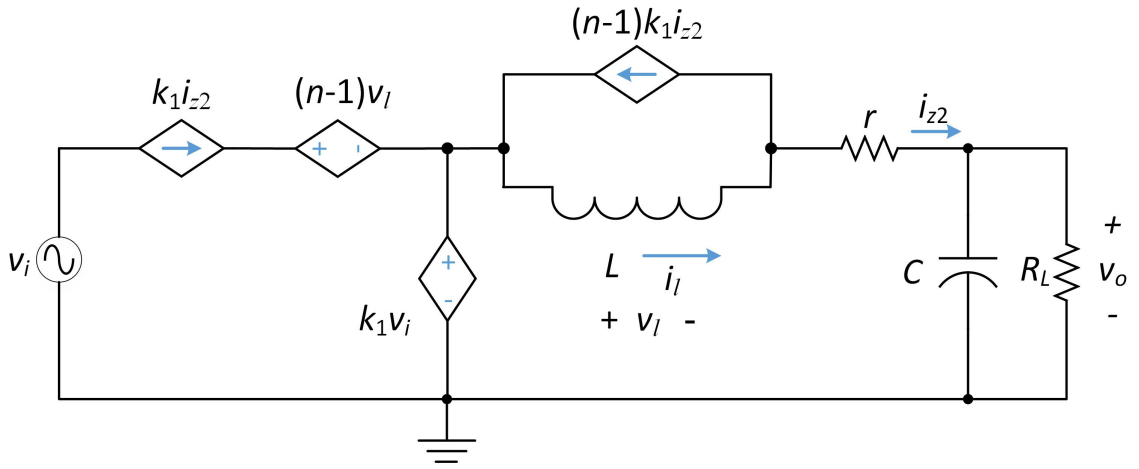

Figure 5.2: Simplified small-signal model of a PWM tapped-inductor buck converter to obtain transfer function M_v.

5.3 Input Voltage-to-Output Voltage Transfer Function M_v

The input voltage-to-output voltage transfer function is obtained by setting $d = 0$ in Fig. 4.16. The simplified circuit can be seen in Fig. 5.2. The current through magnetizing inductance is

$$i_l = i_{z_2} + (n-1)k_1 i_{z_2}. \tag{5.16}$$

Applying Kirchhoff's voltage law

$$k_1 v_i = i_l Z_1 + \left(\frac{r}{Z_2} + 1\right) v_o. \tag{5.17}$$

This can be simplified to obtain i_l as

$$i_l = \frac{1}{Z_1}\left[k_1 v_i - \frac{v_o}{Z_2}(r + Z_2)\right]. \tag{5.18}$$

From (5.4), (5.5), (5.16), and (5.18), the input voltage-to-output voltage transfer function in s-domain as

$$\begin{aligned} M_v(s) &= \frac{v_o(s)}{v_i(s)}|_{d=i_o=0} \\ &= \frac{\left(\frac{k_1 R_L r_C}{L(R_L+r_C)(1+(n-1)k_1)}\right)\left(s+\frac{1}{r_C C}\right)}{s^2+\frac{L(1+(n-1)k_1)+C(R_L r+r r_C+R_L r_C)}{LC(R_L+r_C)(1+(n-1)k_1)}s+\frac{(r+R_L)}{LC(R_L+r_C)(1+(n-1)k_1)}} \\ &= M_{vx}\frac{s+\omega_{zn}}{s^2+2\xi\omega_0 s+\omega_0^2} = M_{vo}\frac{1+\frac{s}{\omega_{zn}}}{\left(\frac{s}{\omega_0}\right)^2+\frac{2\xi s}{\omega_0}+1}, \end{aligned} \tag{5.19}$$

where the dc gain M_{vo} is

$$M_{vo} = \frac{k_1 R_L}{r+R_L} = \frac{R_L}{r+R_L}\frac{D}{D+(1-D)n}, \tag{5.20}$$

the gain M_{vx} is

$$M_{vx} = \frac{k_1 R_L r_C}{L(R_L+r_C\left[1+(n-1)k_1\right]} = \frac{R_L r_C}{L(R_L+r_C)}\frac{D}{n}, \tag{5.21}$$

the angular corner frequency or the angular undamped natural frequency is

$$\omega_0 = \sqrt{\frac{(r+R_L)}{LC(R_L+r_C)(1+(n-1)k_1)}} = \sqrt{\frac{r+R_L}{LC(R_L+r_C)}\frac{D+(1-D)n}{n}}, \tag{5.22}$$

the damping ratio is

$$\begin{aligned} \xi &= \frac{L(1+(n-1)k_1)+C[rR_L+r_C(r+R_L)]}{2\sqrt{LC(R_L+r_C)(r+R_L)(1+(n-1)k_1)}} \\ &= \frac{Ln+C[rR_L+r_C(r+R_L)][D+(1-D)n]}{2\sqrt{nLC(R_L+r_C)(r+R_L)[D+(1-D)n]}} \end{aligned} \tag{5.23}$$

the angular frequency of the left-half plane zero is

$$\omega_{zn} = \frac{1}{r_C C}, \tag{5.24}$$

5.4 Simulation Validation of the Power Stage

The design example used in Section 2.6 can be used to obtain the frequency response of the transfer functions derived in this chapter.

5.4.1 Frequency Response of T_p using MATLAB and SABER Circuit Simulator

Equation (5.9) can be used to obtain the frequency response of control-to-output voltage transfer function on MATLAB. The magnitude plot of this transfer function can be seen in Fig. 5.3 and the phase response can be seen in Fig. 5.4. The dc gain as obtained from

$$T_{po} = \frac{R_L k_3}{R_L + r} = \frac{R_L V_O}{R_L + r} \frac{n}{D[D + (1-D)n]} = 11.50, \tag{5.25}$$

on the decibel scale this is equal to 21.21 db. High frequency gain can be calculated from 5.11

$$T_{px} = -\frac{k_2(n-1)R_L r_C}{(R_L + r_C)(1 + (n-1)k_1)} = -\frac{V_O r_C}{R_L + r_C} \frac{n-1}{[D + (1-D)n]} = -0.0175, \tag{5.26}$$

on the decibel scale this is equal to -35.07 db. The angular corner frequency or the angular undamped natural frequency is

$$\begin{aligned} \omega_0 &= \sqrt{\frac{(r + R_L)}{LC(R_L + r_C)(1 + (n-1)k_1)}} \\ &= \sqrt{\frac{r + R_L}{LC(R_L + r_C)} \frac{D + (1-D)n}{n}} = 20.95 \times 10^3 \text{ rad/sec.} \end{aligned} \tag{5.27}$$

The corner frequency is

$$f_0 = \frac{\omega_0}{2\pi} = 3.33 \text{ KHz.} \tag{5.28}$$

The damping ratio is

$$\begin{aligned} \xi &= \frac{L(1 + (n-1)k_1) + C[rR_L + r_C(r + R_L)]}{2\sqrt{LC(R_L + r_C)(r + R_L)(1 + (n-1)k_1)}} \\ &= \frac{Ln + C[rR_L + r_C(r + R_L)][D + (1-D)n]}{2\sqrt{nLC(R_L + r_C)(r + R_L)[D + (1-D)n]}} = 0.45. \end{aligned} \tag{5.29}$$

The angular frequency of the left-half plane zero is

$$\omega_{zn} = \frac{1}{r_C C} = 70.92 \times 10^3 \text{ rad/sec}, \tag{5.30}$$

frequency of this left-half plane zero is given by

$$f_{zn} = \frac{\omega_{zn}}{2\pi} = 11.28 \text{ kHz}. \tag{5.31}$$

The angular frequency of the right-half plane zero is

$$\omega_{zp} = \frac{k_3}{L(n-1)k_2} = \frac{R_L}{L}\frac{D+(1-D)n}{D(n-1)} = 675 \times 10^3 \text{ rad/sec}, \tag{5.32}$$

and frequency of this right-half plane zero is

$$f_{zp} = \frac{\omega_{zp}}{2\pi} = 107 \text{ kHz}. \tag{5.33}$$

This can also be verified by using SABER circuit simulator to obtain the plots as seen in Fig. 5.5 and Fig. 5.6.

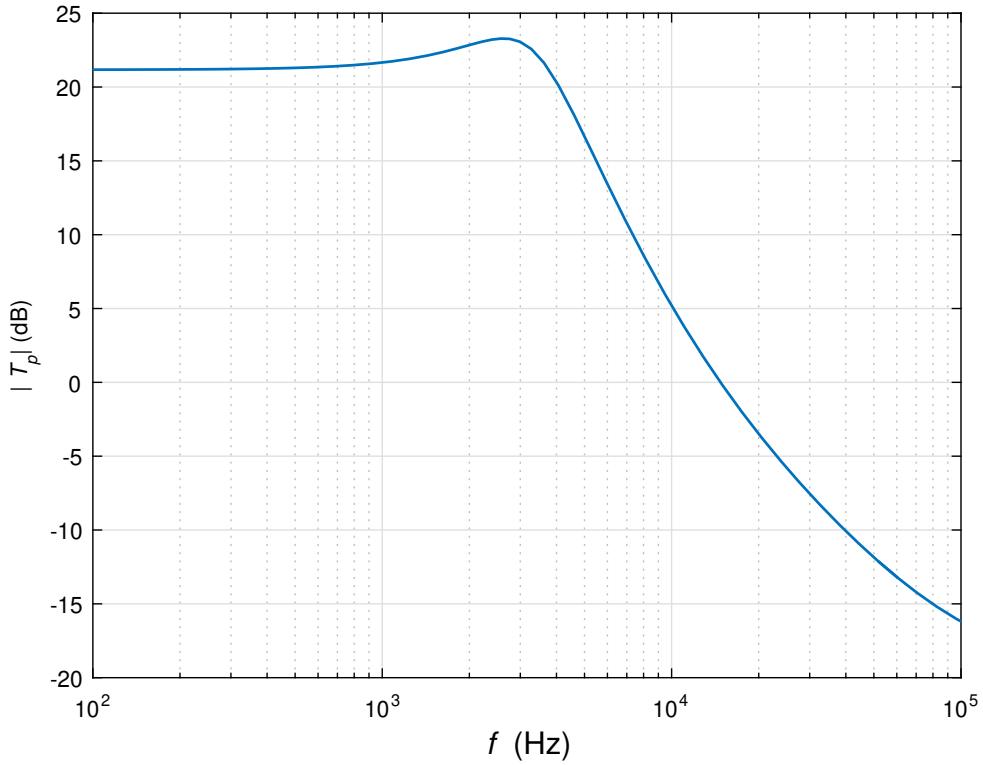

Figure 5.3: Magnitude plot of the T_p transfer function as obtained on MATLAB.

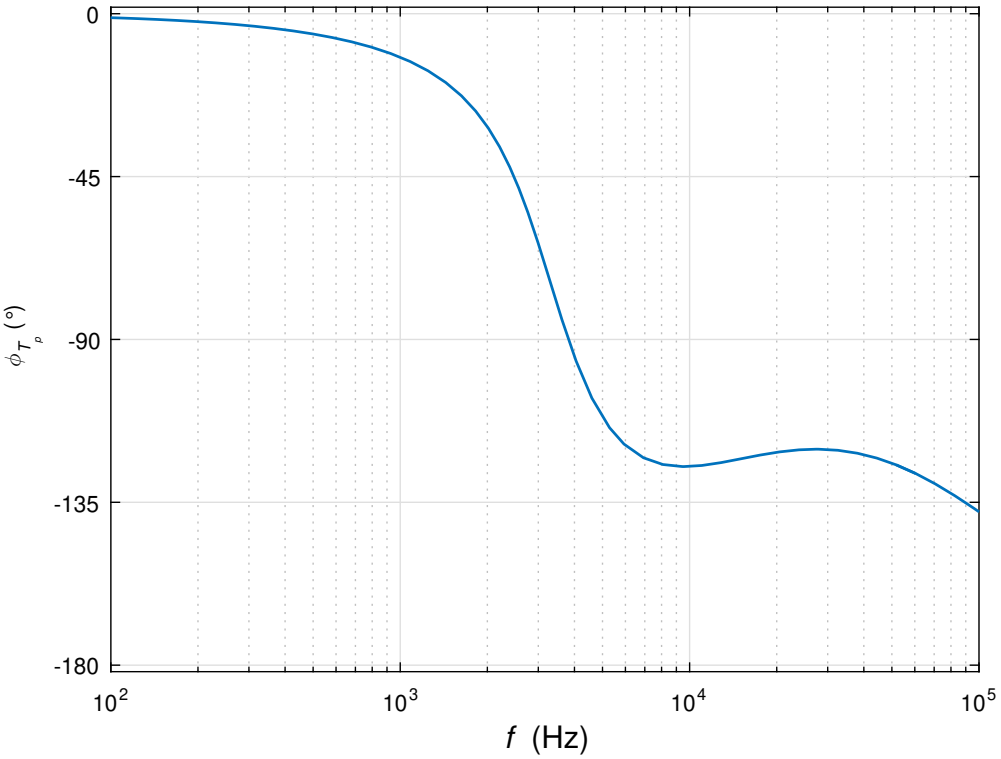

Figure 5.4: Phase plot of the T_p transfer function as obtained on MATLAB.

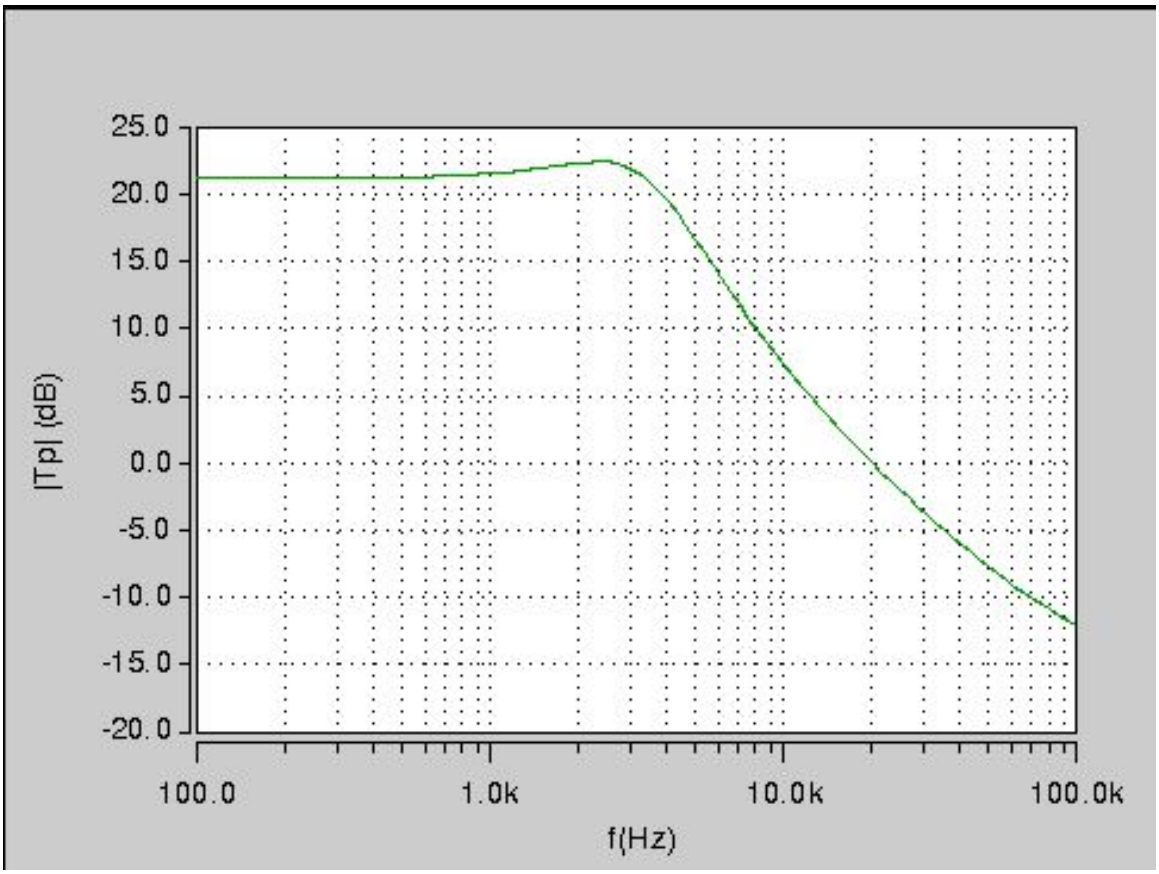

Figure 5.5: Magnitude plot of the T_p transfer function as obtained on SABER.

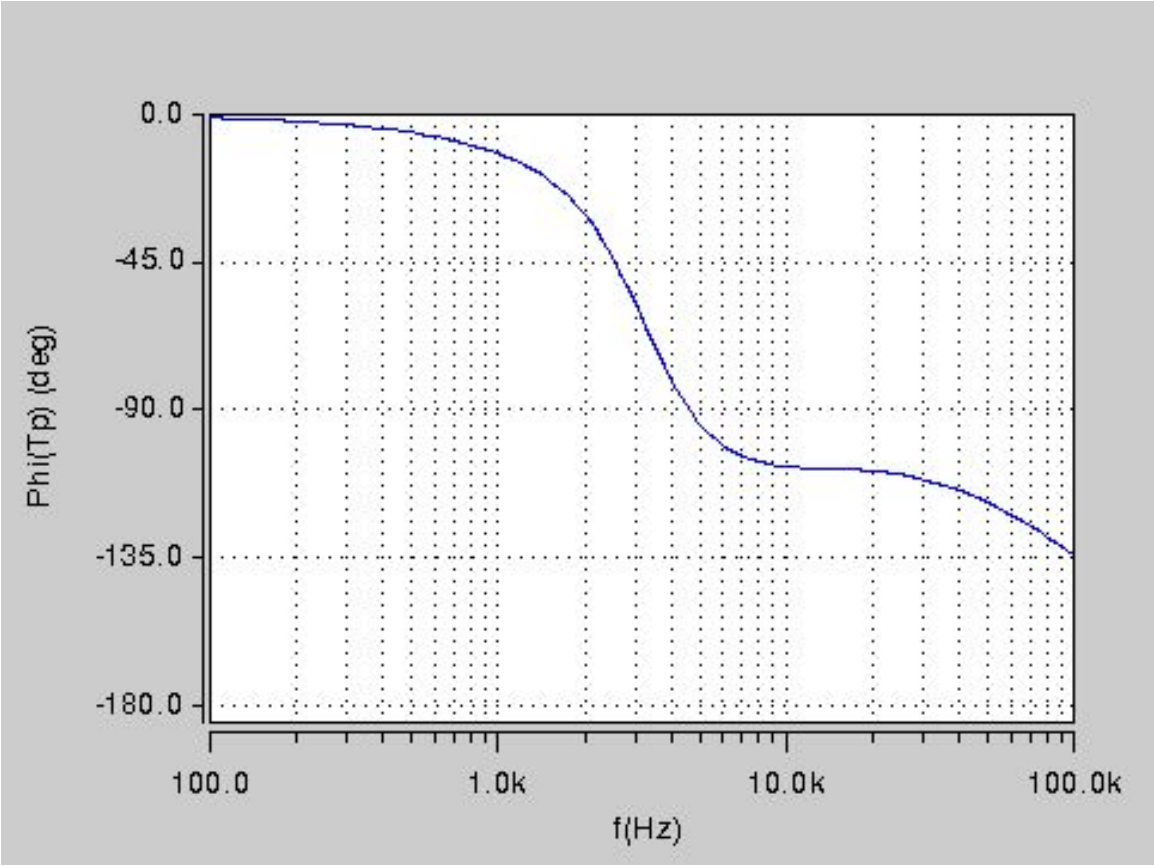

Figure 5.6: Phase plot of the T_p transfer function as obtained on SABER.

5.4.2 Frequency Response of M_v using MATLAB and SABER Circuit Simulator

The equation (5.19) can be used to obtain the frequency response of input-to-output voltage transfer function on MATALB. The magnitude plot of this transfer function can be seen in Fig. 5.7 and the phase response can be seen in Fig. 5.8. The dc gain can be obtained from

$$M_{vo} = \frac{k_1 R_L}{r + R_L} = 0.40, \tag{5.34}$$

on the decibel scale this is equal to -8 db. The gain M_{vx} is

$$M_{vx} = \frac{k_1 R_L r_C}{L(R_L + r_C)(1 + (n-1)k_1)} = \frac{R_L r_C}{L(R_L + r_C)} = 127.62, \tag{5.35}$$

on the decibel scale this is equal to 42.12 db. This can also be verified by using SABER circuit simulator to obtain the plots as seen in Fig. 5.9 and Fig. 5.10.

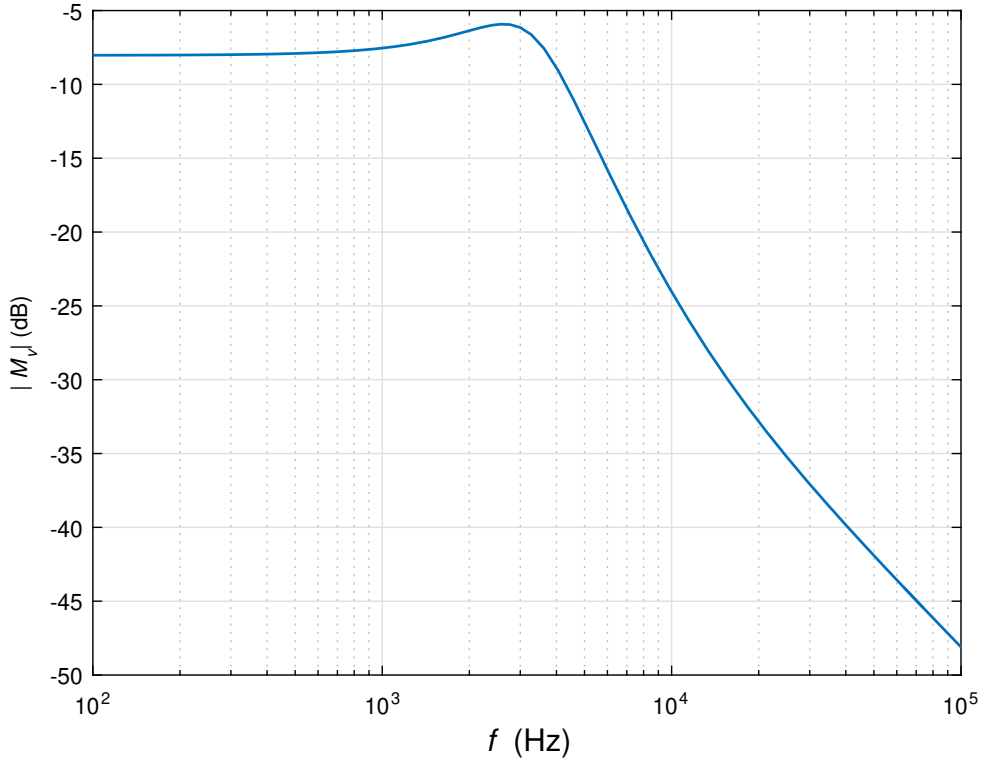

Figure 5.7: Magnitude plot of the M_v transfer function as obtained on MATLAB.

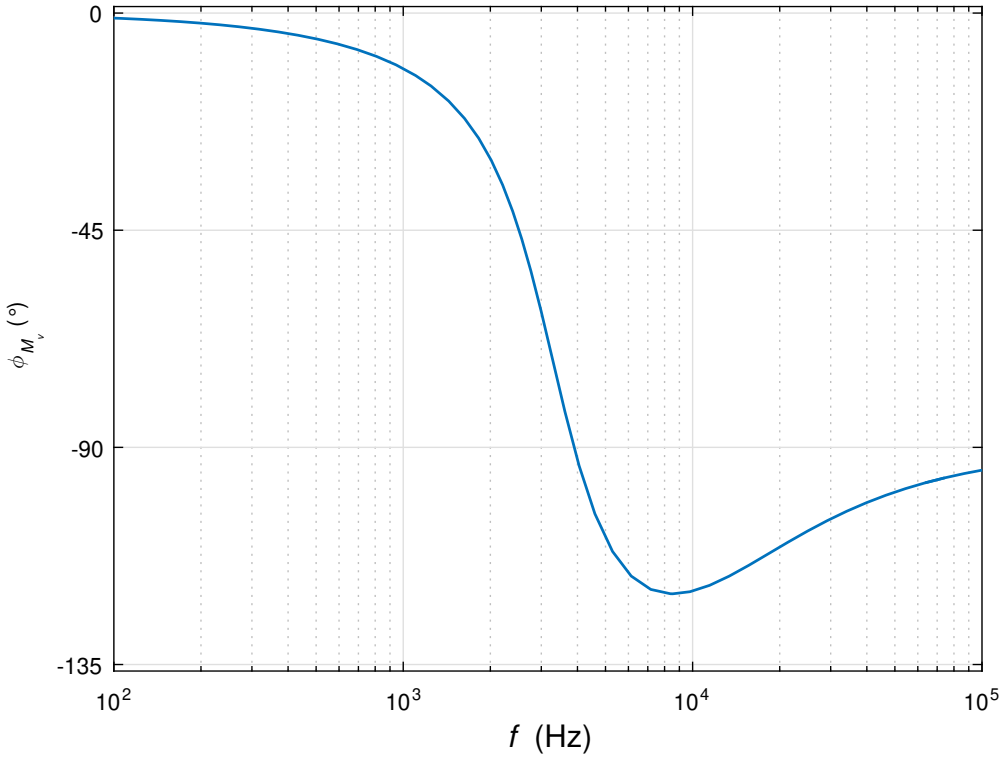

Figure 5.8: Phase plot of the M_v transfer function as obtained on MATLAB.

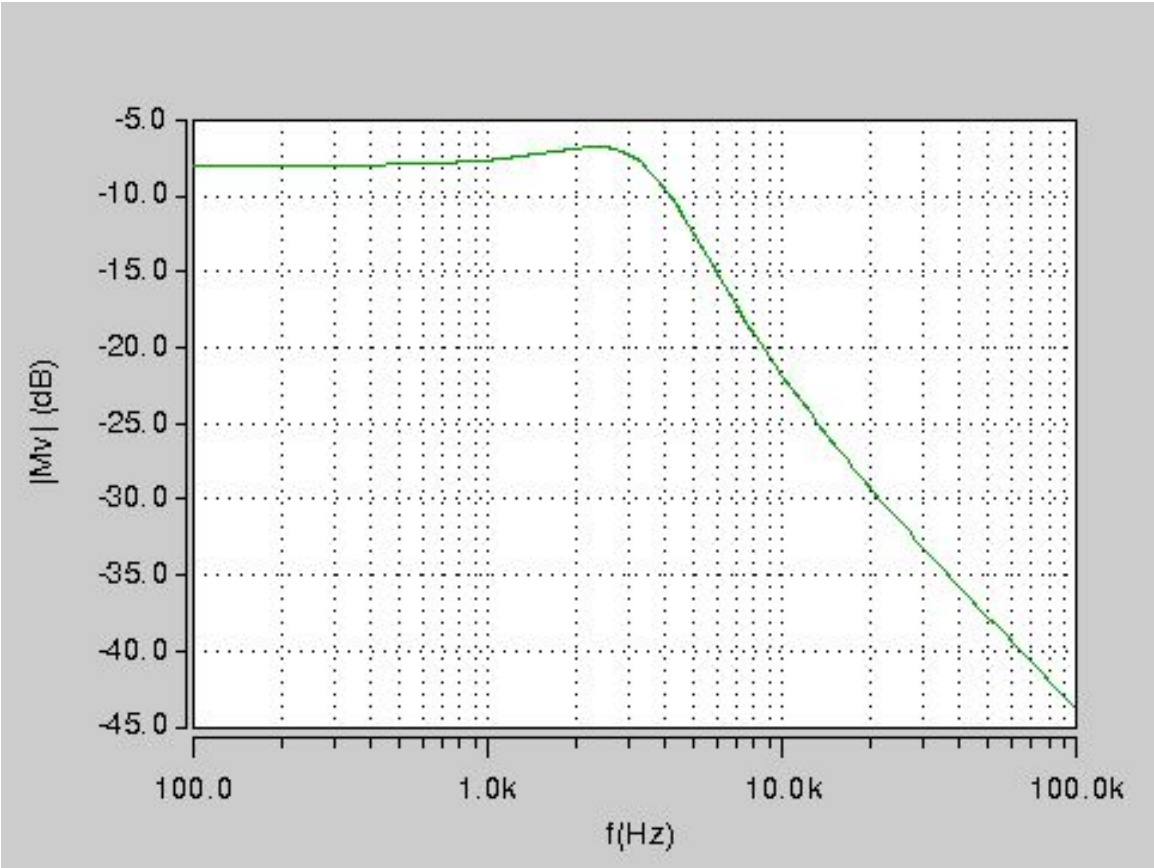

Figure 5.9: Magnitude plot of the M_v transfer function as obtained on SABER.

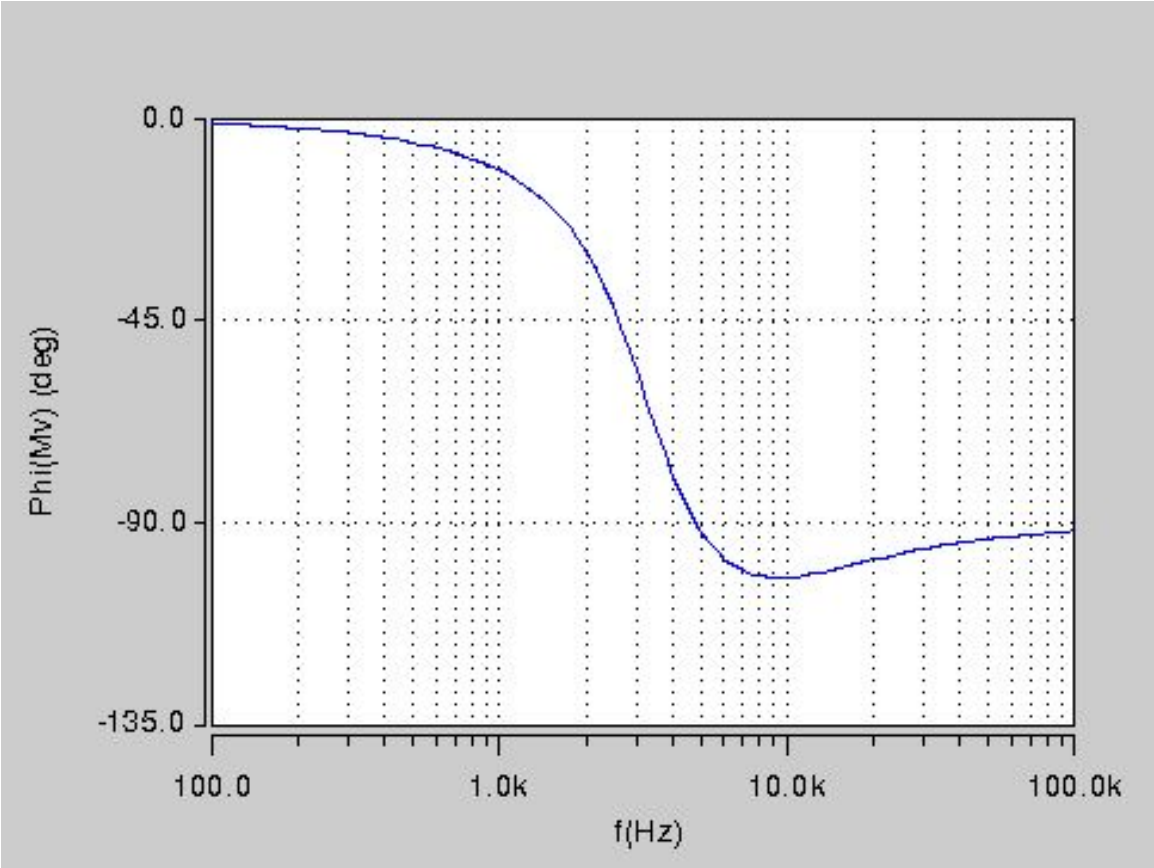

Figure 5.10: Phase plot of the M_v transfer function as obtained on SABER.

5.4.3 Response of Output Voltage for a Step Change in Duty Cycle

The step responses of transfer function T_p can be obtained by implementing $\Delta D = 0.1$ on MATLAB and can be seen in Fig. 5.11. The measured values of overshoot, rise time and settling time are 5 %, 70 μsec, 0.3 msec respectively.

5.4.4 Response of Output Voltage for a Step Change in Input Voltage

The step responses of the transfer function M_v for a step change of $\Delta V_I = 1$ V as obtained on MATLAB and SABER can be seen in Figs. 5.13 and 5.14 respectively. The measured values of overshoot, rise time and settling time are 1.7 %, 69.3 μsec, 0.4 msec respectively.

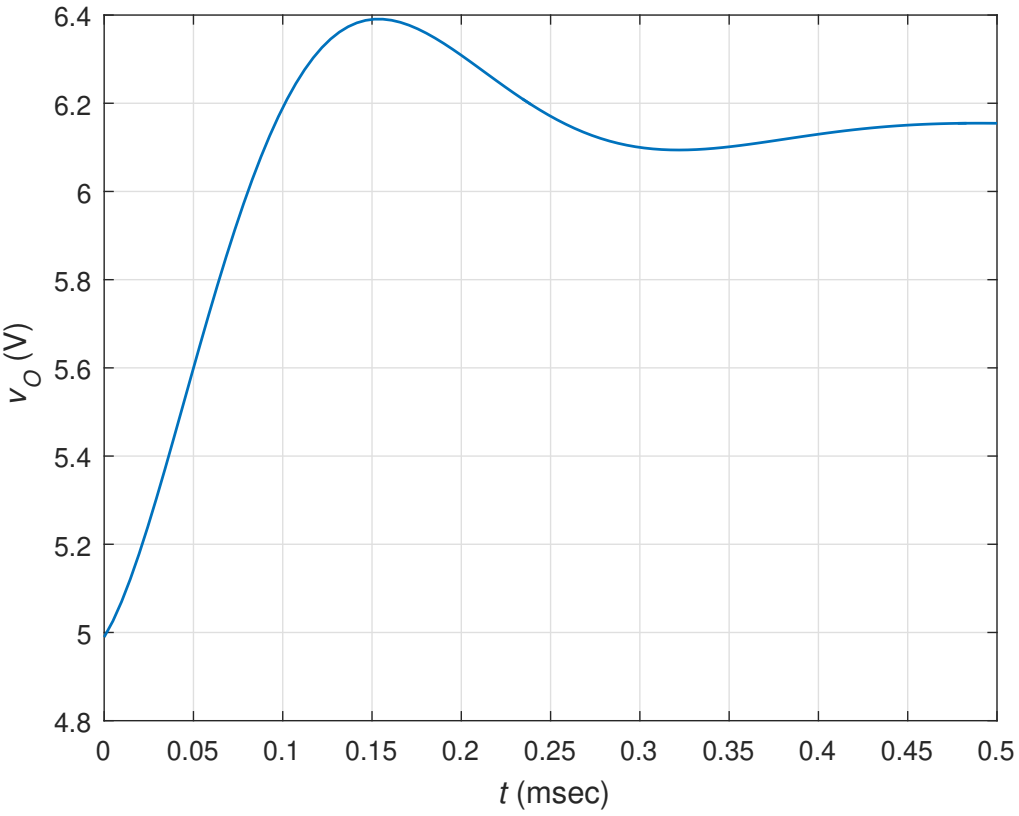

Figure 5.11: Step response of T_p as obtained on MATLAB.

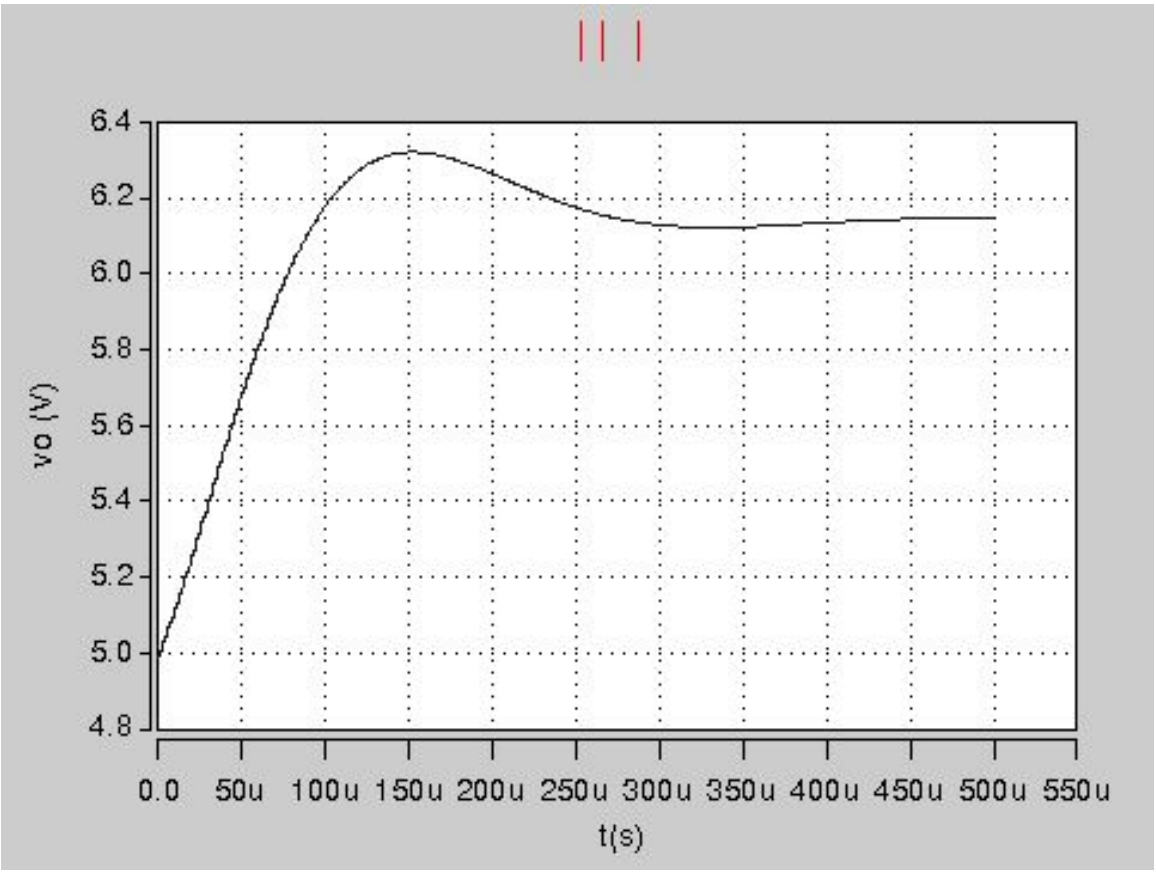

Figure 5.12: Step response of T_p as obtained on SABER.

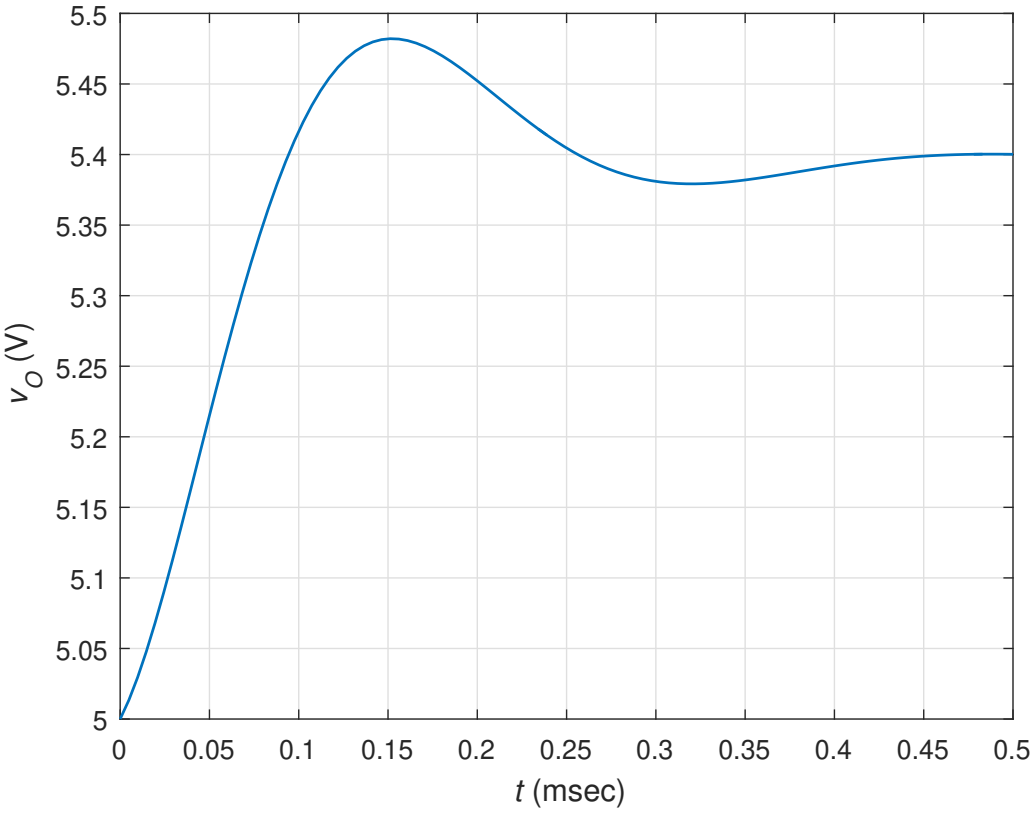

Figure 5.13: Step response of M_v as obtained on MATLAB.

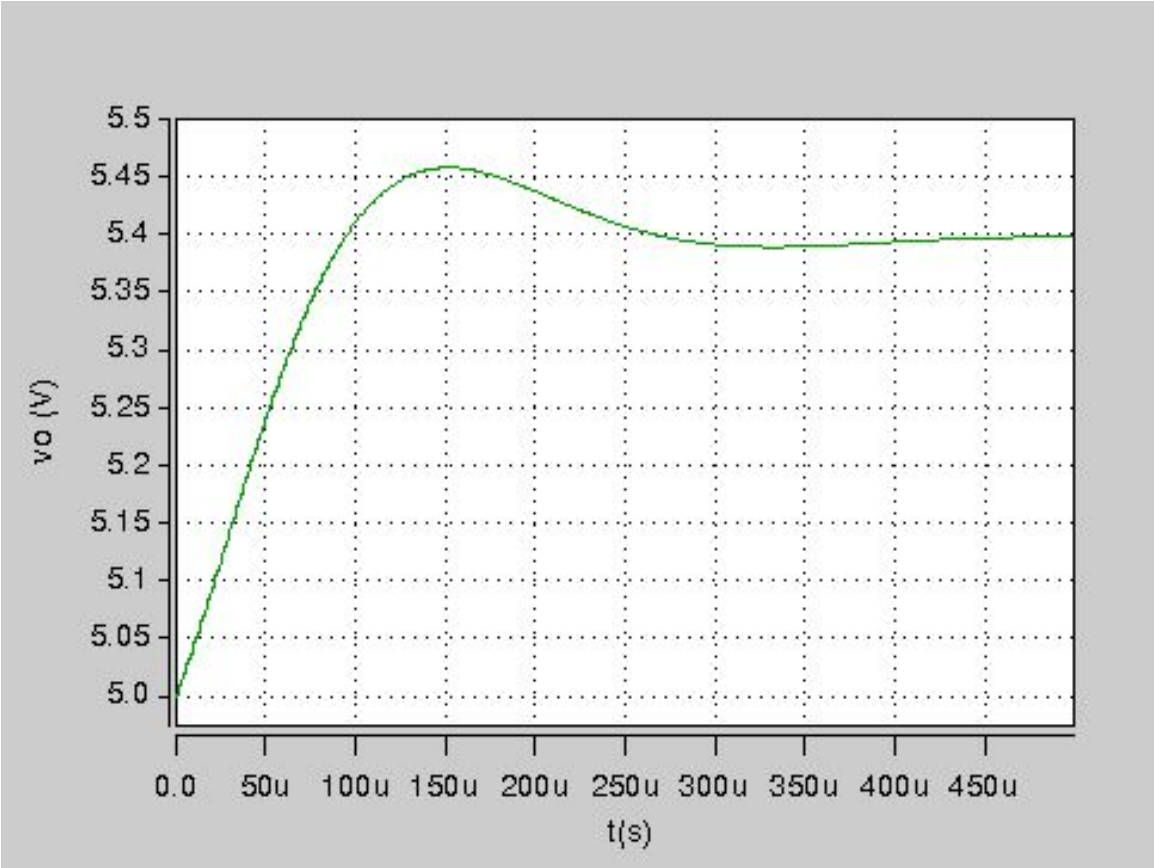

Figure 5.14: Step response of M_v as obtained on SABER.

5.5 Experimental Validation of Tapped-Inductor Buck DC-DC Converter in Frequency-Domain.

A gain-phase analyzer by HP, will be used to validate the magnitude and phase plots as obtained from theoretical calculations and SABER circuit simulators. A 4194A Impedance/gain-phase analyzer by HP works for a frequency range of 10 Hz - 100 MHz. This is a wide enough bandwidth to accommodate the converters switching frequency and should be capable enough to validate the responses. A block diagram representing the gain-phase analyzer can be seen in Fig. 5.15. The analyzer produces an ac output which varies its frequency over time. It also accepts two input signals called a test input and reference input. To test a specific input-to-output transfer function, the output from the system analyzer is first induced into the test equipment to produce perturbation in the test setup. The reference input from the analyzer can be connected to the input part of the transfer function the test input can be connected to the output part of the transfer function. The analyzer calculated the gain and phase difference between the test and reference inputs and provides the information on its display over a wide frequency range. The obtained data can then be noted and plotted by using MATLAB. The drawback of using this gain-phase analyzer is that the input does not accept any signal higher than ±5 V DC. But for the small signal operation the dc can be blocked out by adding bulk capacitors at the input of the gain-phase analyzer. A 47 μF/650VDC, with a flat gain over the required frequency range is used to block any DC voltage trying to enter the gain-phase analyzer. For testing the equipment simulation specifications with $V_I = 12$ V, $f_s = 100$ kHz, $P_O = 2.5$ W, and $V_O = 5$ V was selected. The tapped-inductor turns ratio is $n = 2$. To obtained the required output a coupled inductor DRQ125-330-R by with magnetizing inductance 35 μH was used. The selected MOSFET and diode were IRF540 and MBR10100 by Vishay semiconductors. The complete PCB circuit

can be seen in Fig. 5.16.

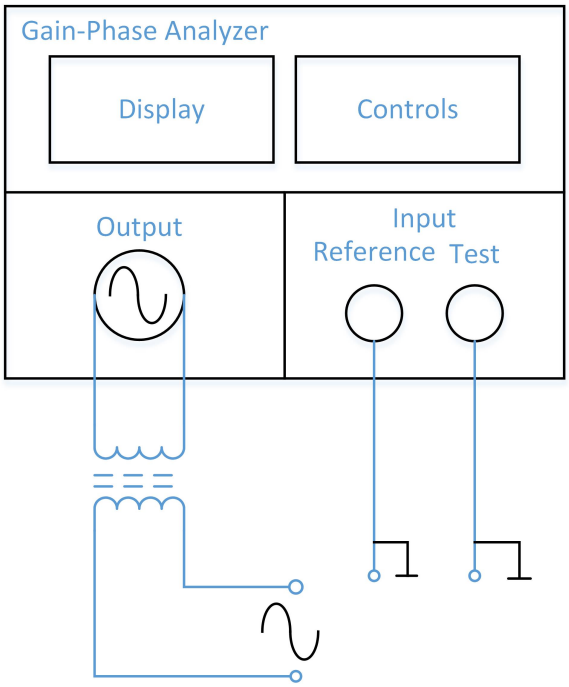

Figure 5.15: Block diagram representing a system analyzer.

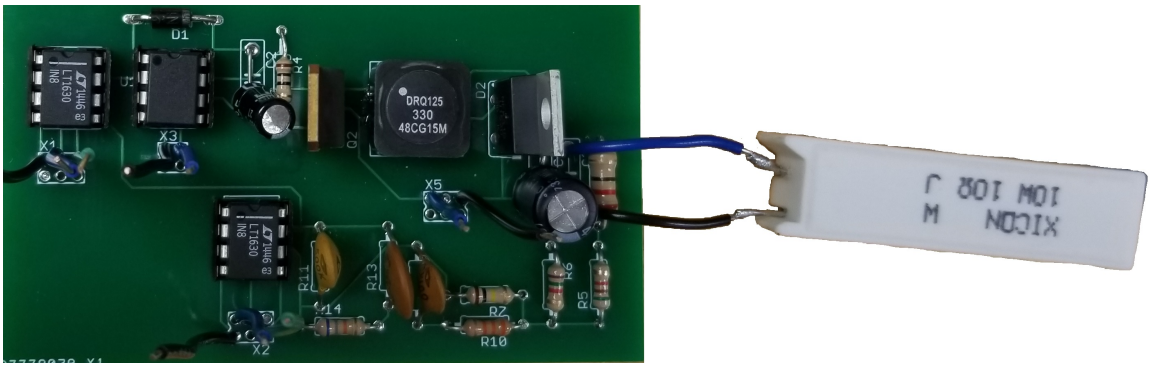

Figure 5.16: Final Product.

5.5.1 Frequency Response of T_p using 4194A Impedance/gain-phase analyzer

The bench set up required to verify the derived transfer function T_p from Section 5.2 can be seen in Fig. 5.17. An LT1630 high bandwidth op-amp is used to produce pulses for MOSFET switching. It also helps superimpose a sinusoidal voltage, with

varying frequency over the control voltage. The triangular voltage with an amplitude V_{Tm} is used to produce the pulse voltage. More on the working of the PWM will be discussed in Section 6.2. The gain offered by the PWM is $T_m = 0.2\ V/V = -14\ dB$. Followed by the PWM output is IR2117 high bandwidth high side MOSFET driver, with bootstap capacitor and diode. The output of the gain-phase analyzer is added in series with the PWM control voltage by using a current transducer with 0.001 gain. The secondary has 50 turns. The total gained offered by the transducer is 0.05 V/V or -26 dB. The reference input is connected in parallel to the gain-phase analyzer output. The gain-phase test input is connected to the output of the converter. The total transducer and PWM gain of -40 dB is added to the obtained magnitude and phase plot on gain-phase analyzer. This gives the magnitude and phase plot of the transfer function T_p. The obtained magnitude and phase plots and its comparison with the theoretical results can be seen in Figs. 5.18 and 5.19 respectively. The obtained responses from the gain-phase analyzer is in good agreement with theoretical responses.

5.5.2 Frequency Response of M_v using 4194A Impedance/gain-phase analyzer

The bench set up required to verify the derived transfer function M_v from Section 5.3 can be seen in Fig. 5.20. The output of the gain-phase analyzer is added in series with the input voltage for the converter by using a current transducer with 0.001 gain. The secondary has 50 turns. The total gained offered by the transducer is 0.05 V/V or -26 dB. The reference input is connected in parallel to the gain-phase analyzer output. The gain-phase test input is connected to the output of the converter. The transducer gain is added to the obtained magnitude and phase plot on gain-phase analyzer. This gives the magnitude and phase plot of the transfer function M_v. The obtained magnitude and phase plots and its comparison with the theoretical results

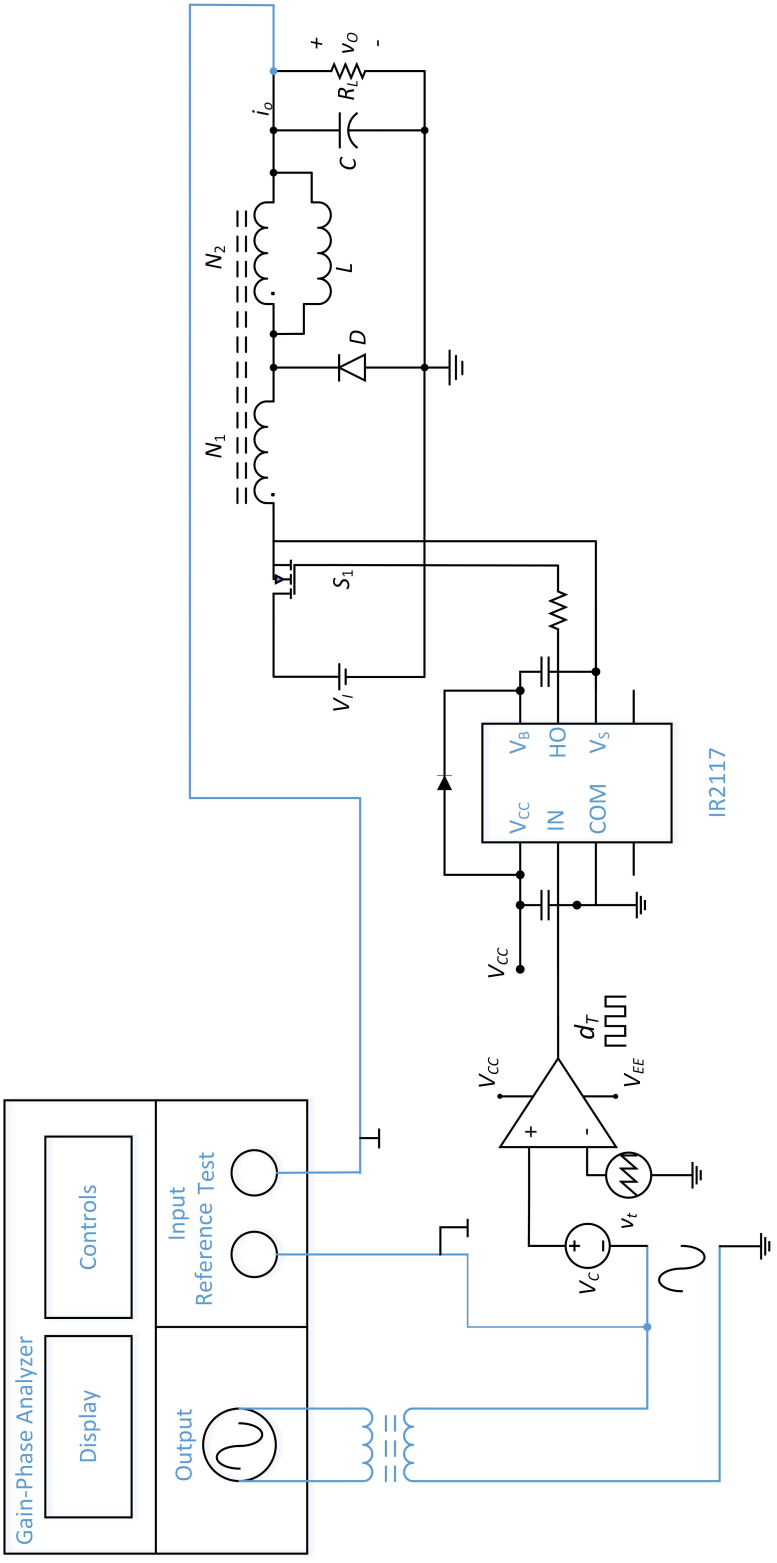

Figure 5.17: Bench setup to obtain control-to-output voltage transfer function.

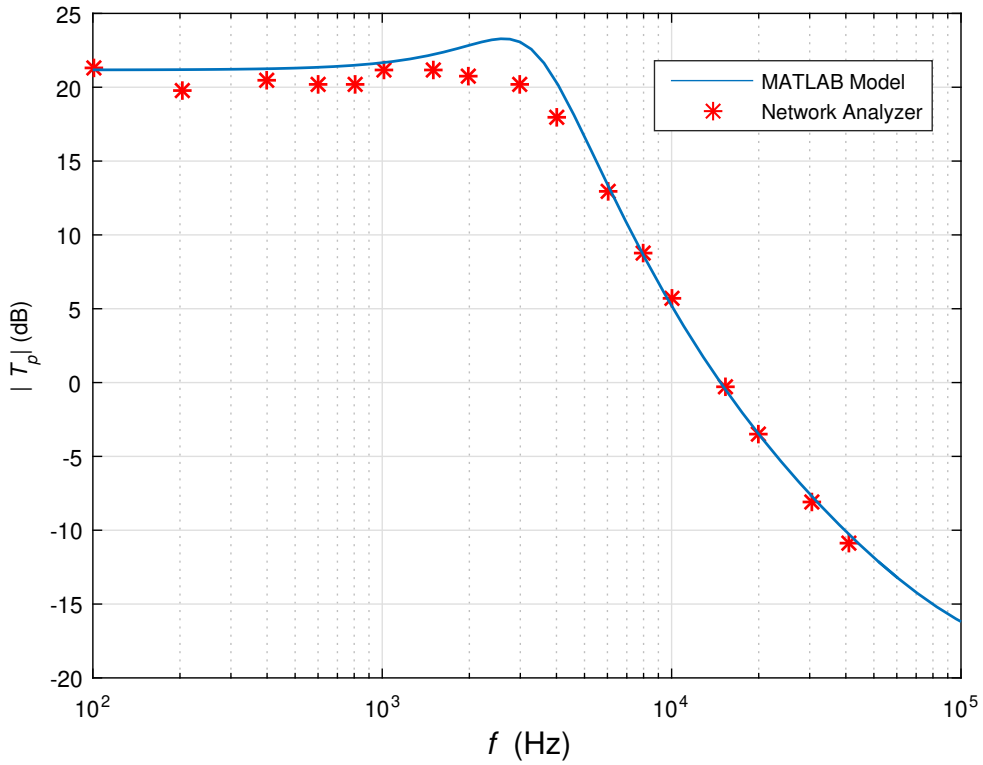

Figure 5.18: Magnitude plot comparing the theoretical and practical results of transfer function T_p.

can be seen in Figs. 5.21 and 5.22 respectively. The obtained responses from the gain-phase analyzer is in good agreement with theoretical responses.

5.5.3 Response of Output Voltage for a Step Change in Duty Cycle

The step change in duty cycle is produced by changing the duty cycle from the function generator by 10%. The obtained step response can be seen in Fig. 5.23. The measured values of overshoot, rise time and settling time are 2.7 %, 4.8 msec, 4 msec respectively.

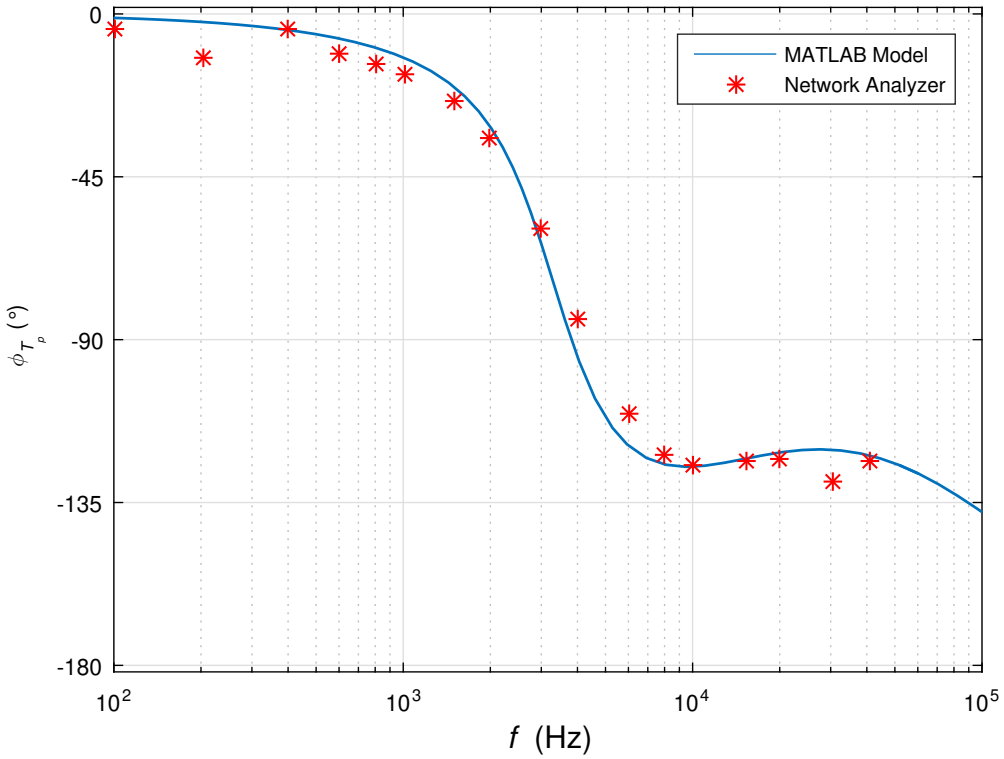

Figure 5.19: Phase plot comparing the theoretical and practical results of transfer function T_p.

5.5.4 Response of Output Voltage for a Step Change in Input Voltage

The step change in duty cycle is produced by changing the supply voltage by 1 V. The obtained step response can be seen in Fig. 5.24. The measured values of overshoot, rise time and settling time are 0.7 %, 2 msec, 2 msec respectively.

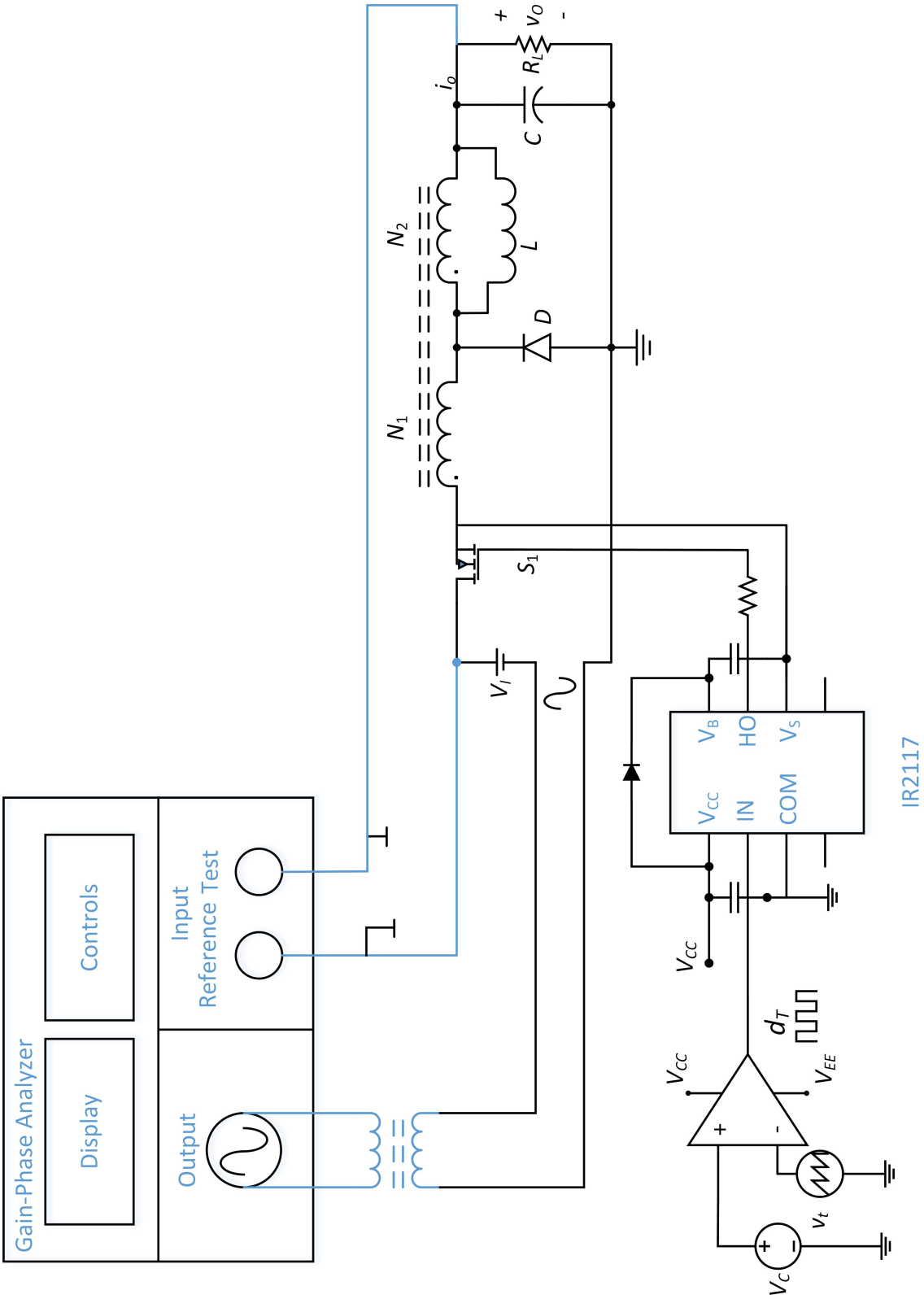

Figure 5.20: Bench setup to obtain input-to-output voltage transfer function.

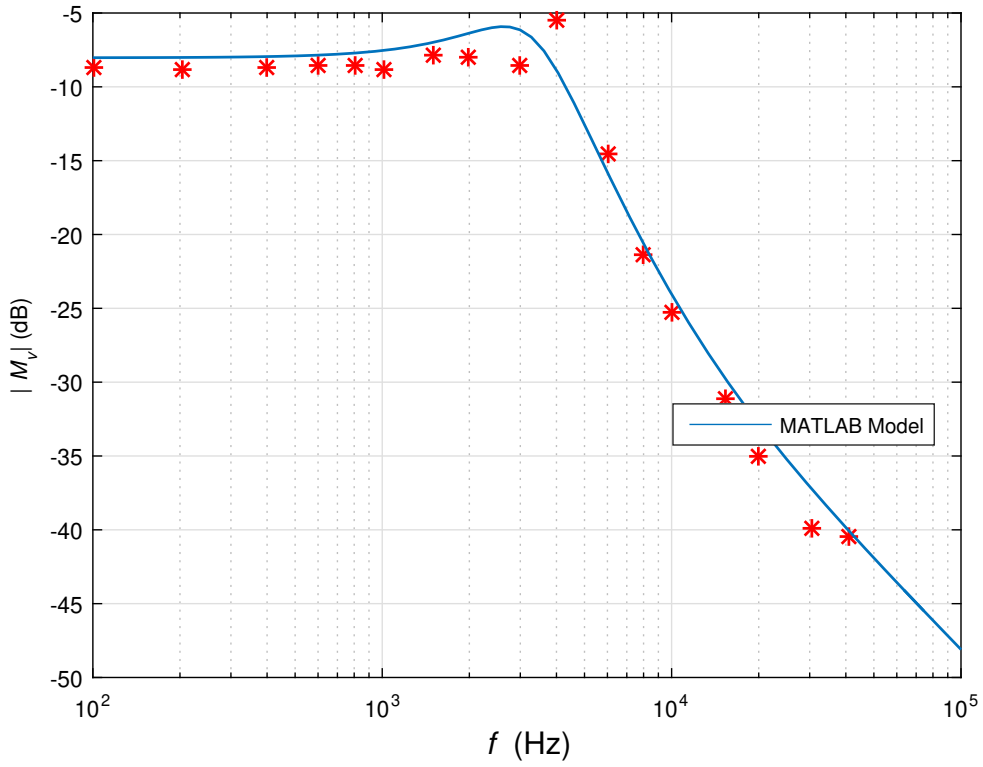

Figure 5.21: Magnitude plot comparing the theoretical and practical results of transfer function M_v.

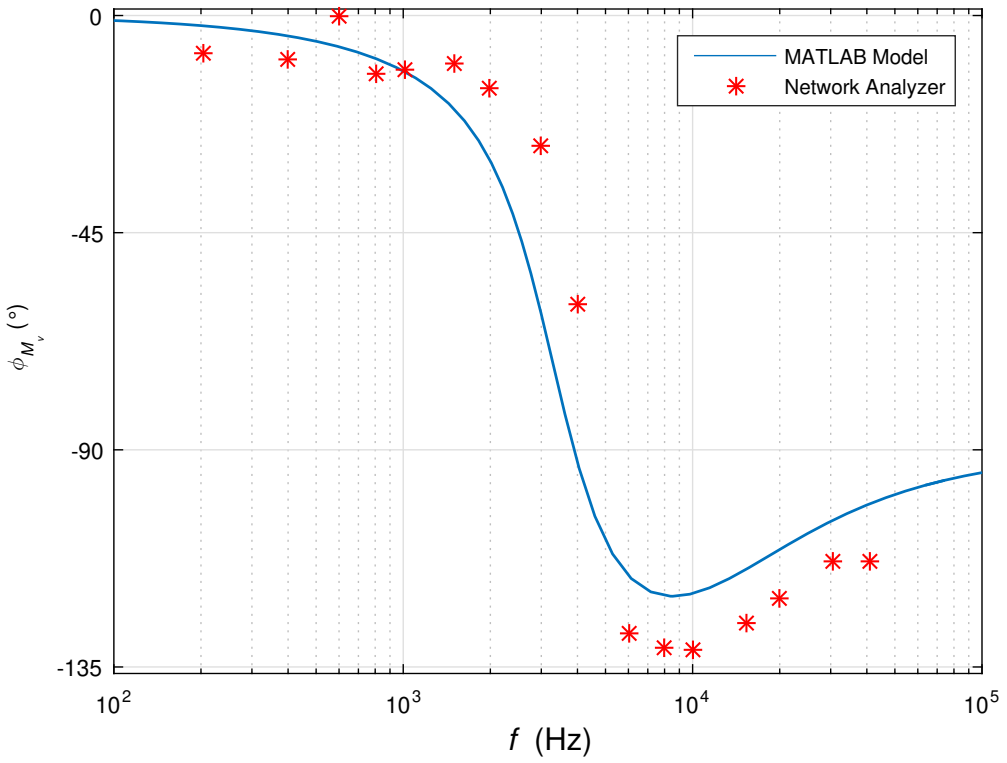

Figure 5.22: Phase plot comparing the theoretical and practical results of transfer function M_v.

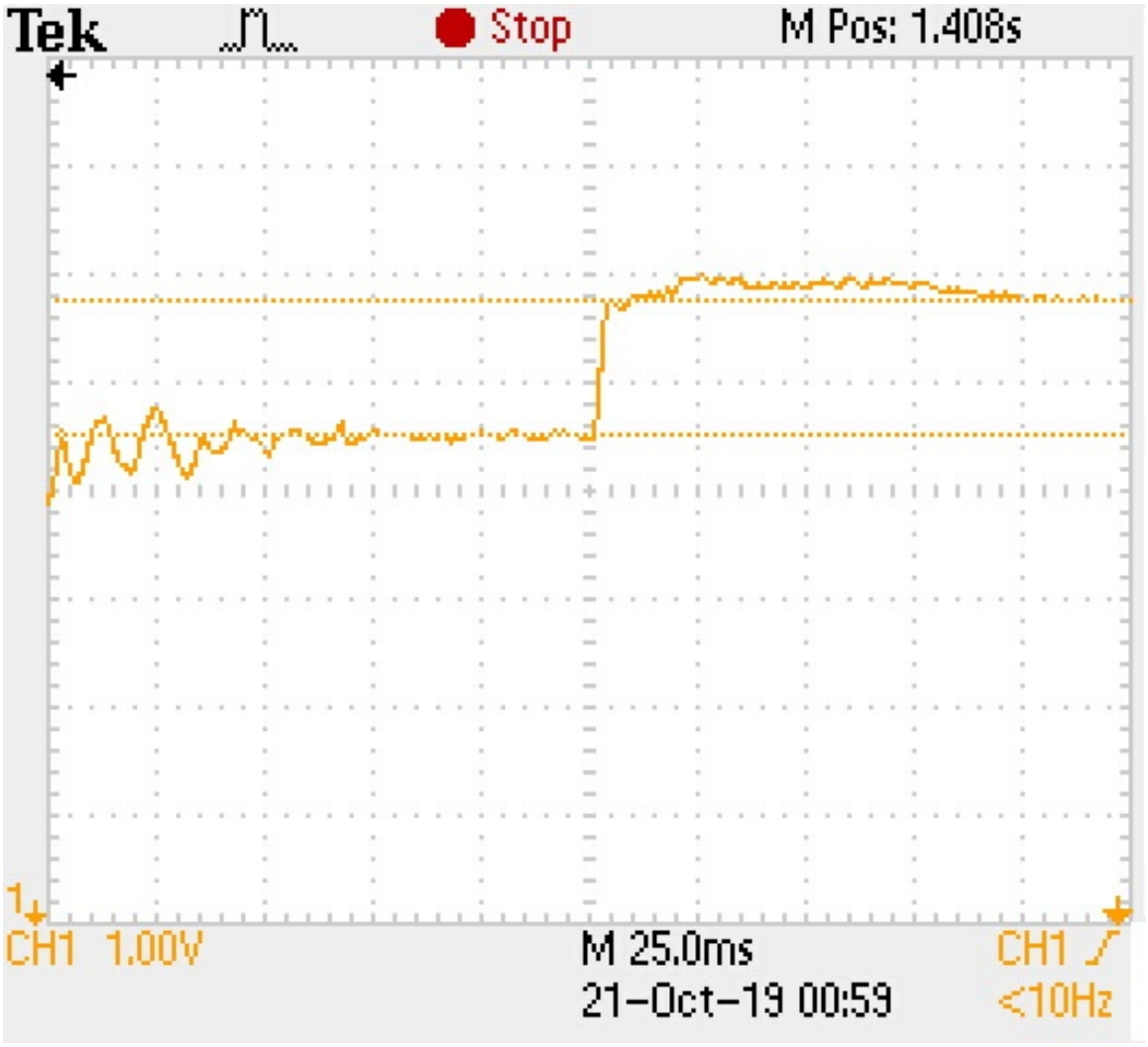

Figure 5.23: Step response of T_p as obtained on the test bench.

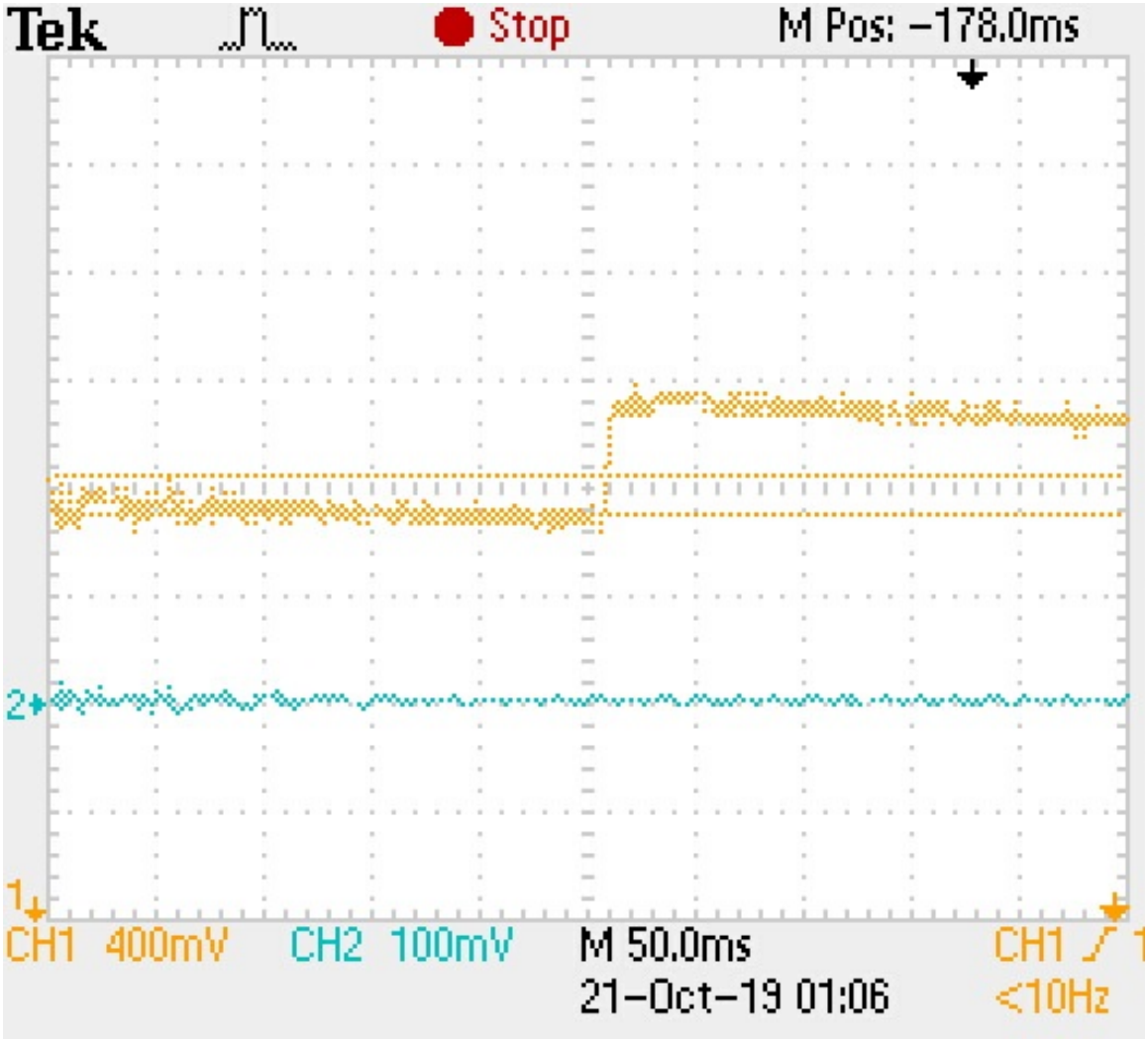

Figure 5.24: Step response of T_p as obtained on the test bench.

6 Voltage-Mode Control

A voltage-mode controller for the tapped-inductor buck dc-dc converter is designed in this section. The required transfer functions are taken as reference from the previous section. Loop gains for an uncompensated system is used to design a controller to control this specific converter. The stable system will required a phase margin of 60° and a gain margin of 15 db. A type III controller namely, an integral-double-lead controller as referred in [1] is used in this instant. Frequency and time-domain response representing a stable closed loop response is presented analytically using MATLAB and verified through SABER circuit simulations.

6.1 Circuit Diagram of the Power Stage with Voltage-Mode Control

A voltage control of a tapped-buck dc-dc converter can be seen in Fig. 6.1. Here the output voltage is being sensed by the sense feedback resistance and is compared to a reference voltage V_R. The control signal produced by the controller is then sent to a pulse width modulator to produce pulses. These pulses are further used to drive the MOSFET and therefore, help maintain the output voltage. As seen in previous chapter the required transfer functions involved in representing a buck dc-dc converter are T_p, M_v, Z_o. In the implemented control scheme the output is being sensed to create required duty cycle, which further controls the converter output. Therefore, the closed-loop small-signal low-frequency model of a tapped-buck dc-dc converter can be seen in Fig. 6.2, where T_c is the controller transfer function, T_m is the PWM transfer function, β is the transfer function of the feedback network, as seen in Fig. 6.1 the value of the feedback resistor is decided by the feedback resistance given by

$$\beta = \frac{R_B}{R_A + R_B}, \tag{6.1}$$

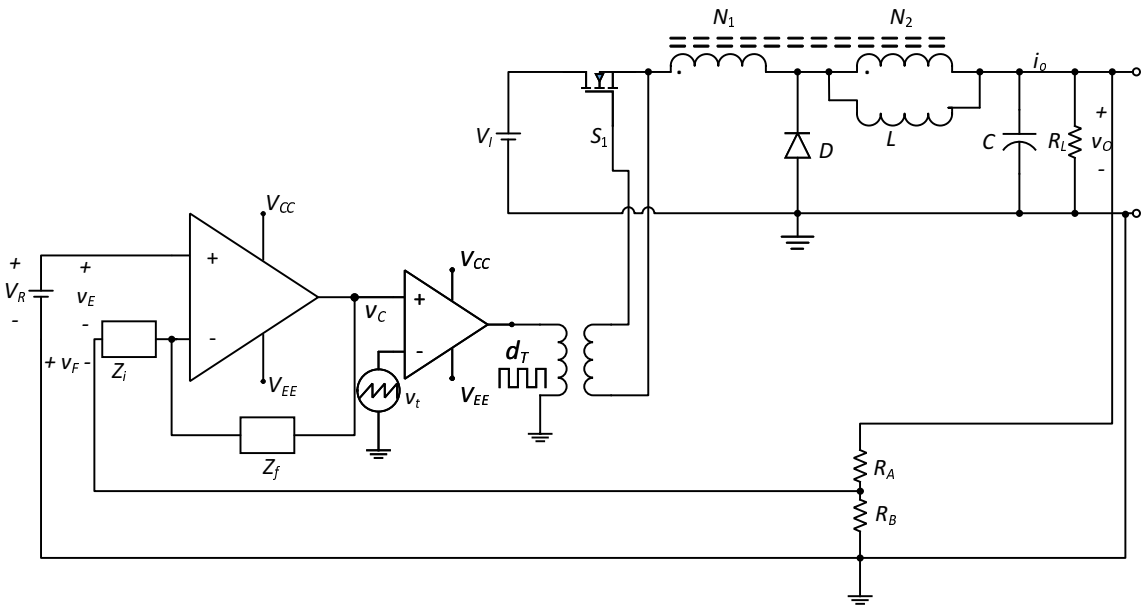

Figure 6.1: Circuit of a closed-loop PWM tapped-inductor buck converter.

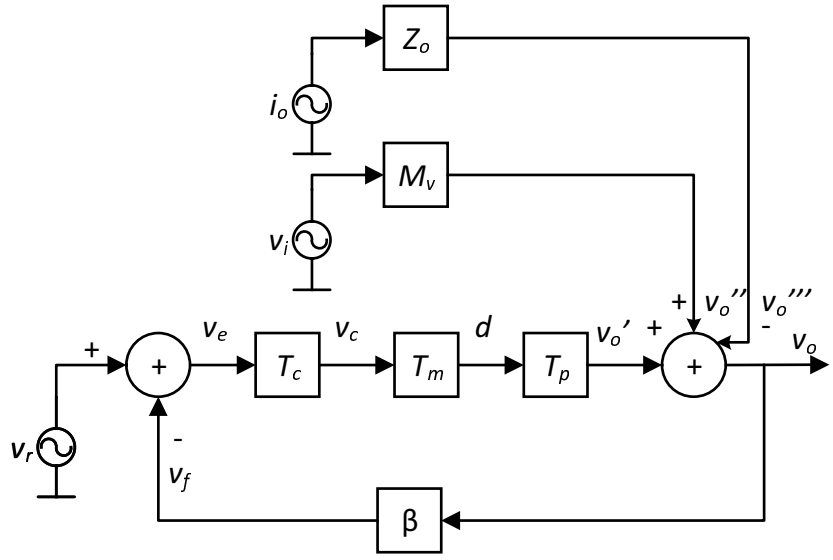

Figure 6.2: Block diagram of a closed-loop PWM tapped-inductor buck converter.

v_f is the ac component of the feedback voltage, v_c is the ac component of the control voltage, v_r is the ac component of the reference voltage. The voltage gain of the forward path is given by

$$A = \frac{v_o}{v_e} = T_c T_m T_p, \tag{6.2}$$

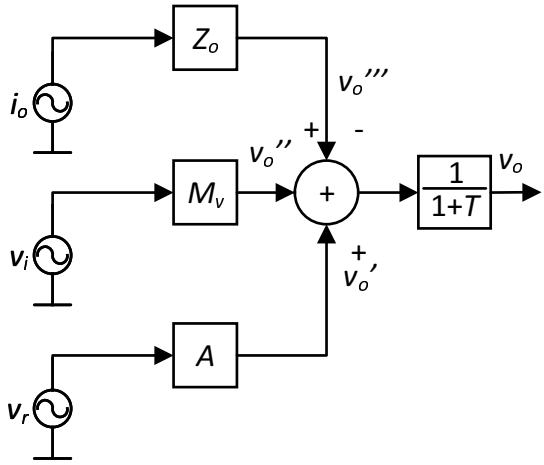

Figure 6.3: Simplified block diagram of a closed-loop PWM tapped-inductor buck converter.

the loop gain is given by

$$T = \frac{v_o}{v_f} = \beta A = \beta T_c T_m T_p. \tag{6.3}$$

The ac component of the output voltage is given by

$$v_o = \frac{A}{1+T} v_r + \frac{M_v}{1+T} v_i - \frac{Z_o}{1+T} i_o = T_{cl} v_r + M_{vcl} v_i - Z_{ocl} i_o, \tag{6.4}$$

where T_{cl}, M_{vcl} and Z_{ocl} are the closed-loop transfer functions of T_p, M_v and Z_o respectively. The simplified block diagram can be seen in Fig. 6.3. Henceforth each and every block as seen in Fig. 6.2 will be derived and explained in detail starting with the PWM, followed by the error amplifier and finally the derivation and implementation of the selected integral-double-lead controller.

6.2 Pulse-Width Modulator

A pulse-width modulator is used to digitize the control signal and use this digitized signal to drive the converter MOSFET. A PWM consists of an op-amp with its non-inverting terminal connected to control signal v_c and the inverting terminal connected to a ramp voltage v_t. Any change in the control signal due to any disturbance in the system causes the control signal to increase $V_C + v_c$, which intern changes the duty

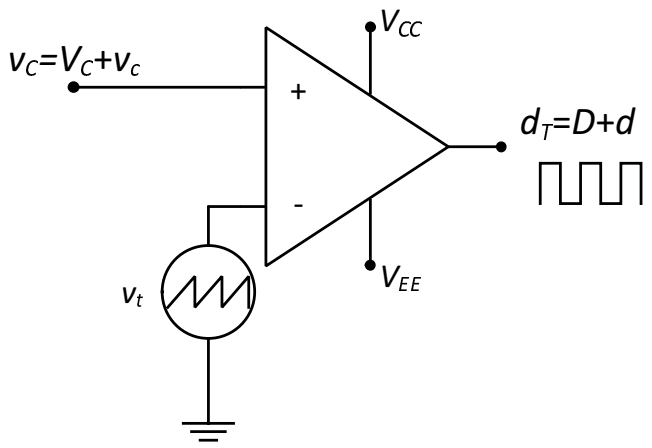

Figure 6.4: Circuit of an op-amp as a comparator used for PWM.

cycle $D + d$ of the op-amp's digitized output. An op-amp used as a PWM can be seen in Fig. 6.4. The ramp input and the pulse output can be seen in Fig. 6.5. The slope of the ramp input is given by

$$M = \tan\gamma = \frac{v_c}{dT_s} = \frac{V_{Tm}}{T_s}, \tag{6.5}$$

Rearranging (6.5) gives the control voltage-to-duty cycle transfer function.

$$T_m = \frac{d}{v_c} = \frac{1}{V_{Tm}} = \frac{1}{MT_s} = \frac{f_s}{M}. \tag{6.6}$$

6.3 Loop Gain without Controller Compensation

The block diagram of the closed-loop system can be seen in Fig. 6.2. The transfer functions required to obtain the loop gain have been derived in (5.9) and (6.6). The transfer function of the feedback is β. The loop gain is

$$T_k = \frac{v_f}{v_c} = T_m T_p \beta. \tag{6.7}$$

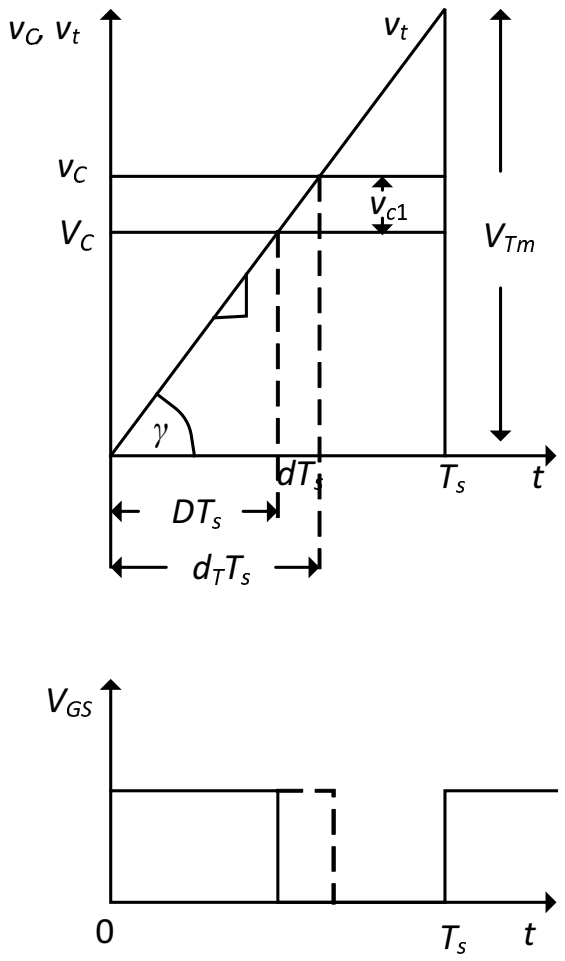

Figure 6.5: Ramp signal for pulse width modulator.

Substituting (5.9) and (6.6) into (6.7), we get

$$
\begin{aligned}
T_k(s) &= \frac{v_f(s)}{v_c(s)} \\
&= -\frac{\left(\dfrac{\beta k_2(n-1)R_L r_C}{V_{Tm}\left[1+k_1(n-1)\right](R_L+r_C)}\right)\left(s-\dfrac{k_3}{Lk_2(n-1)}\right)\left(s+\dfrac{1}{r_C C}\right)}{s^2+\dfrac{L(1+k_1(n-1))+(R_L r+rr_C+R_L r_C)C}{LC[1+k_1(n-1)](R_L+r_C)}s+\dfrac{r+R_L}{LC[1+k_1(n-1)](R_L+r_C)}} \\
&= T_{kx}\frac{(s+\omega_{zn})(s-\omega_{zp})}{s^2+2\xi\omega_0 s+\omega_0^2} = T_{ko}\frac{\left(1+\dfrac{s}{\omega_{zn}}\right)\left(1-\dfrac{s}{\omega_{zp}}\right)}{\left(\dfrac{s}{\omega_0}\right)^2+\dfrac{2\xi s}{\omega_0}+1},
\end{aligned}
\tag{6.8}
$$

where the dc gain T_{ko} is

$$T_{ko} = T_k(0) = -\frac{\beta R_L k_3}{V_{Tm}\,(R_L + r)} = 0.23 = -12.77 \text{ db}, \tag{6.9}$$

6.4 Loop Gain Design Example

For the specification used in designing the tapped-inductor buck dc-dc converter the closed-loop can be implemented by sensing the output voltage using a voltage divider, while making sure the transfer function of the feedback is $\beta = 0.1$.

Selecting R_A for the feedback resistance to be 5 kΩ. The value of R_B can be obtained from (6.1)

$$R_B = \frac{\beta}{1-\beta} R_A = 555.55\ \Omega. \tag{6.10}$$

The amplitude of the triangular wave used for the PWM can be selected to be 5 V. The control to duty cycle transfer function is given by

$$T_m = \frac{1}{V_{Tm}} = \frac{1}{5}. \tag{6.11}$$

From (6.9) The dc gain of T_k is

$$T_k(0) = -\frac{\beta R_L k_3}{V_{Tm}(R_L + r)} = -0.23 \tag{6.12}$$

which in decibel scale is equal to -12.77 db. Using (6.7) and (5.9). The magnitude and phase plots can be seen in Figs. 6.6 and 6.7 respectively.

6.5 Integral-double-lead Controller

As seen in Fig. 6.6, the magnitude of T_k is below zero for entire frequency range. This can be avoided by adding compensator network into the closed loop to maintain the magnitude and phase margin of the loop gain. This helps obtained a controlled and faster response. This controller adds in a pole at origin two pole-zero pairs into the closed loop. This helps reduces the phase difference at the crossover frequency and

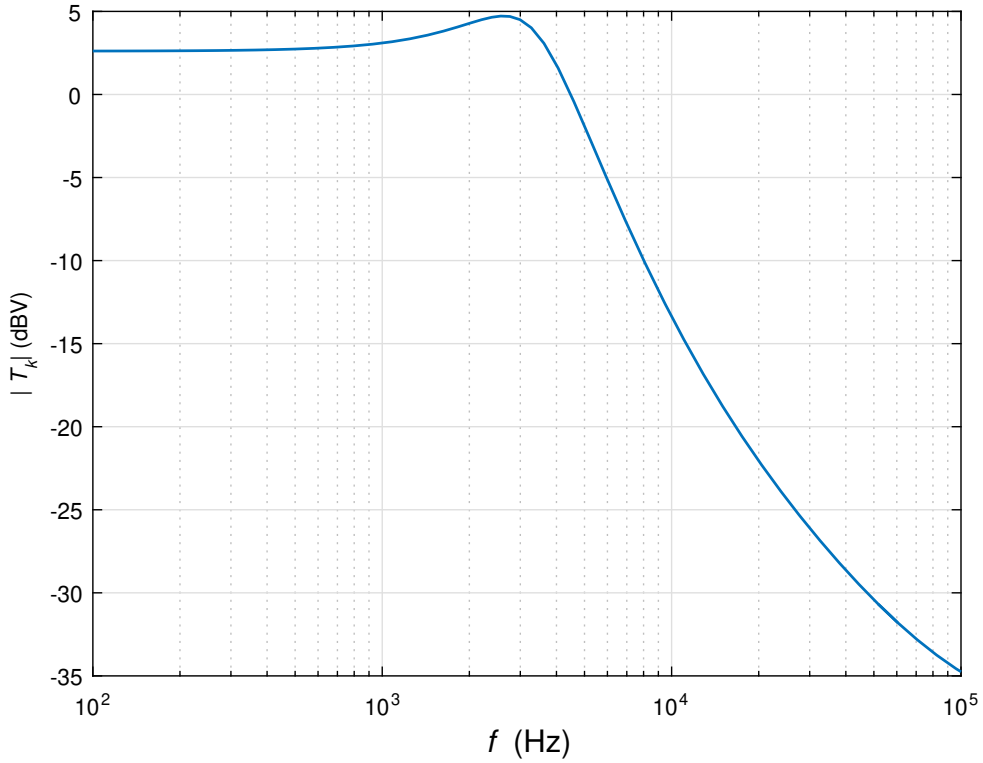

Figure 6.6: Frequency effecting the magnitude of the tapped-inductor buck converter's loop gain without controller compensation.

this help obtain higher phase margins. An circuit of a integral-double-lead controller is connected as shown in Fig. 6.8.The impedance of the feedback network is given by

$$Z_f = \frac{\frac{1}{sC_2}\left(R_2 + \frac{1}{sC_1}\right)}{R_2 + \frac{1}{sC_1} + \frac{1}{sC_2}} = \frac{s + \frac{1}{R_2C_1}}{sC_2\left(s + \frac{C_1 + C_2}{R_2C_1C_2}\right)}, \tag{6.13}$$

The impedance in the forward path of the controller is given by

$$Z_i = h_{11} + \frac{R_1\left(R_3 + \frac{1}{sC_3}\right)}{R_1 + R_3 + \frac{1}{sC_3}} = \left(h_{11} + \frac{R_1R_3}{R_1 + R_3}\right)\frac{s + \frac{R_1 + h_{11}}{C_3\left[R_3\left(R_1 + h_{11}\right) + h_{11}R_1\right]}}{s + \frac{1}{C_3\left(R_1 + R_3\right)}}, \tag{6.14}$$

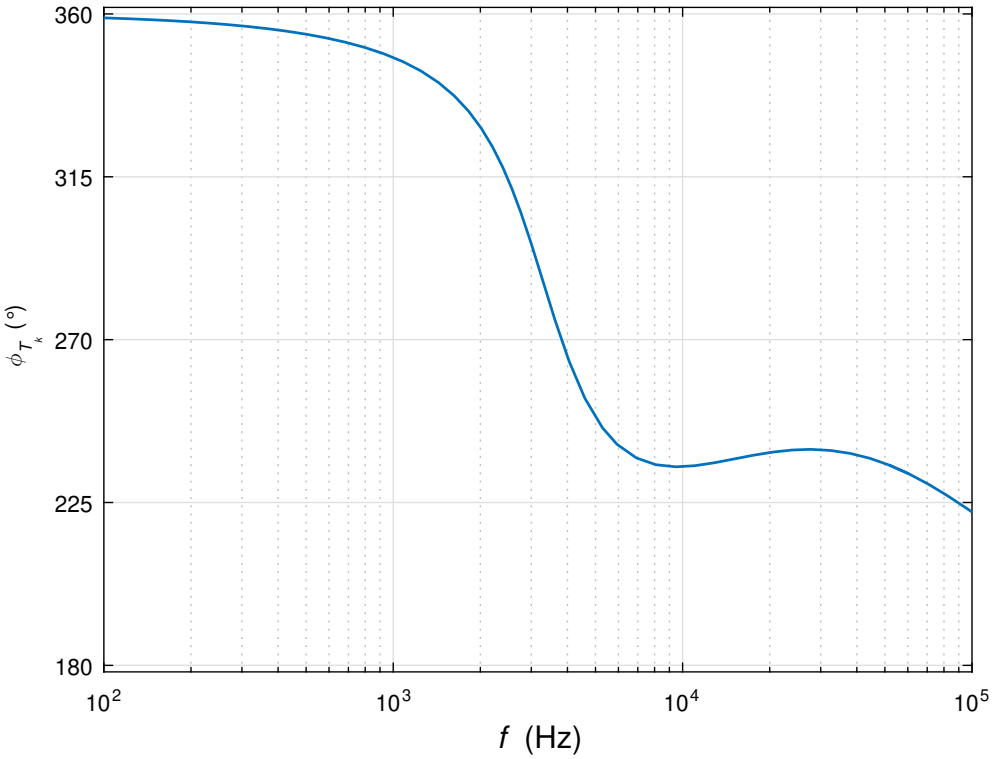

Figure 6.7: Frequency effecting the phase of the tapped-inductor buck converter's loop gain without controller compensation.

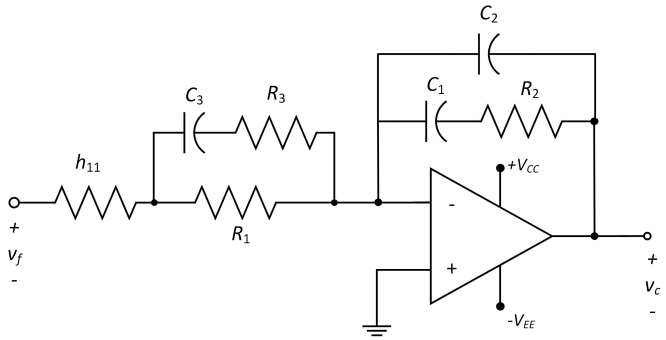

Figure 6.8: Circuit diagram of a integral-double-lead controller with two pole-zero pairs.

where

$$h_{11} = \frac{R_A R_B}{R_A + R_B}. \tag{6.15}$$

The controller gain is given by

$$A_v(s) = \frac{v_c(s)}{v_e(s)} = -\frac{Z_f}{Z_i} = -\frac{R_1 + R_3}{C_2\left[R_1R_3 + h_{11}\left(R_1 + R_3\right)\right]} \times \frac{\left(s + \dfrac{1}{R_2C_1}\right)\left[s + \dfrac{1}{C_3\left(R_1 + R_3\right)}\right]}{s\left(s + \dfrac{C_1 + C_2}{R_2C_1C_2}\right)\left\{s + \dfrac{R_1 + h_{11}}{C_3\left[R_1R_3 + h_{11}\left(R_1 + R_3\right)\right]}\right\}}. \tag{6.16}$$

The control voltage transfer function is given by

$$T_c(s) = -\frac{v_c(s)}{v_e(s)} = -A_v(s) = \frac{B(s + \omega_{zc1})(s + \omega_{zc2})}{s(s + \omega_{pc1})(\omega_{pc2})}, \tag{6.17}$$

where

$$B = \frac{R_1 + R_3}{C_2\left[R_1R_3 + h_{11}(R_1 + R_3)\right]}, \tag{6.18}$$

$$\omega_{zc1} = \frac{1}{R_2C_1}, \tag{6.19}$$

$$\omega_{zc2} = \frac{1}{C_3(R_1 + R_3)}, \tag{6.20}$$

$$\omega_{pc1} = \frac{C_1 + C_2}{R_2C_1C_2} = \omega_{zc1}\left(\frac{C_1}{C_2} + 1\right), \tag{6.21}$$

and

$$\omega_{pc2} = \frac{R_1 + h_{11}}{C_3\left[R_1R_3 + h_{11}\left(R_1 + R_3\right)\right]} = \omega_{zc1}\left(\frac{C_1}{C_2} + 1\right). \tag{6.22}$$

Assuming the two poles are places at the same frequency and two zeros are places at the frequency.

$$\omega_{zc1} = \omega_{zc2} = \omega_{zc} \text{ and } \omega_{pc1} = \omega_{pc2} = \omega_{pc}. \tag{6.23}$$

The poles and zero gains ratio is now given by

$$K = \frac{\omega_{pc1}}{\omega_{zc1}} = \frac{\omega_{pc2}}{\omega_{zc2}} = \frac{\omega_{pc}}{\omega_{zc}} = \frac{C_1}{C_2} + 1 = \frac{\left(R_1 + h_{11}\right)\left(R_1 + R_3\right)}{R_1R_3 + h_{11}\left(R_1 + R_3\right)}. \tag{6.24}$$

Hence the controller transfer function is given by

$$T_c(s) = \frac{v_c(s)}{v_e(s)} = \frac{B\left(s + \omega_{zc}\right)^2}{s\left(s + \omega_{pc}\right)^2} = \frac{B\omega_{zc}^2\left(1 + \dfrac{s}{\omega_{zc}}\right)^2}{\omega_{pc}^2 s\left(1 + \dfrac{s}{\omega_{pc}}\right)^2} = \frac{B\left(1 + \dfrac{s}{\omega_{zc}}\right)^2}{K^2 s\left(1 + \dfrac{s}{\omega_{pc}}\right)^2} \tag{6.25}$$

6.6 Loop Gain

Knowing the controller compensation the loop gain of the converter is given by

$$\begin{aligned} T(s) &= \left.\frac{v_f(s)}{v_e(s)}\right|_{v_i=i_o=0} = T_c(s)T_{mp}(s)\beta \\ &= \frac{T_x\left(s+\omega_{zc}\right)^2\left(s+\omega_{zn}\right)\left(s-\omega_{zp}\right)}{s(s+\omega_{pc})^2(s^2+2\xi\omega_0 s+\omega_0^2)}, \end{aligned} \tag{6.26}$$

where

$$T_x = -\frac{\beta B V_O r_C}{V_{Tm}(1-D)(R_L+r_C)}. \tag{6.27}$$

6.7 Simulation Validation of Loop-Gain

6.7.1 Frequency Response of T_c using MATLAB and SABER Circuit Simulator

The selected controller can be designed to compensated the tapped-inductor buck converter and provide good gain and phase margins are the cross over frequencies. The cross over frequency for the selected system can be selected to be at $f_c = 3$ kHz. The task of the controller is to compensate the system gain at the crossover frequency.

$$|T_c(f_c)T_k(f_c)| = 1. \tag{6.28}$$

This can be simplified to obtain

$$|T_c(f_c)| = \frac{1}{T_k(f_c)} = \frac{1}{\beta|T_{mp}(f_c)|} = 0.8143 = -1.7843 \text{ db}. \tag{6.29}$$

The phase at the loop gain without controller compensation at the crossover frequency is given by

$$\phi_{T_k}(f_c) = -180^\circ + \arctan\left(\frac{f_c}{f_{zn}}\right) - \arctan\left(\frac{f_c}{f_{zp}}\right) - \arctan\left[\frac{\left(\frac{2\xi f_c}{f_0}\right)}{1-\left(\frac{f_c}{f_0}\right)^2}\right] = -94.74^\circ. \tag{6.30}$$

Since the systems is to be designed to maintain a phase margin of 60°, the required phase boost is given by

$$\phi_m = PM - \phi_{T_k}(f_c) - 90 = 64.74^\circ, \tag{6.31}$$

and the K factor is

$$K = \tan^2\left(\frac{\phi_m}{4} + 45^\circ\right) = 3.30. \tag{6.32}$$

From equation 6.18 and 6.29

$$B = \omega_c K|T_c(f_c)| = 2\pi \times 3000 \times 3.30 \times 1.7843 = 7.2 \times 10^4 (\text{rad/s}). \tag{6.33}$$

Assuming the resistance in the forward path to be $R_1 = 100$ kΩ. From 6.32, one can obtain

$$R_3 = \frac{R_1 \left[R_1 - h_{11} \left(K - 1\right)\right]}{\left(K - 1\right) \left(R_1 + h_{11}\right)} = 39.89 \text{ k}\Omega. \tag{6.34}$$

Pick $R_3 = 3.3$ kΩ.

$$C_2 = \frac{\beta |T_{mp}(f_c)|}{\omega_c \left(R_1 + h_{11}\right)} = 474.63 \text{ pF}. \tag{6.35}$$

Pick $C_2 = 500$ pF.

$$C_1 = C_2(K - 1) = 1.15 \text{ nF}. \tag{6.36}$$

Pick C_1 =1.58 nF

$$R_2 = \frac{\sqrt{K}}{\omega_c C_1} = 45.78 \text{ k}\Omega. \tag{6.37}$$

Pick $R_2 = 68$ kΩ.

$$C_3 = \frac{R_1 + h_{11}}{\omega_c \sqrt{K} \left[R_1 R_3 + h_{11} \left(R_1 + R_3\right)\right]} = 610.29 \text{ pF}. \tag{6.38}$$

Pick $C_3 = 750$ pF. The magnitude and phase plot of the designed controller can be seen in Figs. 6.9 and 6.10 respectively. The magnitude and phase plot of the designed controller on SABER circuit simulator can be seen in Figs. 6.11 and 6.12 respectively.

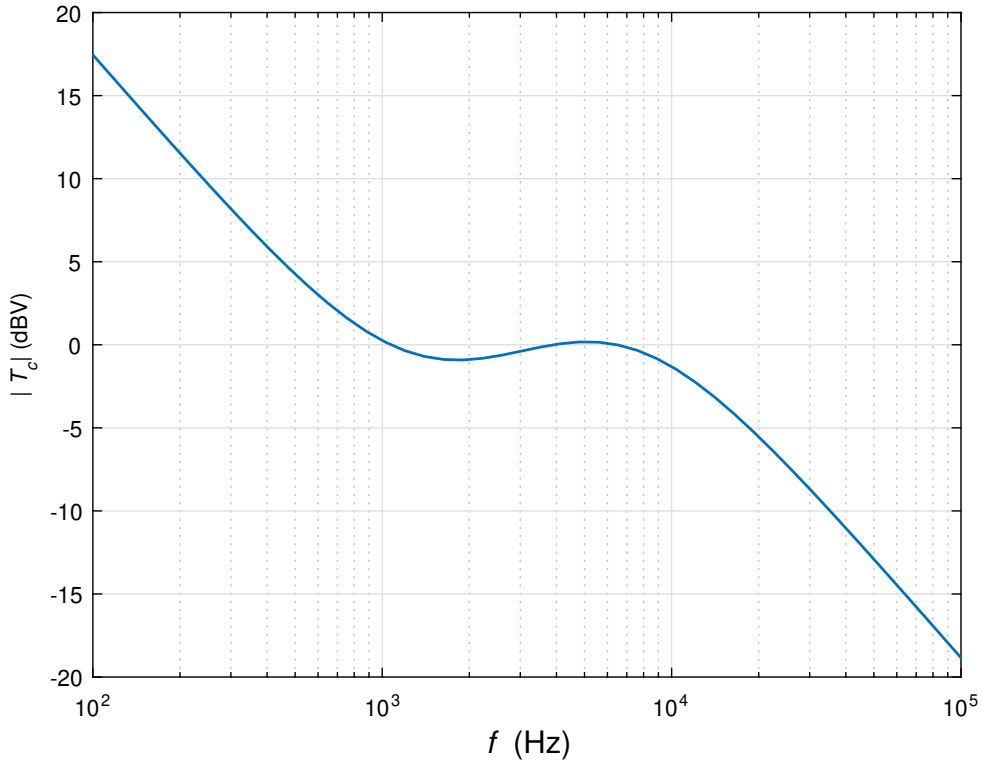

Figure 6.9: Magnitude plot of the designed controller compensation.

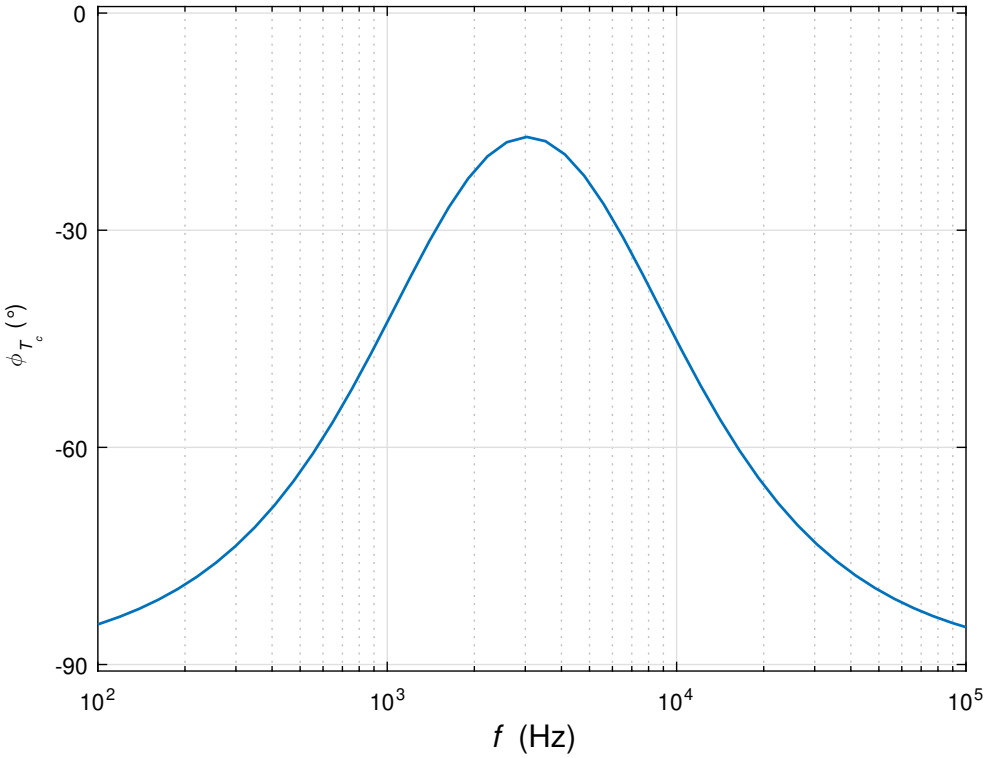

Figure 6.10: Phase plot of the designed controller compensation.

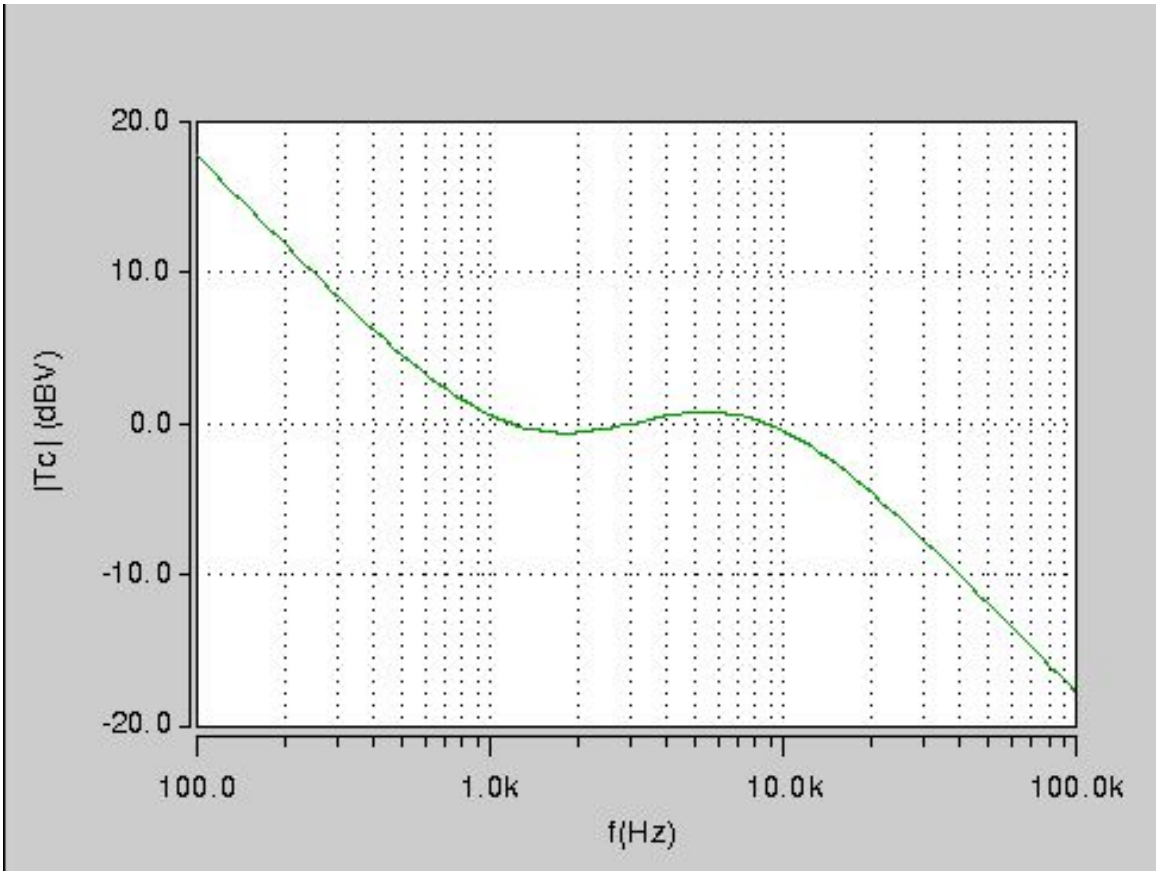

Figure 6.11: Magnitude plot of the designed controller compensation on SABER circuit simulator.

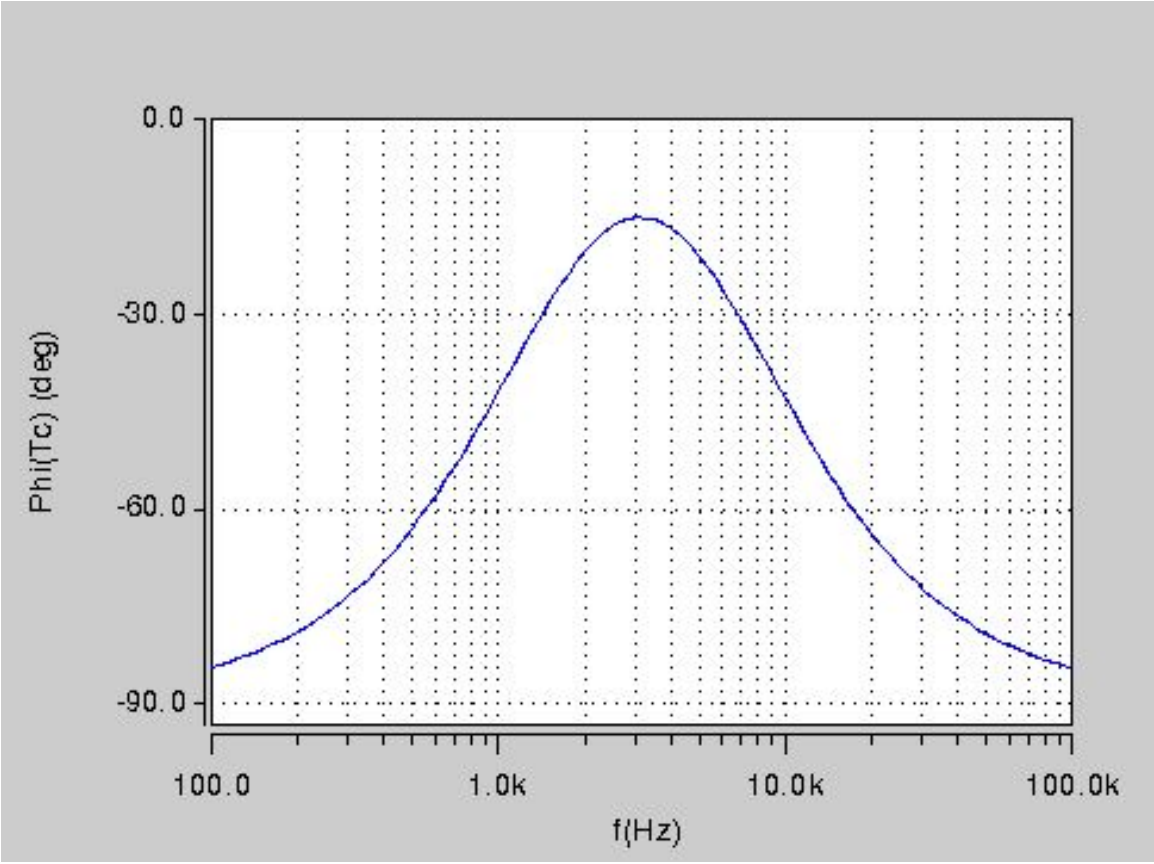

Figure 6.12: Phase plot of the designed controller compensation on SABER circuit simulator.

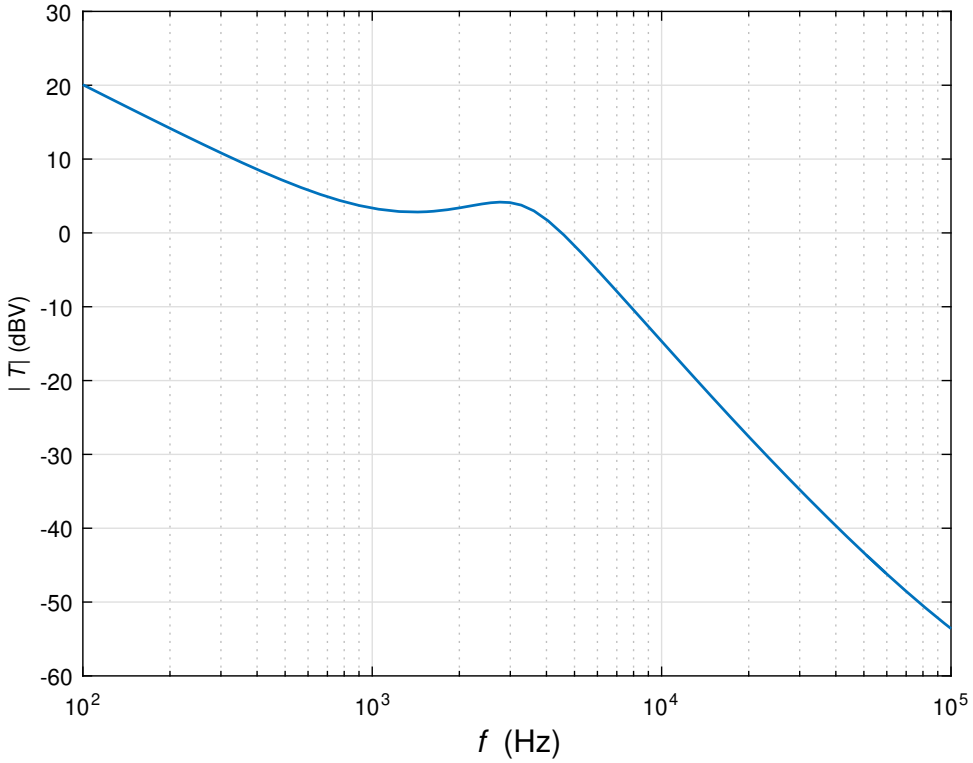

Figure 6.13: Magnitude plot of loop gain with controller compensation.

6.7.2 Frequency Response of T using MATLAB and SABER Circuit Simulator

The magnitude and the phase plot can be seen in Figs. 6.13 and 6.14 respectively. The crossover frequency is $f_c = 4.5$ kHz. The obtained gain margin of the obtained loop gain is 21.7 db and the phase margin is 54°. The respective magnitude and phase plots of the loop-gain on SABER circuit simulator can be seen in Figs. 6.15 and 6.16.

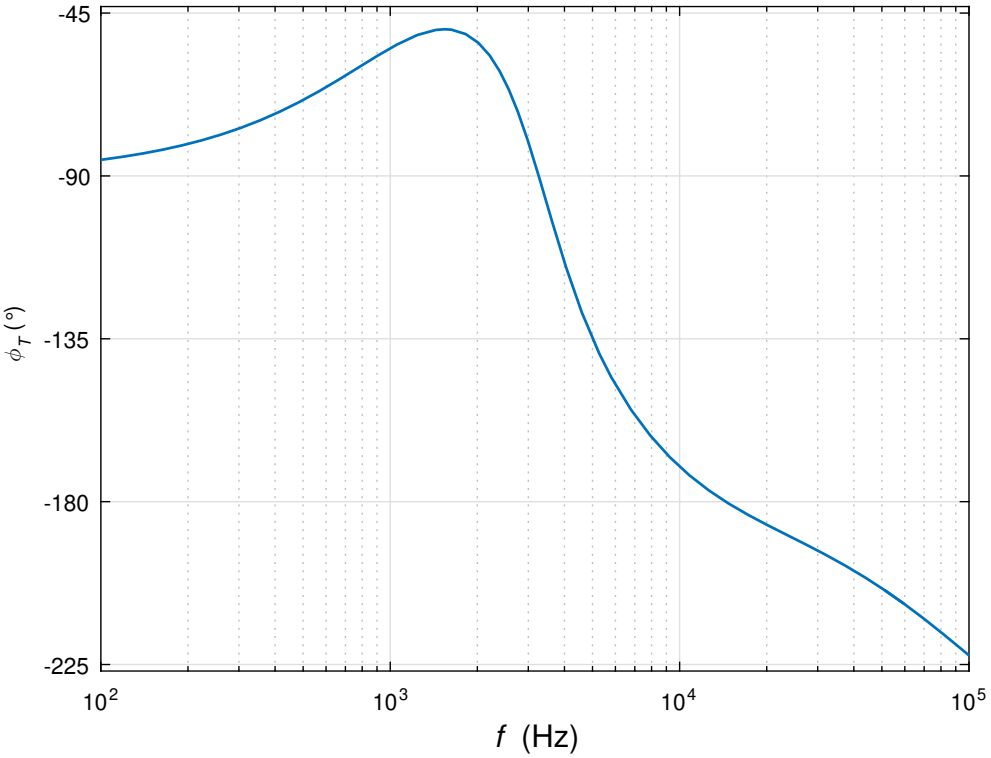

Figure 6.14: Phase plot of loop gain with controller compensation.

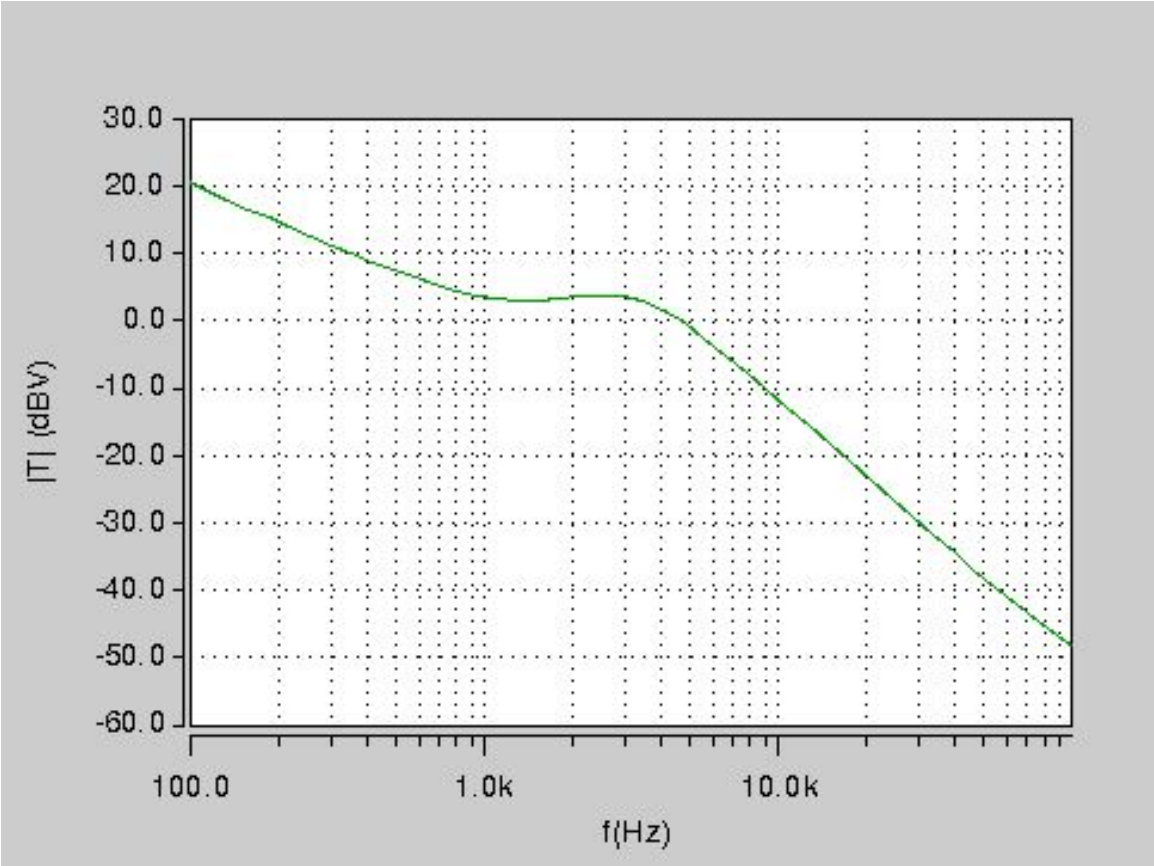

Figure 6.15: Magnitude plot of loop gain with controller compensation on SABER circuit simulator.

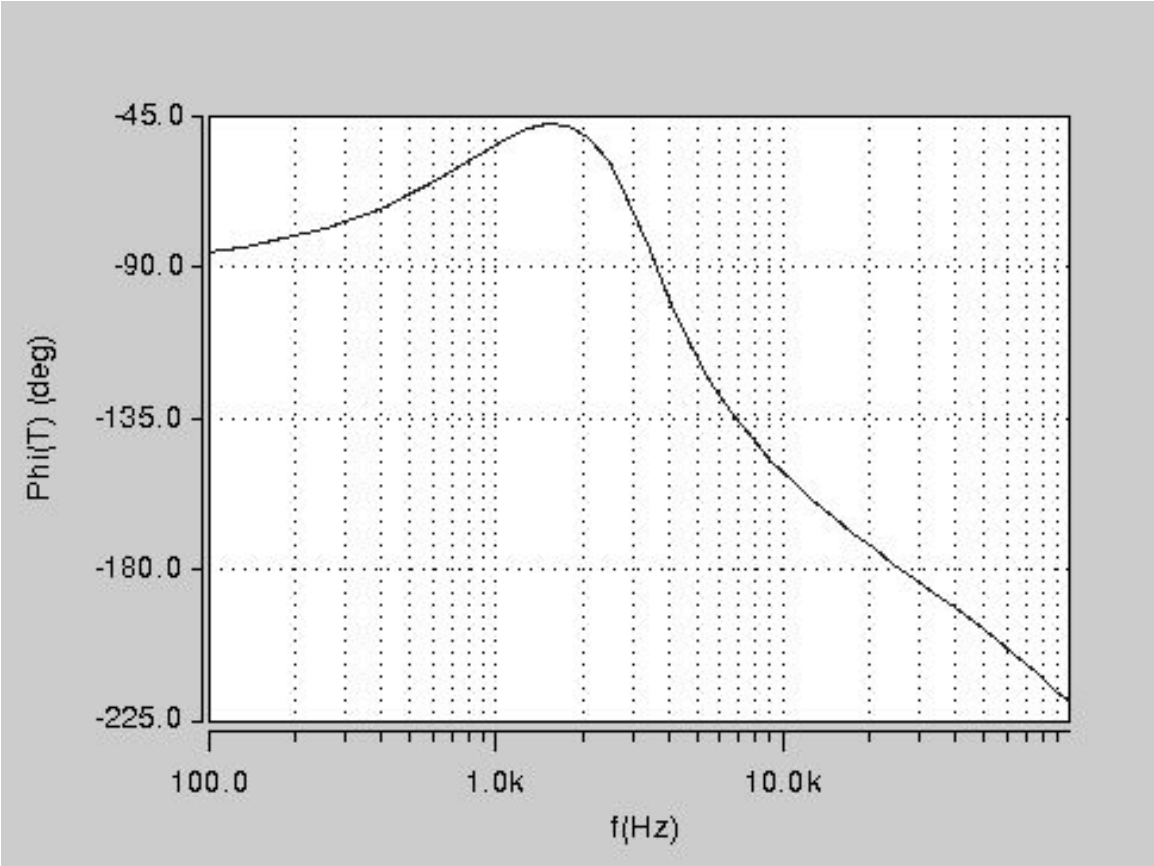

Figure 6.16: Phase plot of loop gain with controller compensation on SABER circuit simulator.

6.8 Experimental Validation of Loop-Gain

6.8.1 Frequency Response of T_c using 4194A Impedance/gain-phase analyzer

To analyzed the controller magnitude an phase plot. The reference input of the network analyzer is connected to the inverting terminal of the controller op-amp. The test input is connected to the output of the op-amp and the injection is connected at the input of the op-amp controller. The inverting input of the op-amp is also virtually grounded. The measured gain-phase plot of the double-lead integral controller when compared to the theoretical plot can be seen in Figs. 6.17 and 6.18. Both the theoretical and practically obtained responses are in good agreement with each other.

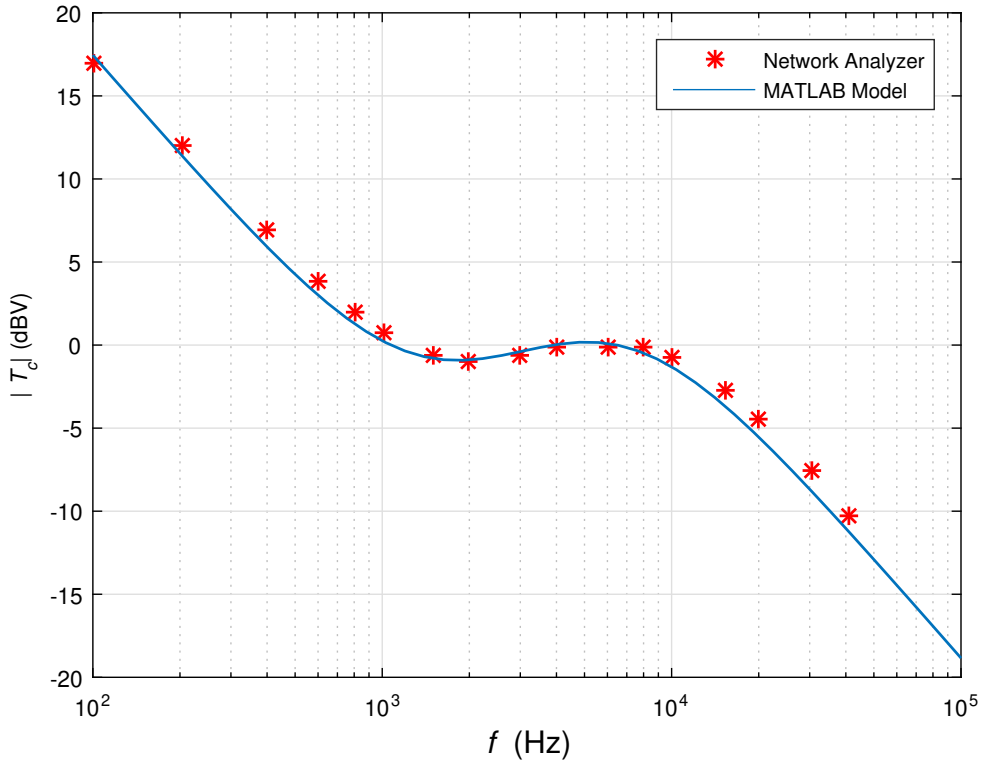

Figure 6.17: Magnitude plot comparing the theoretical and practical results of transfer function T_c.

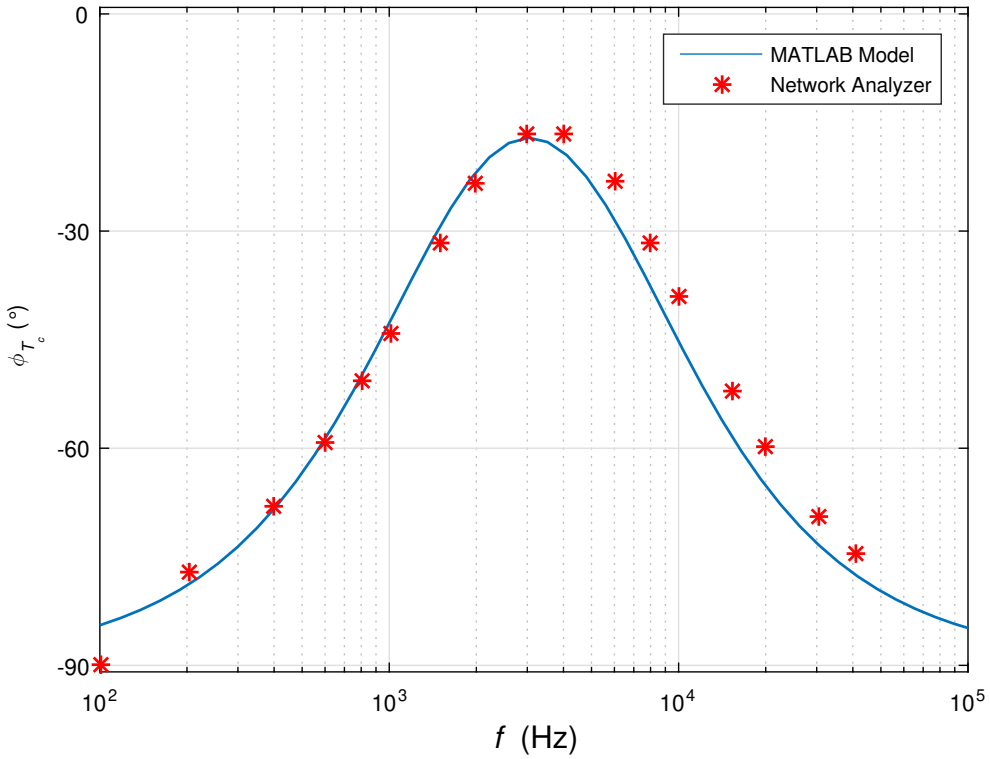

Figure 6.18: Phase plot comparing the theoretical and practical results of transfer function T_c.

6.8.2 Frequency Response of T using 4194A Impedance/gain-phase analyzer

Similar to the open-loop analysis a 4194A impedance/gain-phase analyzer by HP will be used. To inject the changing frequency and amplitude input an injecting resistor R_{in} is used. A low resistance for R_{in} is selected. This low resistance will not effect overall loop-gain. The setup required to measure the loop-gain can be seen in Fig. 6.19. The injection resistor is inserted between the output and the feedback. This is done so that the input side of the network analyzer has higher impedance compared to the output side of the network analyzer. Now the reference input from the network analyzer is connected to the feedback and the test input is connected to the output of

the converter. The obtained magnitude response compared to the theoretical response can be seen in Fig. 6.20. The phase response compared tot he theoretical response can be seen in Fig. 6.21. The obtained responses are in good agreement with the theoretical response.

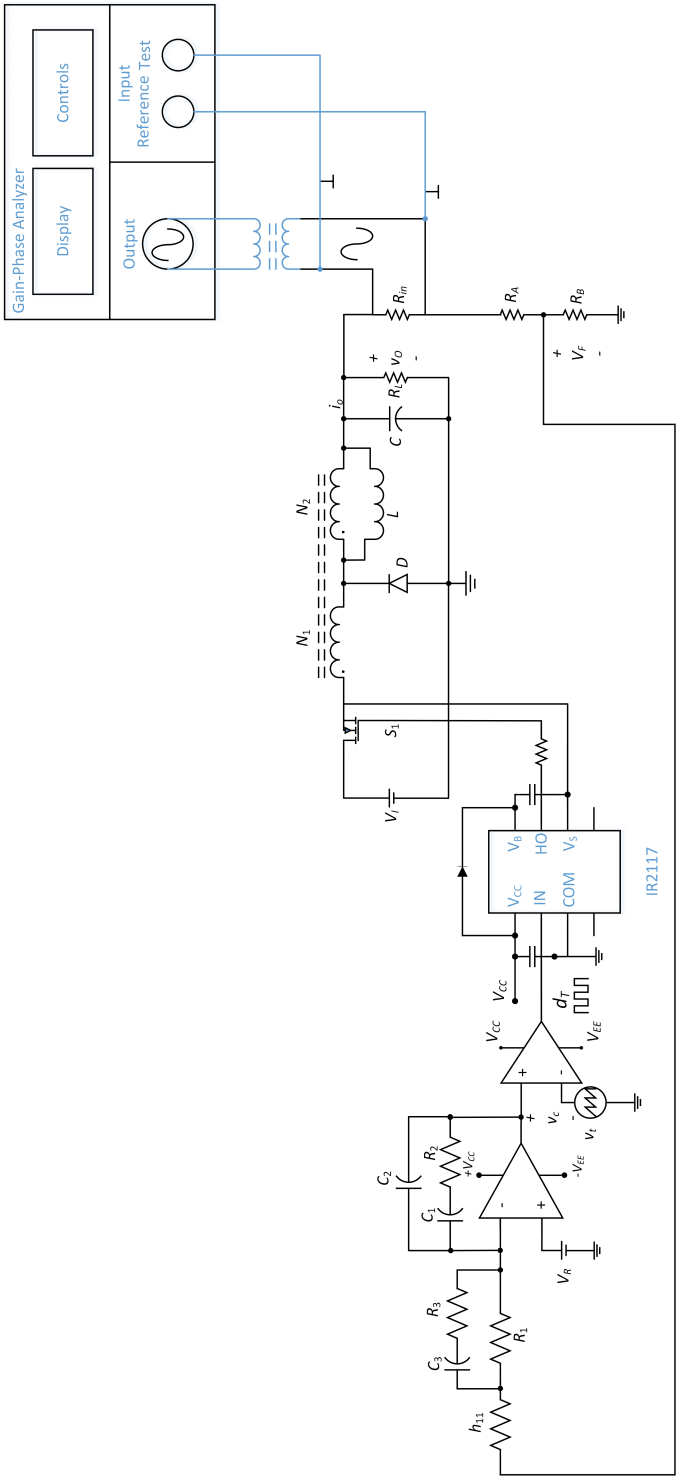

Figure 6.19: Bench setup to obtain loop-gain transfer function.

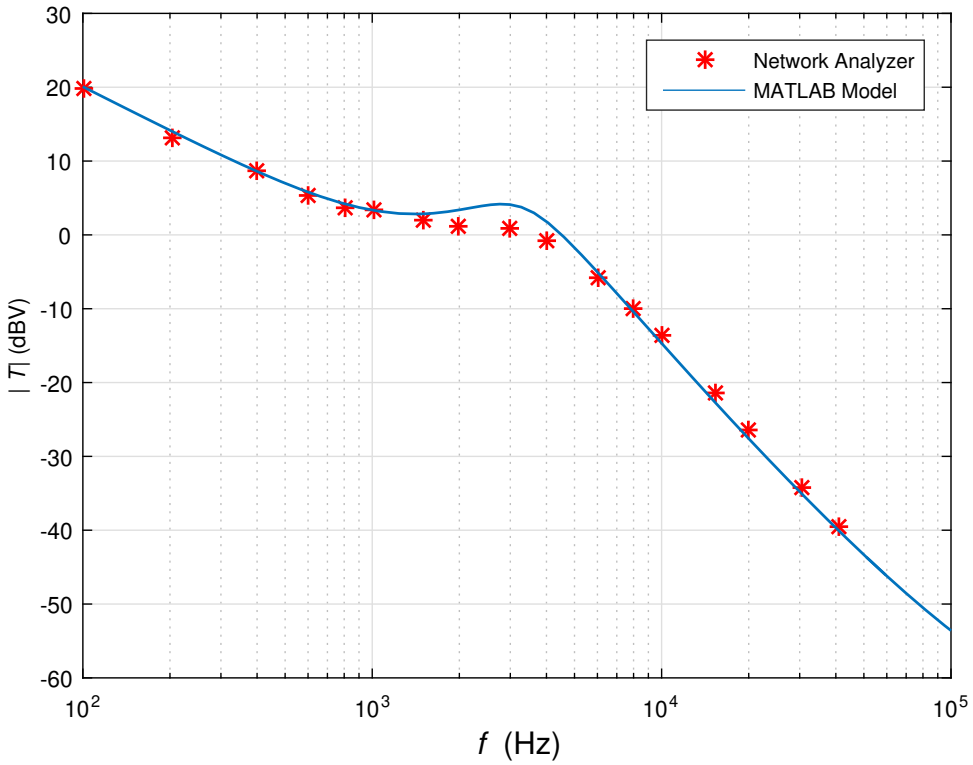

Figure 6.20: Magnitude plot comparing the theoretical and practical results of transfer function T.

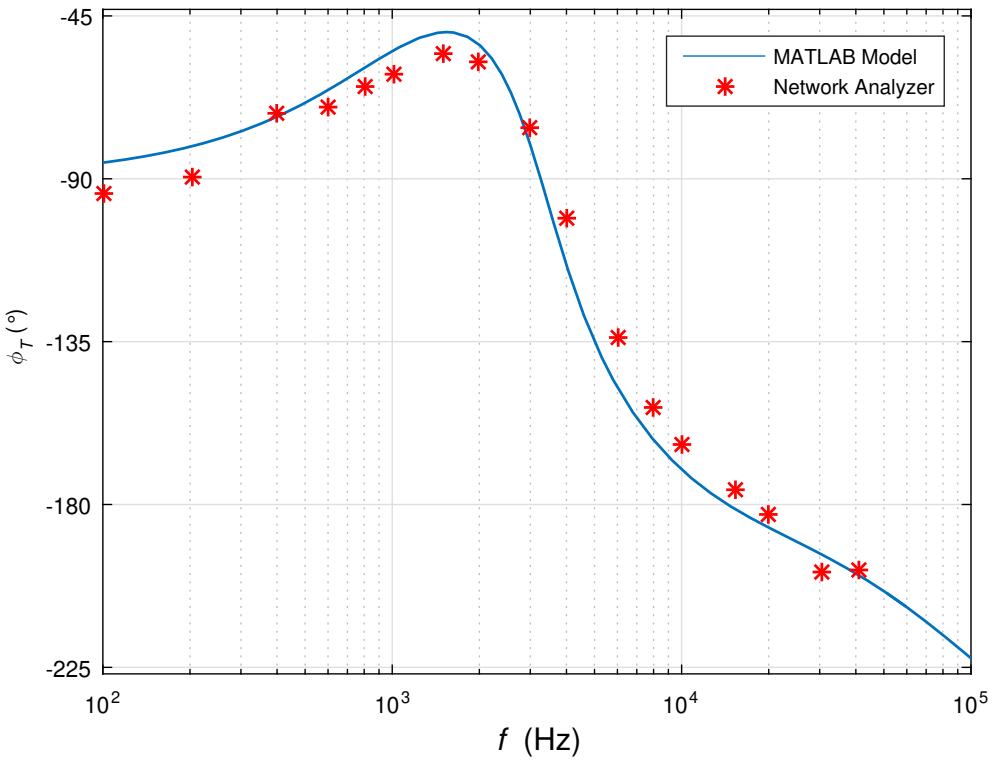

Figure 6.21: Phase plot comparing the theoretical and practical results of transfer function T.

7 Closed-loop Responses

7.1 Closed-loop Control-to-output Voltage Transfer Function

The closed-loop control-to-output voltage transfer function is given by

$$\begin{aligned} T_{cl}(s) = \frac{v_o(s)}{v_r(s)} = \Big|_{v_i=i_o=0} = \frac{A(s)}{1+\beta A(s)} = \frac{T_c(s)T_mT_p(s)}{1+\beta T_c(s)T_mT_p(s)} \\ = \frac{T_x}{\beta}\frac{(s+\omega_{zc})^2(s+\omega_{zn})(s-\omega_{zp})}{s(s+\omega_{pc})^2(s^2+2\xi\omega_0 s+\omega_0^2)+T_x(s+\omega_{zc})^2(s+\omega_{zn})(s-\omega_{zp})} \end{aligned} \tag{7.1}$$

7.2 Closed-loop Input-to-output Voltage Transfer Function

The closed-loop input-to-output voltage transfer function is given by

$$\begin{aligned} M_{vcl}(s) = \frac{v_o(s)}{v_i(s)} = \Big|_{v_r=i_o=0} = \frac{M_v(s)}{1+T(s)} = \frac{M_v(s)}{1+\beta T_c(s)T_mT_p(s)} \\ = \frac{M_{vx}s(s+\omega_{zn})(s+\omega_{pc})^2}{s(s+\omega_{pc})^2(s^2+2\xi\omega_0 s+\omega_0^2)+T_x(s+\omega_{zc})^2(s+\omega_{zn})(s-\omega_{zp})} \end{aligned} \tag{7.2}$$

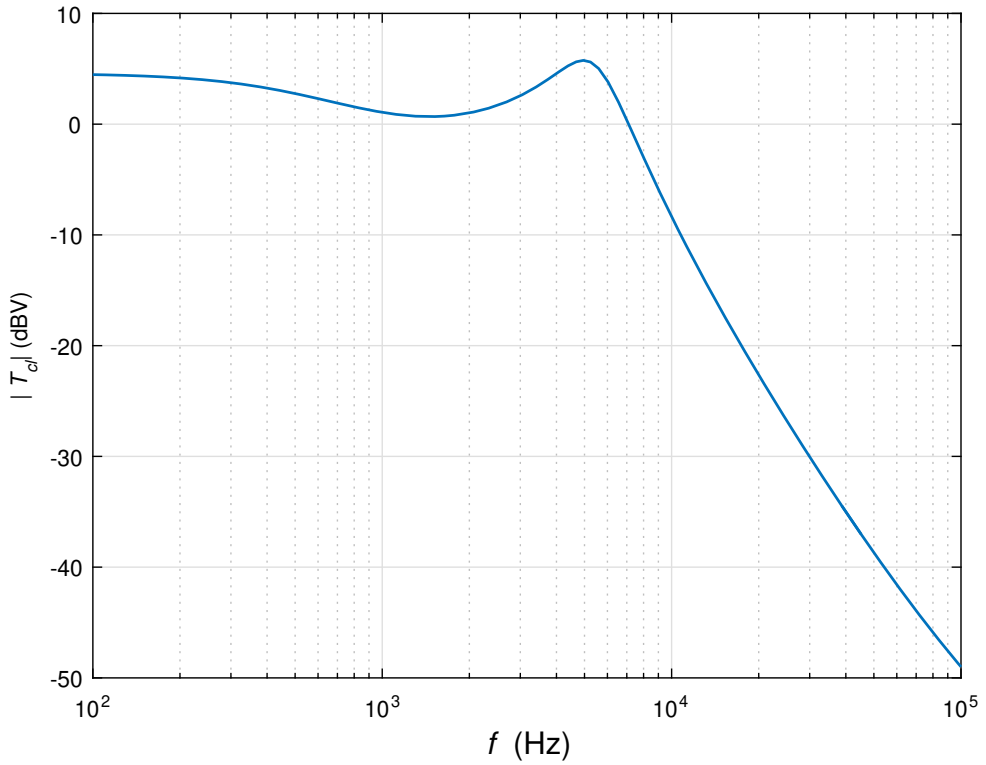

Figure 7.1: Magnitude plot of the T_{cl} transfer function as obtained on MATLAB.

7.3 Simulation validation of the closed-loop Tapped-Buck DC-DC Converter

7.3.1 Frequency Response of T_{pcl} using MATLAB and SABER Circuit Simulator

The magnitude and phase plots as seen on MATLAB can be seen in Figs. 7.1 and 7.2. The dc gain as observed in Fig. 7.1 is 20 dB. This is equivalent to 10 V.

7.3.2 Frequency Response of M_{vcl} using MATLAB and SABER Circuit Simulator

The magnitude and phase plots as seen on MATLAB can be seen in Figs. 7.5 and 7.6. As seen in the magnitude response the magnitude is way lower than 0 dB. This means that any perturbations in the system die to the input of the converter will get

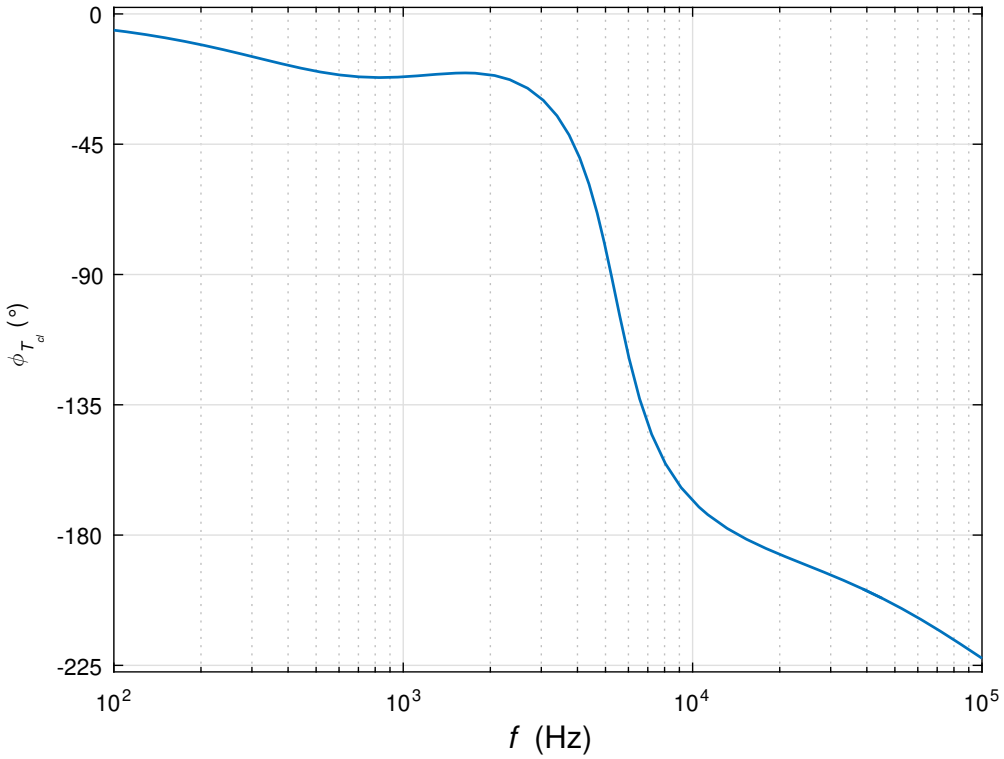

Figure 7.2: Phase plot of the T_{cl} transfer function as obtained on MATLAB.

attenuated and thus would not reflect on the output voltage.

7.3.3 Response of Output Voltage for a Step Change in Reference Voltage

For a step change in reference voltage of $\delta v_r = 0.1$ the output voltage should increase by 1 V. The time-domain responses of the closed-loop control-to-output voltage transfer function can be seen in Fig. 7.9 and The measured values of overshoot, rise time and settling time are 0 %, 77 μsec, 1 msec respectively. The response is in good agreement with the frequency-domain response.

7.3.4 Response of Output Voltage for a Step Change in Input Voltage

It can be observed that the closed-loop response is better as compared to the open-loop response as the response has an overshoot of around 4.5 %, the settling time

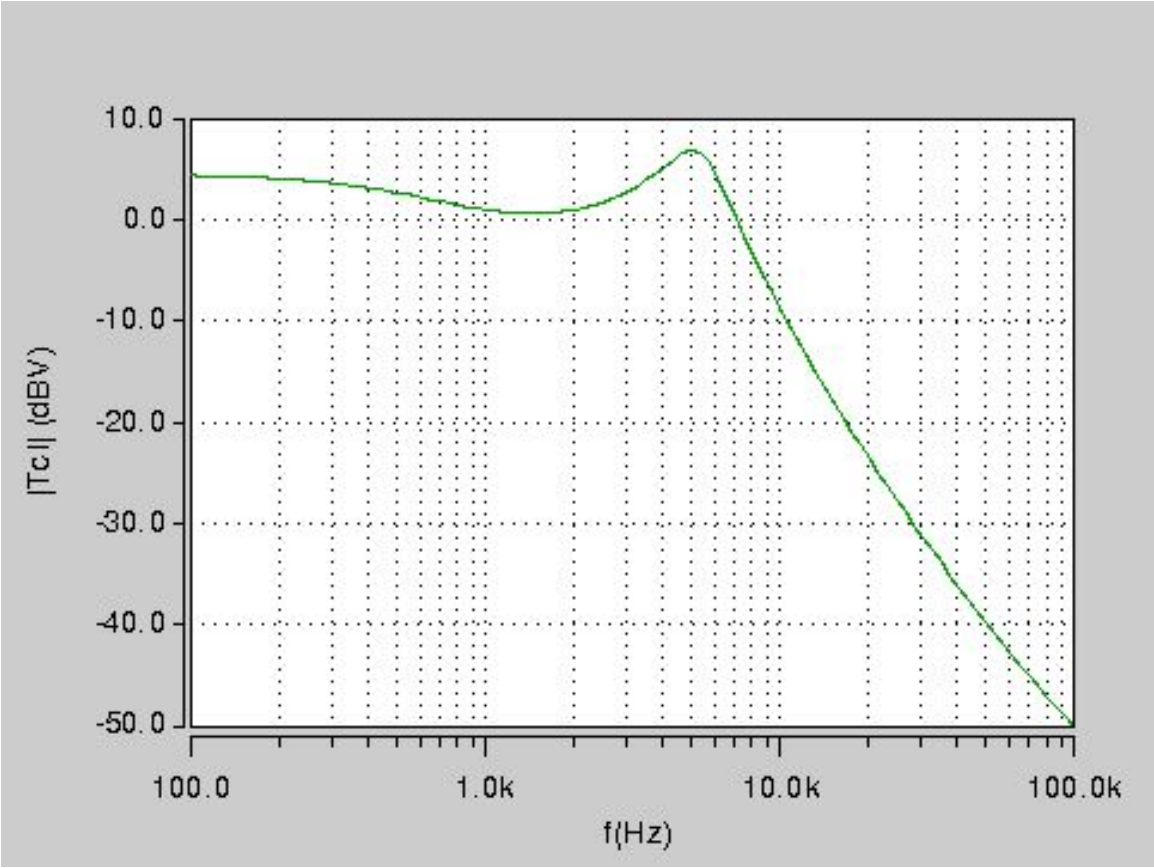

Figure 7.3: Magnitude plot of the T_{cl} transfer function as obtained on SABER Simulator.

Figure 7.4: Phase plot of the T_{cl} transfer function as obtained on SABER Simulator.

has dropped down to 1.14 msecs and rise time has dropped down to almost 0.The time-domain responses of the closed-loop input-to-output voltage transfer function can be seen in Fig. 7.11, as seen in this response the output voltage auto-corrects itself and prevents any effect on the output voltage.

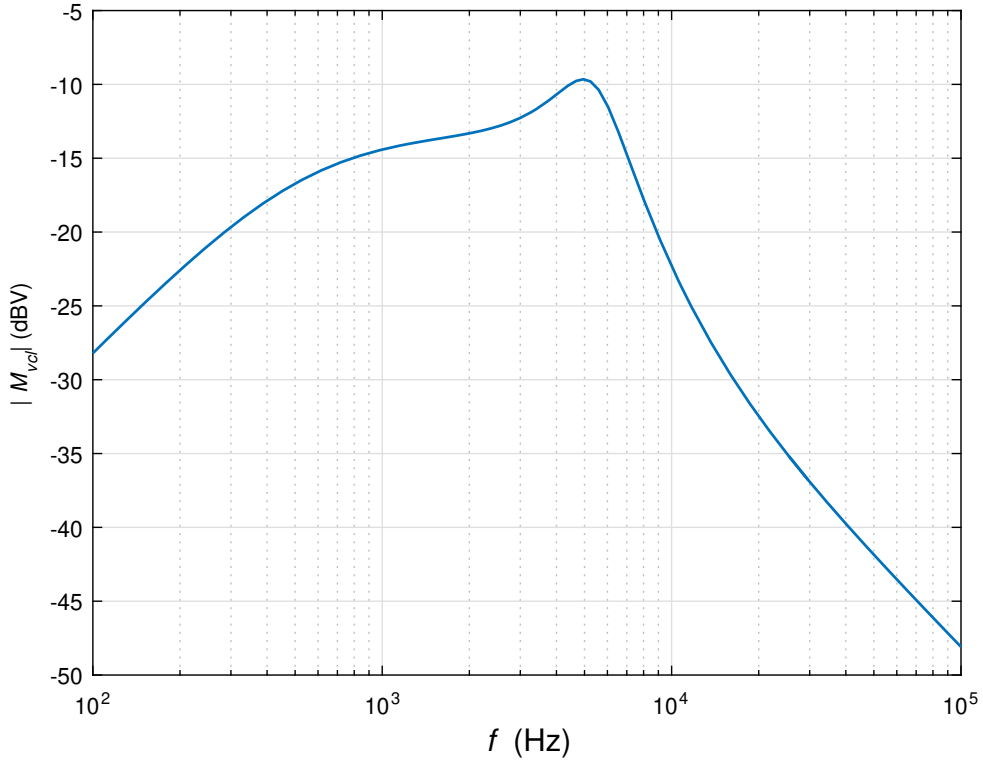

Figure 7.5: Magnitude plot of the M_{vcl} transfer function as obtained on MATLAB.

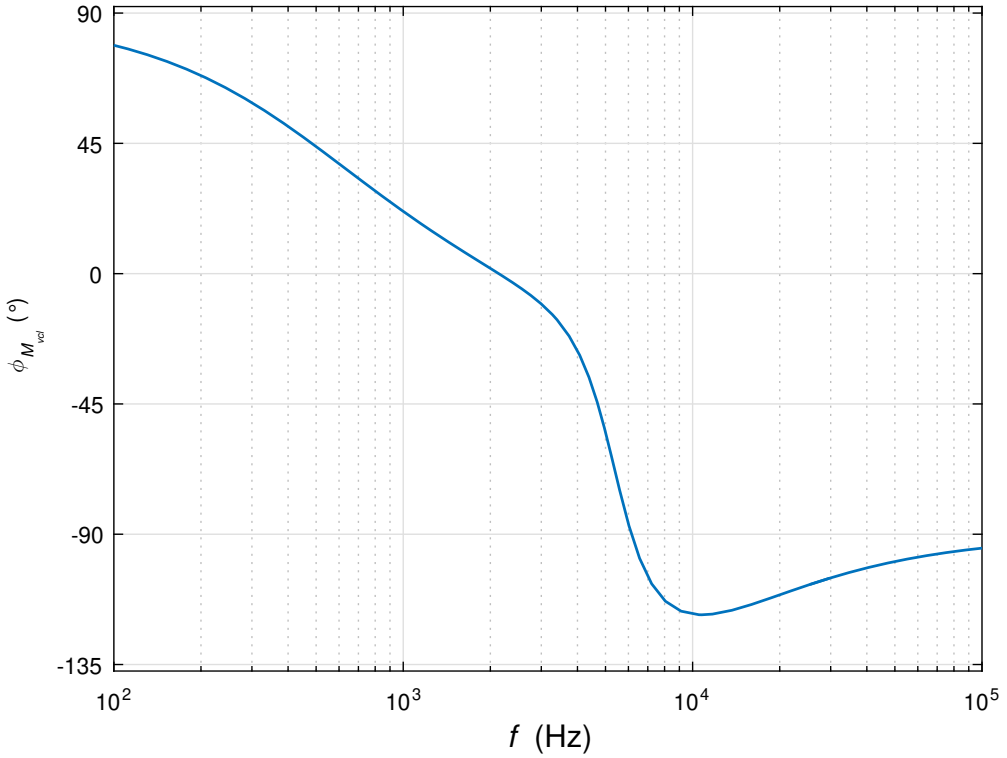

Figure 7.6: Phase plot of the M_{vcl} transfer function as obtained on MATLAB.

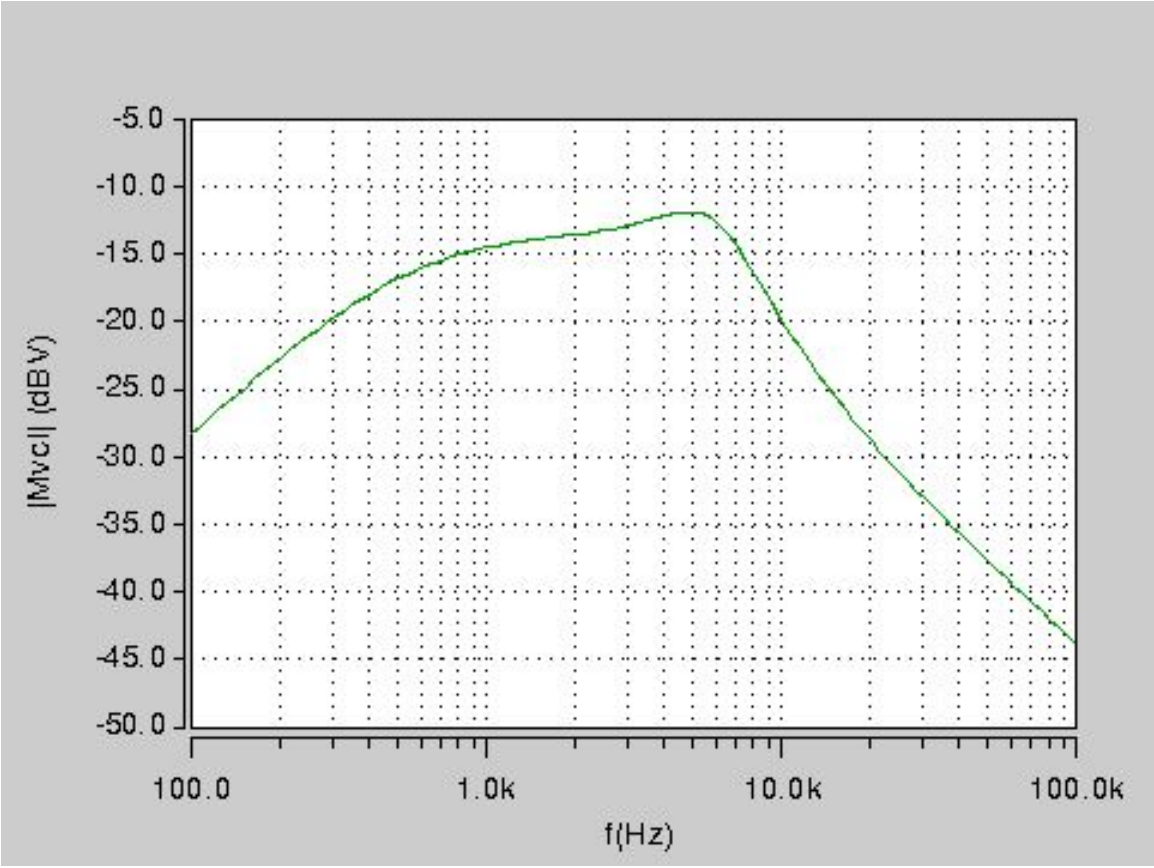

Figure 7.7: Magnitude plot of the M_{vcl} transfer function as obtained on SABER Simulator.

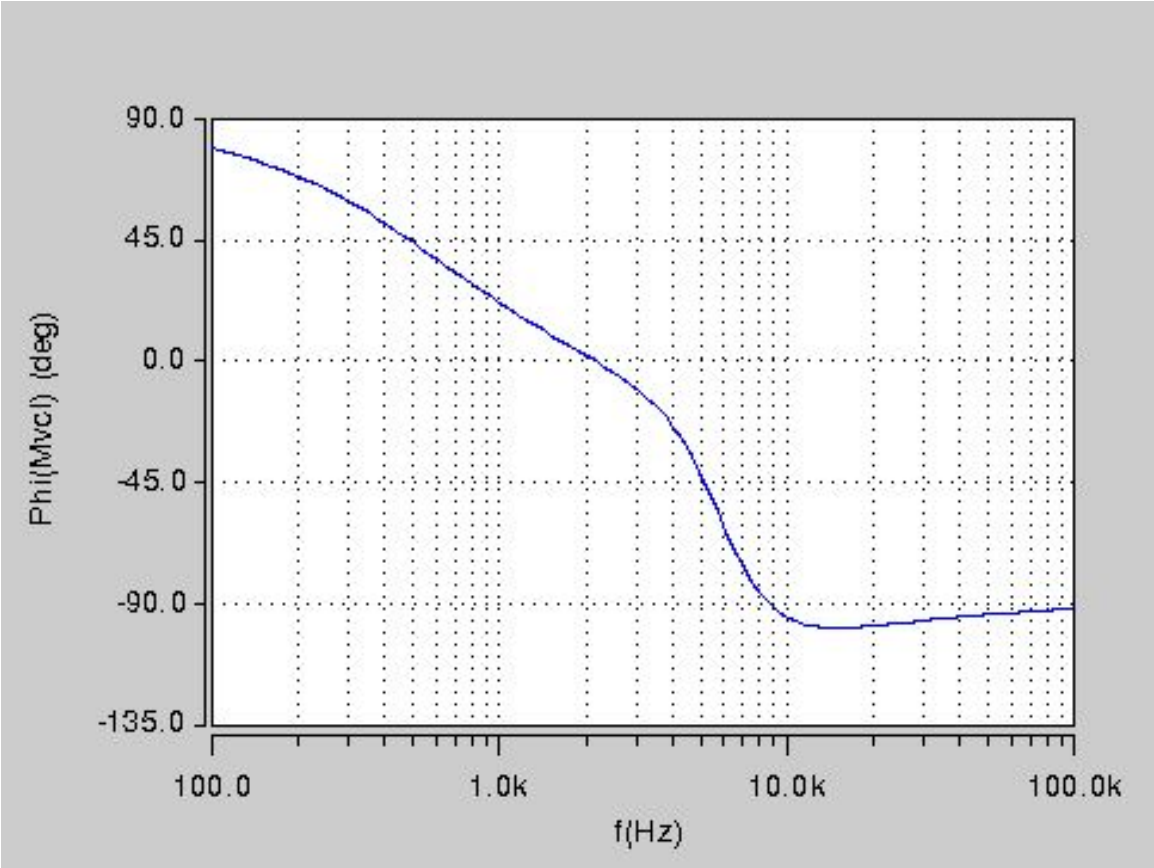

Figure 7.8: Phase plot of the M_{vcl} transfer function as obtained on SABER Simulator.

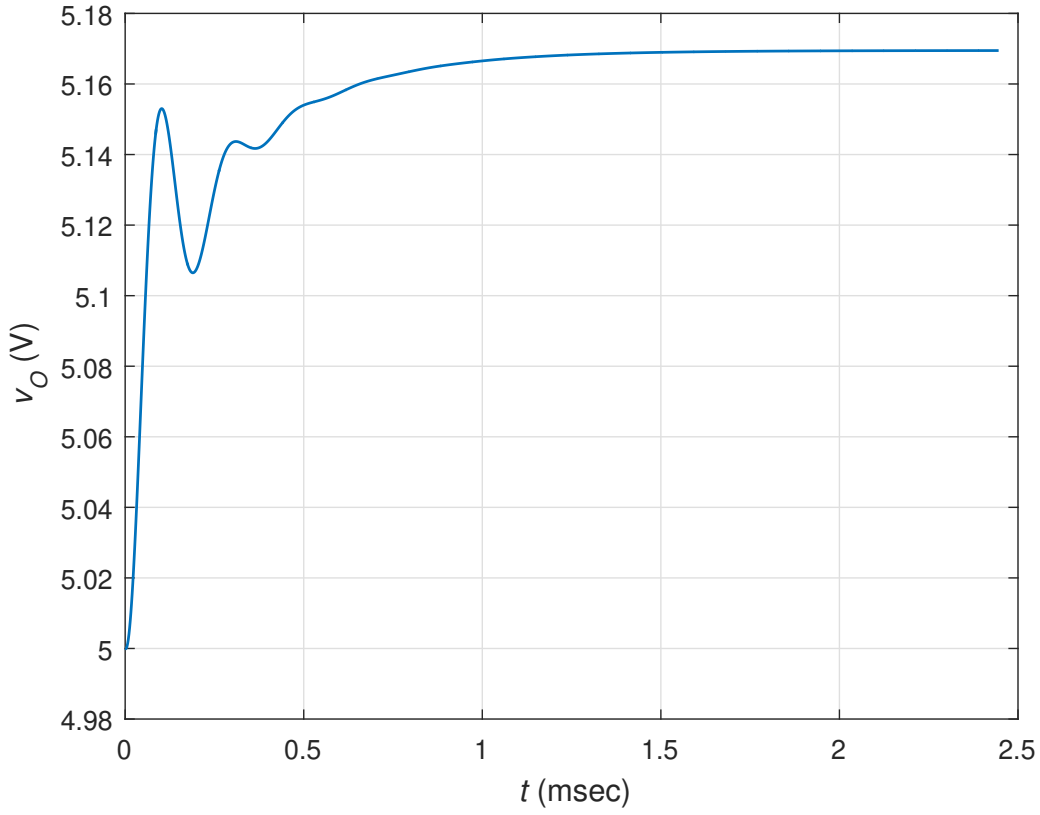

Figure 7.9: Step Response of closed-loop control-to-output voltage transfer function.

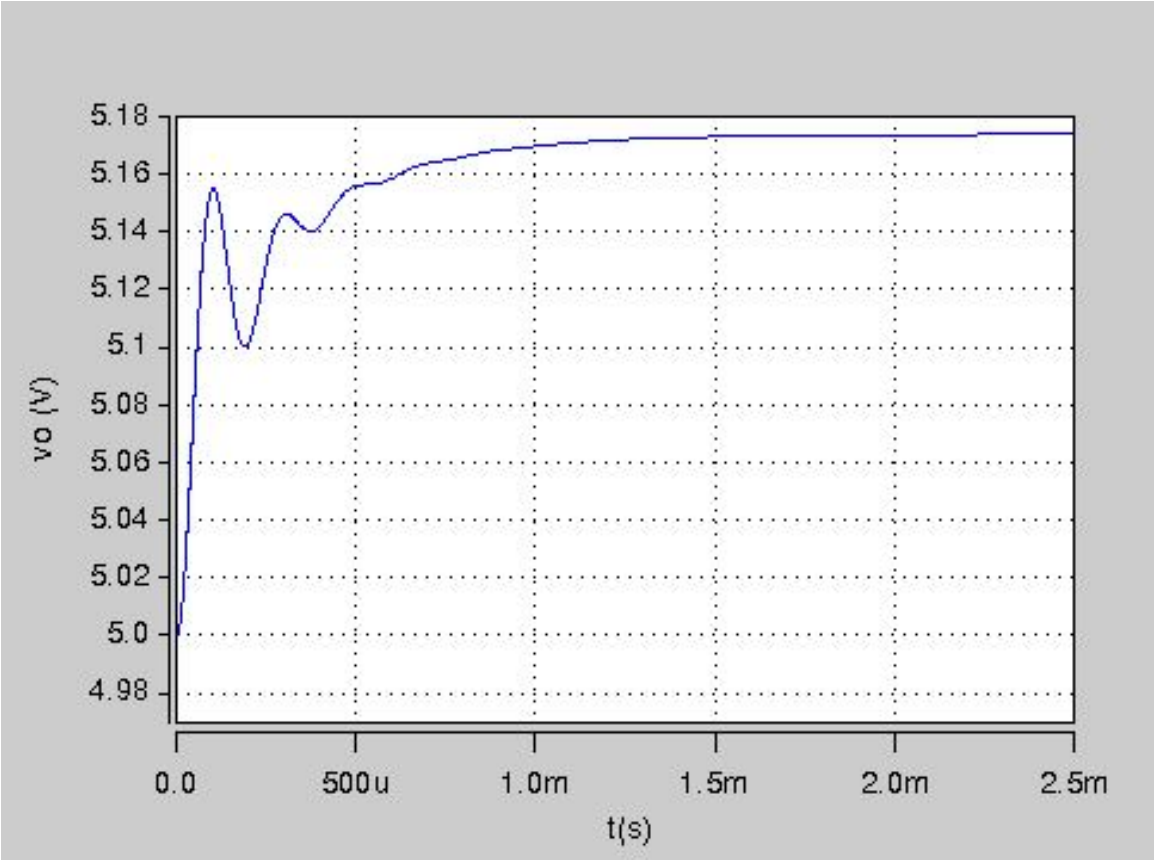

Figure 7.10: Step Response of closed-loop control-to-output voltage transfer function.

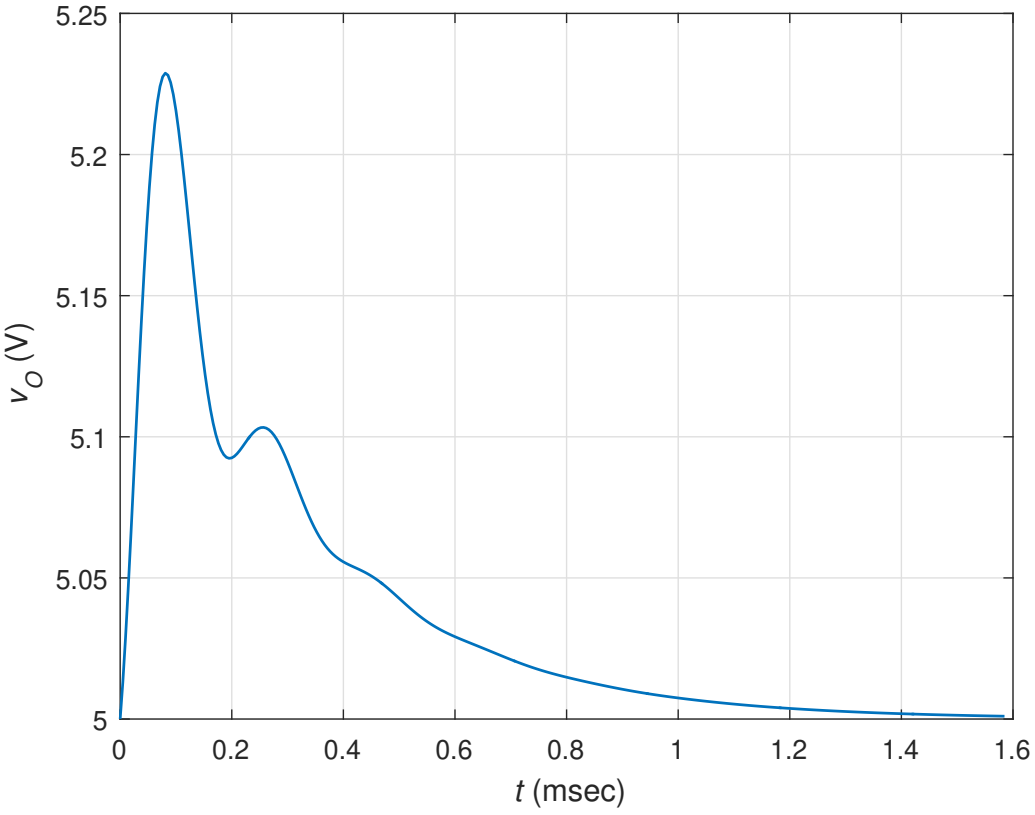

Figure 7.11: Step Response of closed-loop input-to-output voltage transfer function.

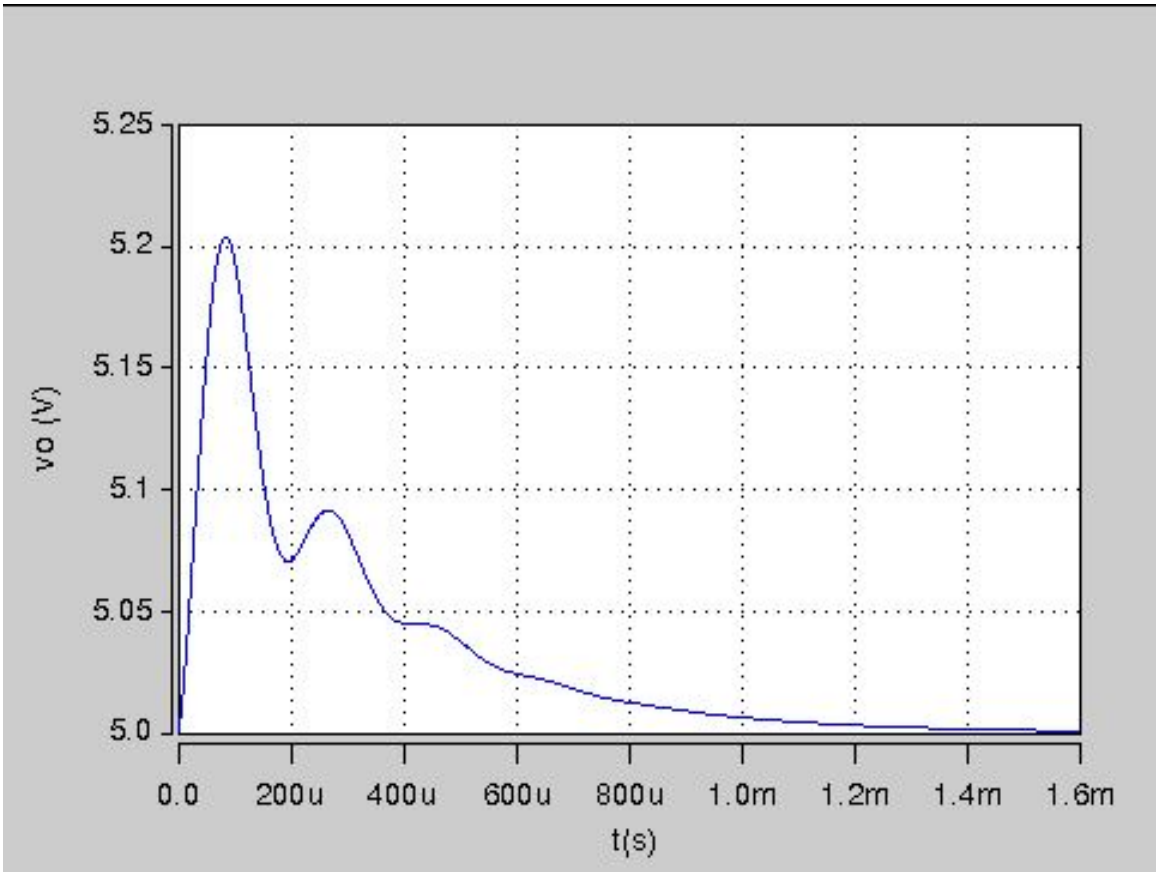

Figure 7.12: Step Response of closed-loop control-to-output voltage transfer function.

7.4 Experimental validation of the closed-loop Tapped-Buck DC-DC Converter

The designed converter can be made to run over different frequencies to check for its magnitude and phase responses between the inputs and outputs using a 4194A Impedance/gain-phase analyzer. This equipment is designed to measure transmission characteristics of a plant for a wide frequency ranges. This specific model is capable of testing the equipment is capable of testing the plant between the frequency range of 10 Hz - 100 MHz. This is fully capable of handling the designed converter over the required frequency ranges. The obtained plots is then used to validated the ones obtained using MATLAB and SABER circuit simulations. The Drawback of using this equipment is that, it can not read any dc values at its input. This will required an additional circuit modifications which requires huge bulk capacitors at the input of the instrument to eliminate any dc component running into the instrument.

7.4.1 Frequency Response of T_{pcl} Using 4194A Impedance/gain-phase Analyzer

For the transfer function in question, the change in the reference voltage of the controller can be taken as the input of the transfer function and is connected reference input of the network analyzer. This input is also connected in series with the output of the network analyzer. This is made possible by using an isolating transformer with 50:1 turns ratio. This reduces the magnitude of the response by -26 dB. The output voltage of the converter is considered as the output of the transfer functions. This is connected to the test input of the network analyzer. The 4194A can now be used to produce required frequency plots and as mentioned earlier. The setup required to obtained transfer function can be seen in Fig. 7.13. The obtained magnitude and phase response of the closed-loop converter compared to the theoretically obtained response can be seen in Figs. 7.14 and 7.15 respectively.

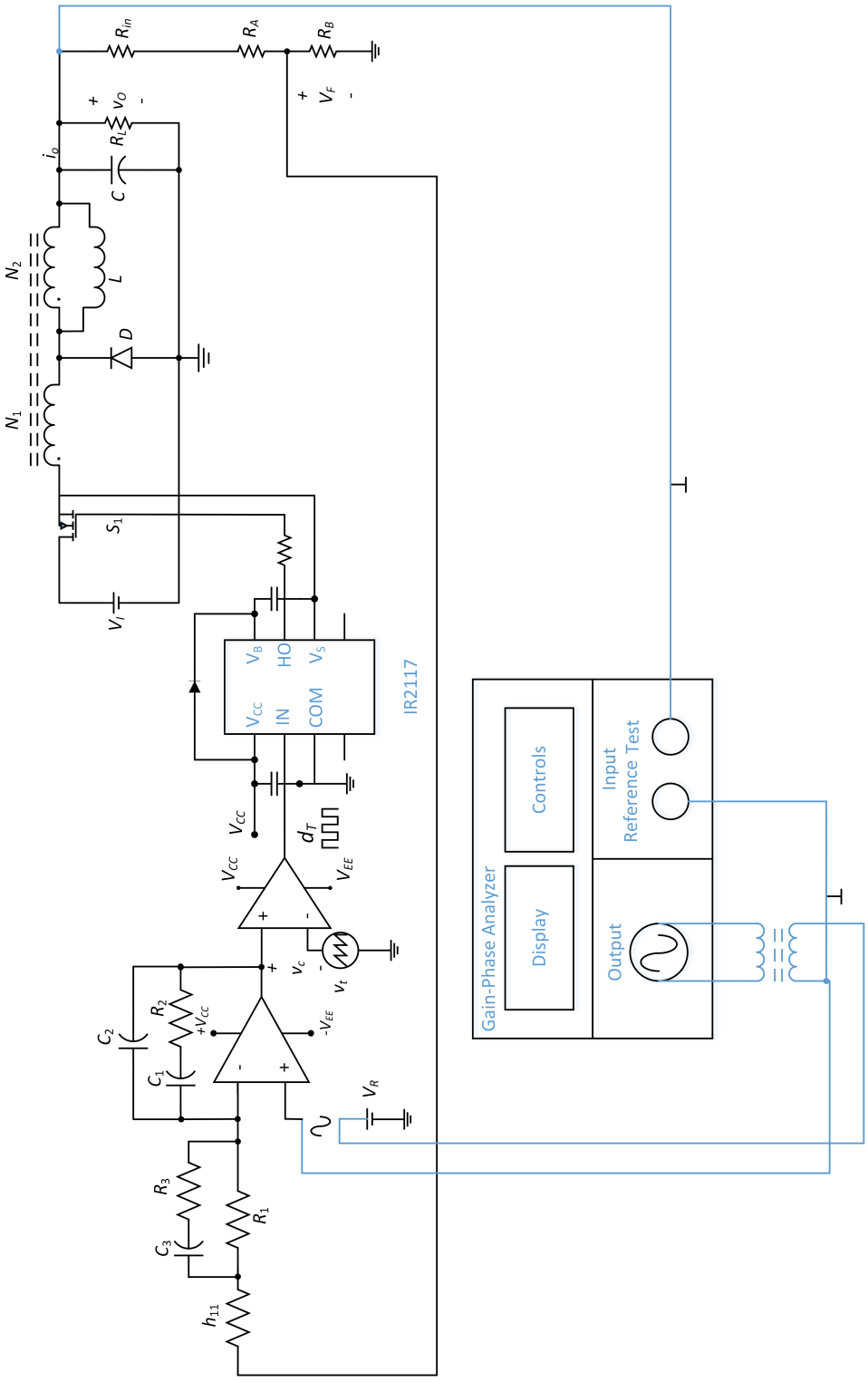

Figure 7.13: Bench setup to obtain closed-loop control-to-output voltage transfer function.

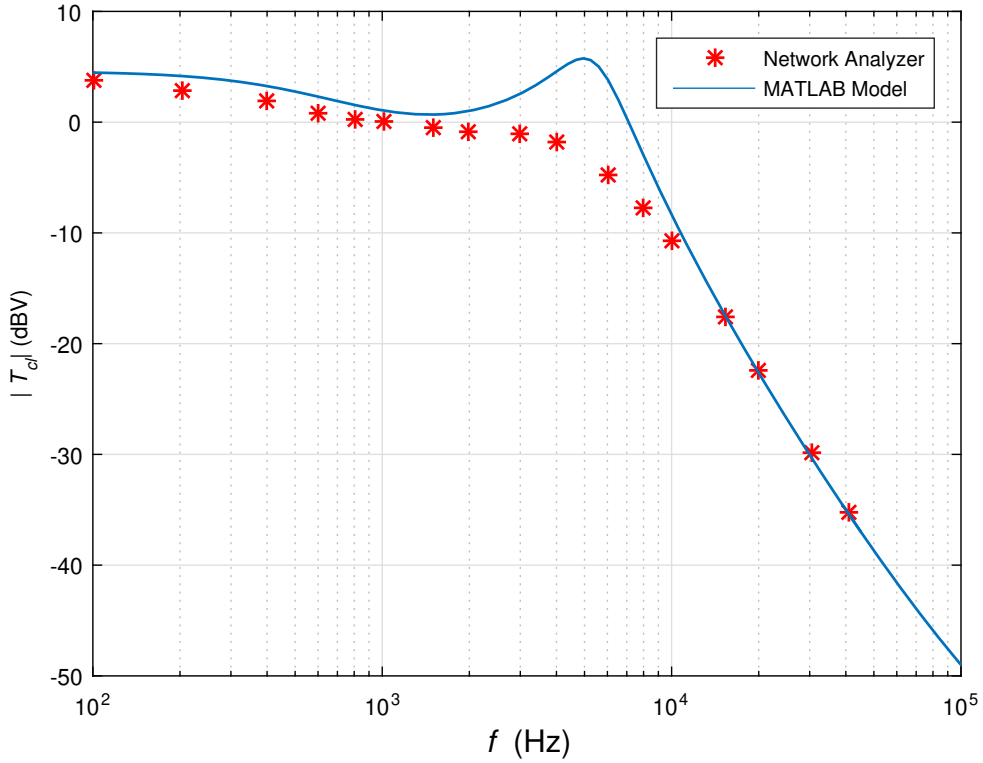

Figure 7.14: Magnitude plot comparing the theoretical and practical results of transfer function T_{cl}.

7.4.2 Frequency Response of M_{vcl} Using 4194A Impedance/gain-phase Analyzer

For the transfer function in question the change in the input voltage of the converter can be taken as the input of the transfer function. An isolating transformer with 50:1 turns ratio is used to add the output of the network analyzer in series with the input of the dc-dc converter. This adds a -26 dB magnitude of the output response. The network analyzer's reference inputs is also connected to the output of the isolating transformer. The output voltage of the converter can be considered as the output of the transfer functions. The test input of the network analyzer is connected to the output of the converter. The required test setup can be seen in Fig.

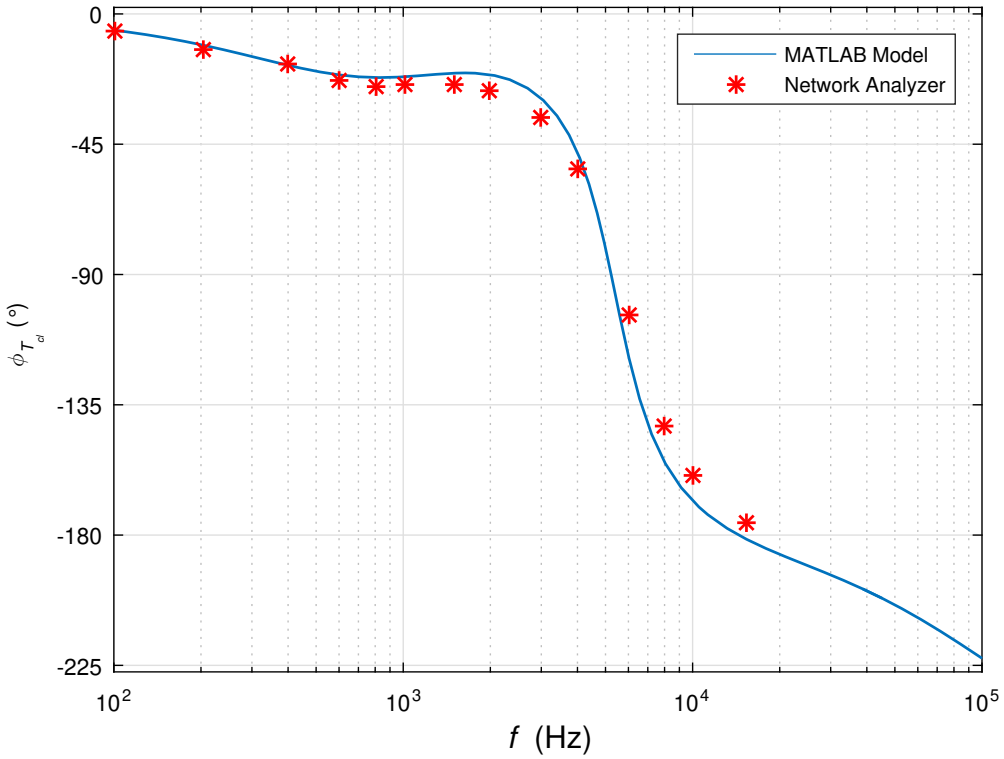

Figure 7.15: Phase plot comparing the theoretical and practical results of transfer function T_{cl}.

7.16. The obtained magnitude and phase response can be seen in Figs. 7.17 and 7.18 respectively.

7.4.3 Response of Output Voltage for a Step Change in Duty Cycle

The non-inverting input of the op-amp can be connected to a step-input. By producing a step voltage at the input of the op-amp will help produce a step response at the output voltage. The obtained response on oscilloscope can be seen in Fig. 7.19. The measured values of overshoot, rise time and settling time are 0 %, 13 μsec, 1.7 msec respectively.

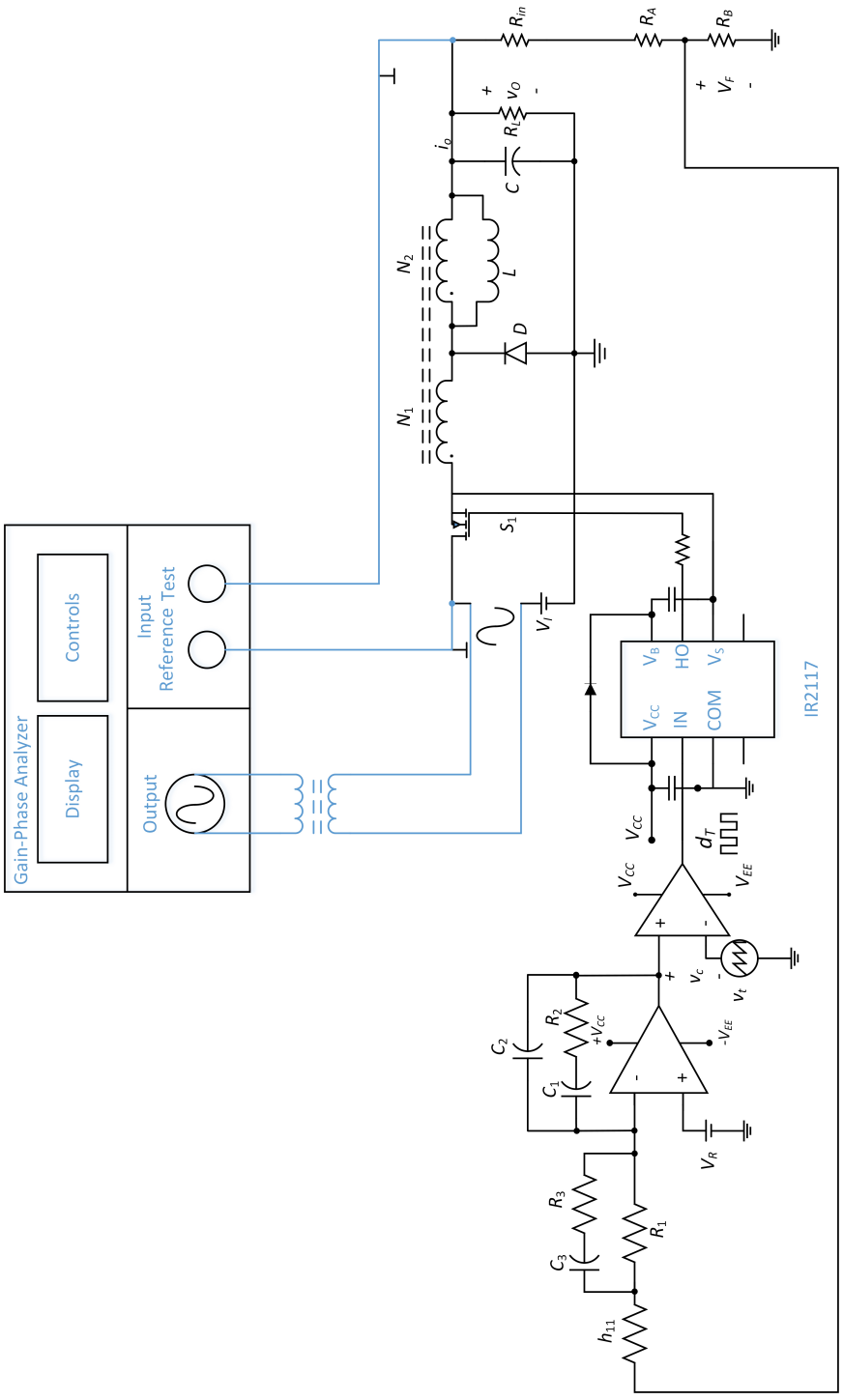

Figure 7.16: Bench setup to obtain closed-loop input-to-output voltage transfer function.

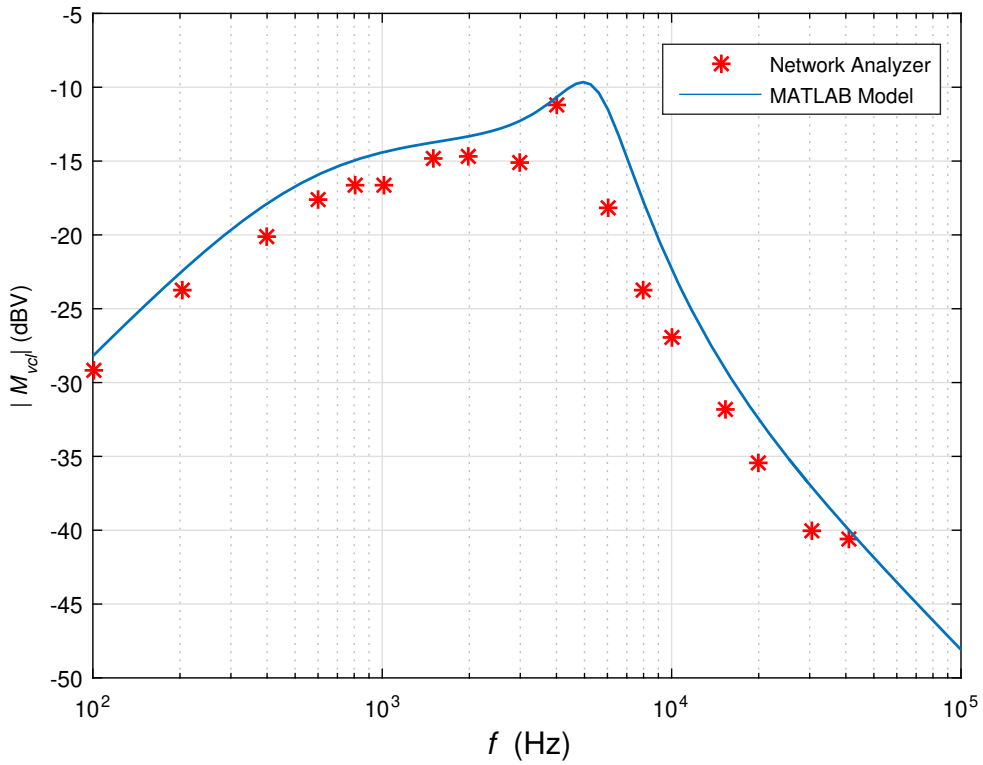

Figure 7.17: Magnitude plot comparing the theoretical and practical results of transfer function M_{vcl}.

7.4.4 Response of Output Voltage for a Step Change in Reference Voltage

A step input can be connected to the reference of the controller. By producing a step voltage at the input of the controller a step response at the output voltage is produced. The obtained response can be seen in Fig. 7.20. The measured values of overshoot, rise time and settling time are 10 %, 0 μsec, 1.7 msec respectively.

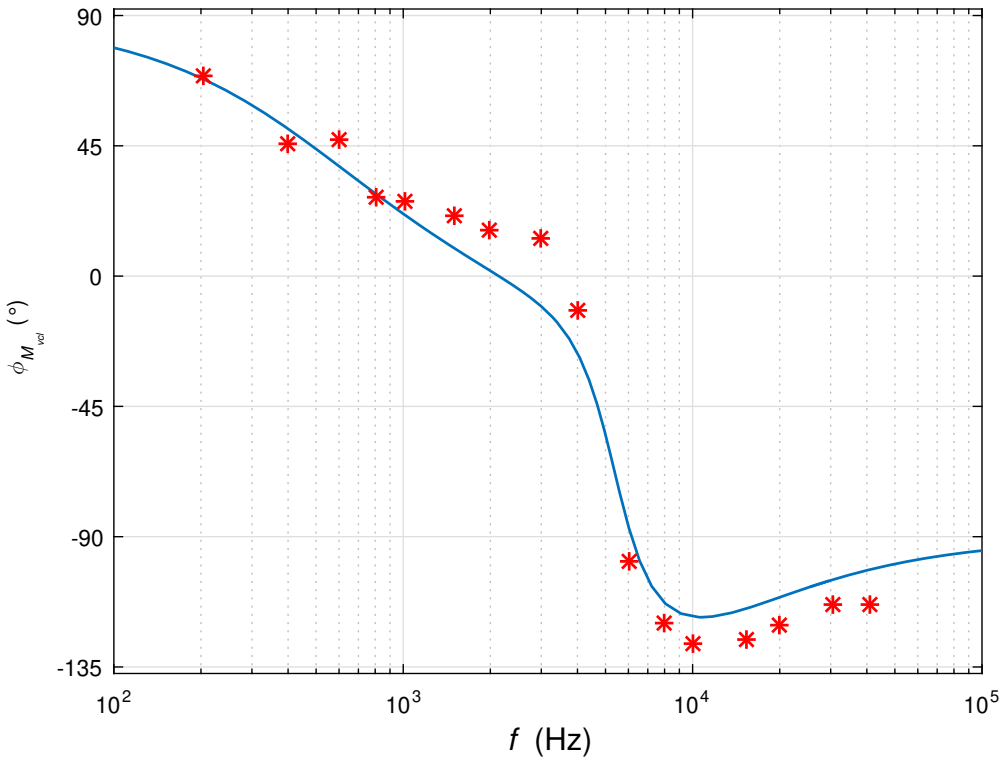

Figure 7.18: Phase plot comparing the theoretical and practical results of transfer function M_{vcl}.

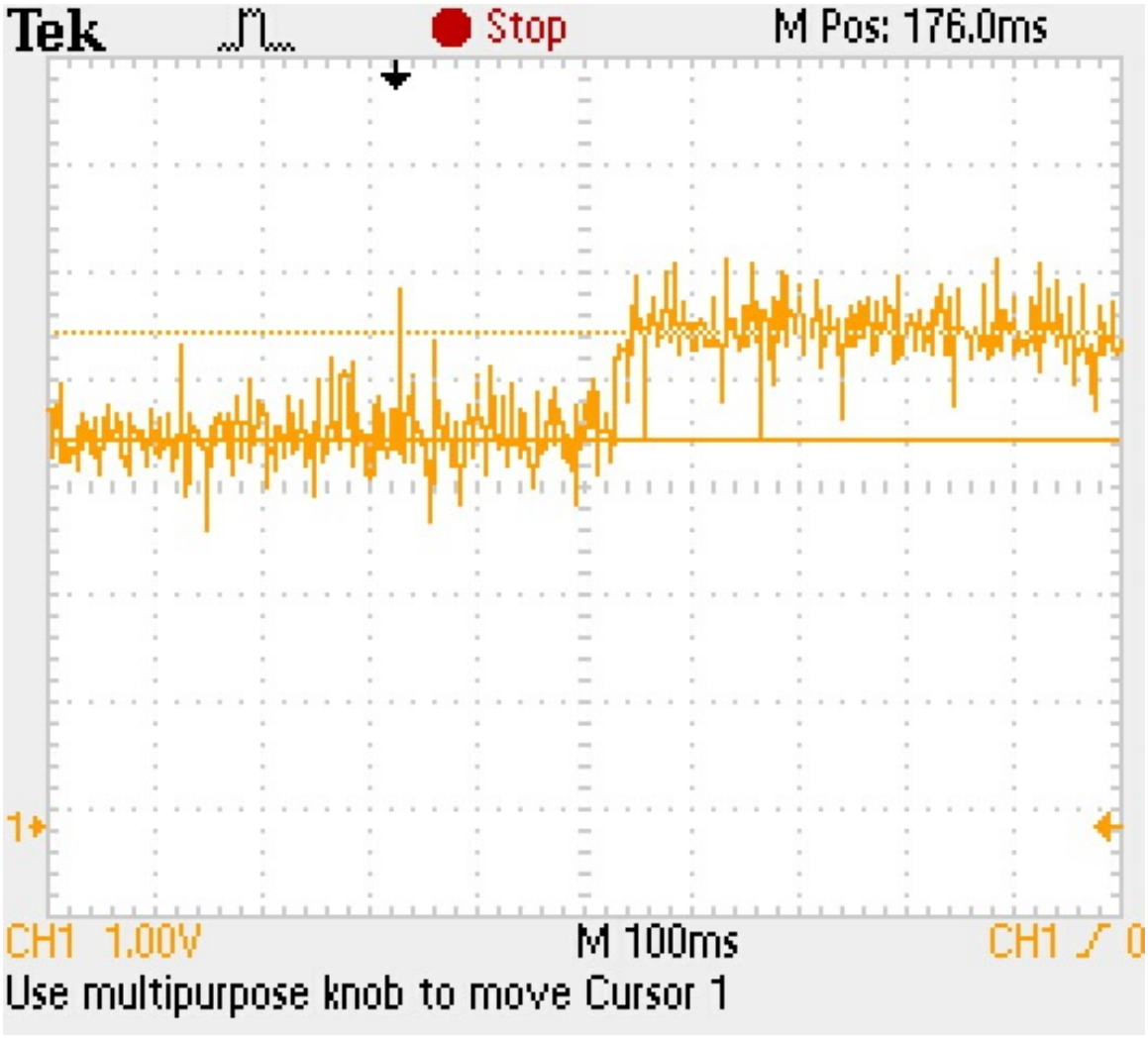

Figure 7.19: Step response of T_{pcl} as obtained on the test bench.

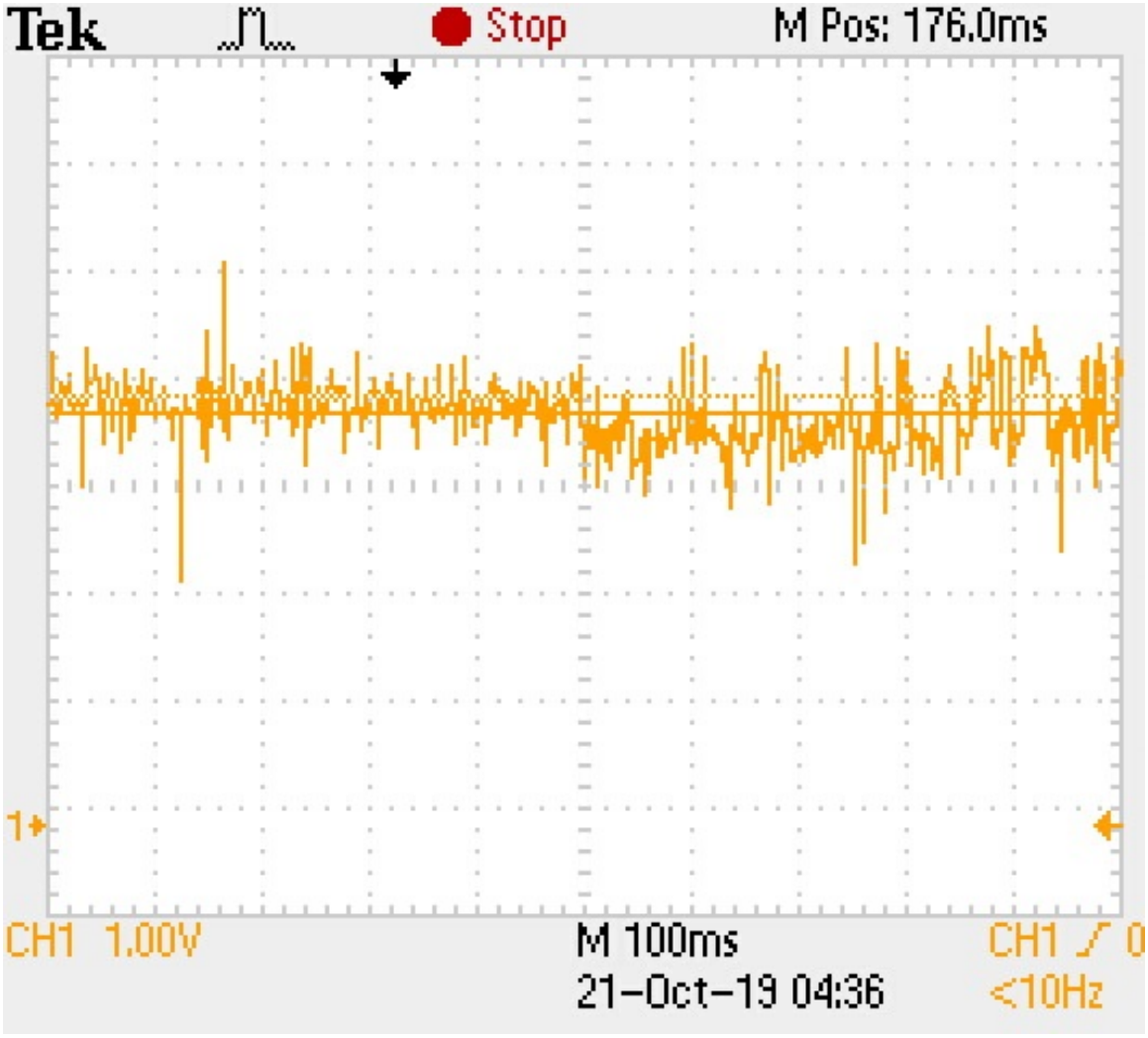

Figure 7.20: Step response of M_{vcl} as obtained on the test bench.

8 Conclusion

- Tapped-inductor buck dc-dc converter provides higher step down at the output voltage due to the presence of turns ratio in the tapped-inductor.
- This can help simplify higher stage for power conversion, utilizing a single stage instead of multiple conversion stages.
- The steady-state analysis of the pulse-width modulated (PWM) tapped-inductor buck dc-dc converter in continuous-conduction mode has been performed.
- The expressions to design the converter components and over all efficiency have been derived. There is a loss in efficiency due to the higher losses observed in tapped-inductor.
- An averaged small-signal model for a tapped-inductor buck dc-dc converter has been derived.
- The obtained small-signal model is used to derive the power stage transfer functions. It is observed that the control-to-output voltage transfer function has a right half plane zero, which is not present in a conventional buck dc-dc converter. This makes the controller is little more complex.
- An integral-double-lead controller for the voltage mode control has also been derived and implemented. All the theoretical expressions have been validated through MATLAB, saber circuit simulations and hardware implementation.

9 Future Work

This dissertation already provides the waveform of the converter during different time intervals, when the converter is running in DCM. This can be expanded upon by averaging the waveforms to obtain an averaged circuit model for the tapped-inductor buck dc-dc converter running in DCM. This should help eliminate the non-linear components in the circuit and thus making the characterization of the converter much simpler. Since a tapped-inductor has been implemented for storing the energy, a multi-output tapped-inductor buck can also be analyzed and implemented depending on the applications.

References

[1] M. K. Kazimierczuk, Pulse-Width Modulated DC-DC Power Converters. Wiley, 2015.

[2] Y. Kaiwei, Y. Mao, X. Ming, F. C. Lee, "Tapped-inductor buck converter for high-step-down DC-DC conversion" *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 775-780, Jul. 2005.

[3] R. D. Middlebrook, "A continuous model for the tapped-inductor boost converter," in *Proc. IEEE Power Electron. Specialists Conf.*, pp. 55-71, 1975.

[4] D. Maksimovič and S. Ćuk, "Switching converters with wide DC conversion range ," *IEEE Trans. Power. Electron.*, vol. 6, no. 6, pp. 151-157, Jan. 1991.

[5] A. Ayachit and M. K. Kazimierczuk, "Steady-state analysis of PWM quadratic buck converter in CCM," in *Proc. IEEE Midwest Symp. Circ. Syst.,* Columbus, USA, pp. 49-52, Aug. 2013.

[6] J. Wei, P. Xu, H. Wu, F. C. Lee, K. Yao, and M. Ye, "Comparison of three topology candidates for 12V VRM," in *Proc. IEEE Applied Power Electron. Conf.*, 2001, pp. 245-251.

[7] D. K. Saini, A. Ayachit, T. Salvatierra, and M. K. Kazimierczuk, "Design of zero-voltage-ripple buck dc-dc converter," in *Proc. IEEE Midwest Symp. Circ. Syst.,* Boston, USA, pp. 456-459, Aug. 2017.

[8] J. Lange, "Tapped inductor improves efficiency for switching regulator," *Electron. Design,* vol. 27, no. 16, pp. 114-116, Aug. 1979.

[9] D. A. Grant and Y. Darroman, "Extending the tapped-inductor DC-to-DC converter family," *Electron. Lett.*, vol. 37, pp. 145-146, Feb. 2001.

[10] J. Park and B. H. Cho, "The zero voltage switching (ZVS) critical conduction mode (CCM) buck converter with tapped-inductor," in *Proc. IEEE Applied Power Electron. Conf.*, 2003, pp. 1077-1081.

[11] D. Czarkowski and M. K. Kazimierczuk, "Energy-conservation approach to modeling PWM DC-DC converters," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 29, no. 3, pp. 1059-1063, Jul. 1993.

[12] N. Kondrath and M. K. Kazimierczuk, "Analysis and design of common-diode tapped inductor PWM buck converter," in *Proc. Electrical Manufacturing and Coil Winding Conf.*, Nashville, TN, Sept. 2009.

[13] A. Chadha, A. Ayachit, D.K. Saini, and M. K. Kazimierczuk, "Steady-state analysis of PWM tapped-inductor buck DC-DC converter in CCM," in Proc. *IEEE Texas Power and Energy Conf.*, College station, TX, Feb. 2018.

[14] B. Bryant and M. K. Kazimierczuk, "Voltage-loop power-stage transfer functions with MOSFET delay for boost PWM converter operating in CCM," in *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 347-353, Feb. 2007.

[15] B. Bryant and M. K. Kazimierczuk, "Voltage loop of boost PWM DC–DC converters with peak current-mode control," *IEEE Trans. Circ. Systems-I: Regular Papers,* vol. 53, no. 1, pp. 99-107, Jan. 2006.

[16] M. K. Kazimierczuk, "Transfer function of current modulator in PWM converters with current-mode control," *IEEE Trans. Circ. and Syst. I: Fundamental Theory and Applications*, vol. 47, no. 9, pp. 1407-1412, Sept. 2000.

[17] R. D. Middlebrook, "Topics in multiple-loop regulators and current-mode programming," *IEEE Trans. Power Electron.*, vol. PE-2, no. 2, pp. 109-125, Apr. 1987.

[18] F. D. Tan and R. D. Middlebrook, “A unified model for current-programmed converters,” *IEEE Trans. Power Electron.,* vol. 10, no. 4, pp. 397–408, Jul. 1995.

[19] R. Redl and I. Novak, “Instabilities in current-mode controlled switching voltage regulators,” in Proc. Power Electronics. Specialists. Conf., pp. 17-28, 1981.

[20] —, ”Small-signal duty cycle to inductor current transfer function for boost PWM dc–dc converter in continuous conduction mode,” in *Proc. IEEE Intl. Symp. Circ. Syst.,* Vancouver, BC, Canada, May 23-26, 2004, pp. 856-859.

[21] B. Bryant and M. K. Kazimierczuk, ”Open-loop power-stage transfer functions relevant to current mode control of boost PWM converter operating in CCM,” *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 52, no. 10, pp. 2158-2164, Oct. 2005.

[22] A. Ayachit and M. K. Kazimierczuk, “Small-signal modeling of PWM boost dc-dc converter at boundary conduction mode by circuit averaging technique,” in *IEEE Intl. Symp. Circ. and Syst.*, Lisbon, Portugal, May 2015, pp. 229-232.

[23] A. Ayachit and M. K. Kazimierczuk, “Open-loop small-signal transfer functions of the quadratic buck PWM dc-dc converter in CCM,” *IEEE Ind. Electron. Society Conf.*, Dallas, USA, November 2014, pp. 1643-1649.

[24] D. K. Saini, A. Ayachit, and M. K. Kazimierczuk, “Small-signal analysis of closed-loop PWM boost converter in CCM with complex impedance load,” in *IEEE Intl. Symp. Circ. and Syst.*, Montreal, Canada, May 2016, pp. 433-436.

[25] D. K. Saini, A. Ayachit, M. K. Kazimierczuk, and T. Suetsugu,“Small-signal analysis of PWM boost converter in CCM with complex impedance load,” in *IEEE Ind. Electron. Society Conf.*, Yokohama, Japan, November 9-12, 2015, pp. 3597-3602.

[26] A. Ayachit, Y. P. Siwakoti, V. P. N. Galigekere, M. K. Kazimierczuk, "Steady-state and small-signal analysis of a-source converter," in *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 7118-7131, Aug. 2018.