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Logistic Function based Nonlinear Modeling and Circuit Analysis of the Bipolar Vacancy Migration Memristor

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LOGISTIC FUNCTION BASED NONLINEAR MODELING AND CIRCUIT ANALYSIS OF THE BIPOLAR VACANCY MIGRATION MEMRISTOR

A dissertation submitted in partial fulfillment of the

requirements for the degree of

Doctor of Philosophy

by

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I HEREBY RECOMMEND THAT THE DISSERTATION PREPARED UNDER MY SUPERVISION BY Isaac P. Abraham ENTITLED Logistic Function based Nonlinear Modeling and Circuit Analysis of the Bipolar Vacancy Migration Memristor BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Doctor of Philosophy.

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ABSTRACT

Abraham, Isaac P., Ph.D., Electrical Engineering Ph.D. program, Wright State University, 2020. Logistic Function based Nonlinear Modeling and Circuit Analysis of the Bipolar Vacancy Migration Memristor.

Memristor is an acronym for **mem**ory **r**es**istor**. Memristors promise to be building blocks for high density memory and analog computation. Hewlett Packard's announcement in 2008 of having fabricated a memristor on an integrated circuit scale has created a tangible excitement in this field. Understanding and exploiting the full potential of these devices requires good compact models. Symbolic modeling provides a balance between achieving accurate empirical fit and generating closed form expressions. This dissertation simplifies the transport equation into a variable coefficient advection equation, very similar to a Burgers' equation traditionally used in fluid dynamics. The Burgers'-like model reveals the dual variable resistance initially proposed by HP that has served as a gold standard to date. The Burgers' model also shows the emergence of an active phenomenon within the device as some researchers have suspected. Results from this model are compared favorably with independent experimental data.

The insight obtained from this computational ion transport model is the motivation for proposing a simpler computational logistic function based memory resistance model. The logistic model is a solution to the well-known logistic equation and map. This relationship between functions and maps opens the door to understanding how the memristor can exhibit sensitivity to initial conditions as claimed by some researchers. The logistic model is validated by fitting to experimental data. The usability of the model in practical circuit design is demonstrated with a relaxation oscillator implemented in LTSpice. The oscillator implemented is power and reliability aware. A formal method to estimate the frequency of such a nonlinear circuit is presented. Computationally estimated frequency is validated against results from LTSpice. A variant of the oscillator is shown to function as a simple offset voltage detector. Unlike numerical methods, the symbolic, closed form approach in this dissertation provides an unparalleled perspective into the inner workings of the memristor. The peer reviewed, published findings of this research invalidate the claim that the memristor is a passive fundamental circuit element; an issue associated with the device since its inception.

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1 Introduction

A two terminal resistor that retains its prior programmed resistance is called a **mem**ory **r**es**istor**. The phenomenon is called nonvolatile memory effect. In contemporary electrical phraseology, resistance R is a phenomenological constant, defined as the ratio of voltage to current. The phenomenological constant associated with memory resistance is memristance M, defined as the ratio of electric flux to charge. Memristance is characterized by hysteresis in the device output characteristic curve. Hysteresis causes a specific stimulus to have two different responses depending on the direction of travel of the stimulus. Memristive hysteresis appears in voltage-current coordinates, not in the coordinates of the memristor's constitutive relation which are flux and charge.

1.1 Historical Hysteretic Devices

The modern memristor was postulated as a theoretical fundamental device by Leon Chua in 1971 [1]. However, the phenomenon of memristance has been observable in electrical experiments from approximately two hundred years ago. Prodromakis et al. survey a detailed collection of historical examples ranging from vacuum tubes, mercury vapor lamp, silver sulfide-based thermistors and the voltaic pile [2]. Fig. 1.1 shows a sample from Prodromakis' survey.

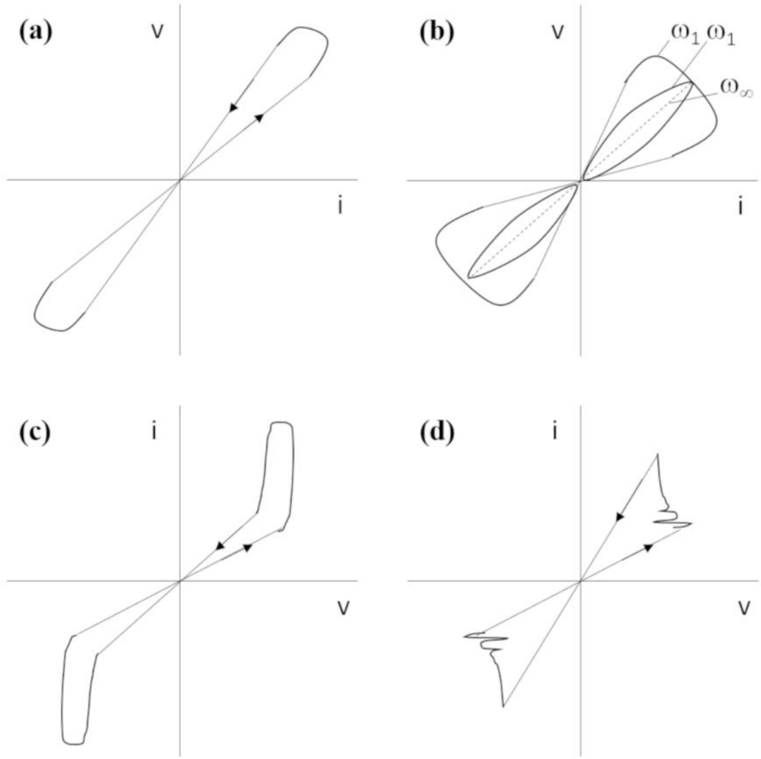

Fig. 1.1 Memristive current-voltage curves over the centuries.

Fig. 1.1 shows a variety of bipolar current-voltage (I-V) response curves transcribed from historical literature into the review in [2] and other referenced documents. Panel (a) shows a tungsten filament I-V curve as reproduced in [2] from the original textbook "Fundamentals of Discharge Tube Circuits" by V. J. Francis. Panel (b) shows Chua's conceptual I-V curves with frequency dependence as mentioned in [3]. Panel (c) is Argall's experimental titanium oxide I-V curves from [4] and panel (d) shows Williams et al. demonstrating simulated and experimental I-V curves in [5].

If a pinched hysteresis curve is the signature of memristance, then it is also observable in natural phenomena. The analemma curve which plots the year-round position of the sun from a fixed geographical location and time looks very much like the bow-tie or pinched hysteresis curves described above [6]. For a memristor this signature bowtie or pinched hysteresis I-V curve is generated with a sinusoidal input applied to the two terminal memristor device.

1.2 Contemporary Hysteretic Devices

1.2.1 Pre Hewlett-Packard

A more modern and often referenced experimental work that reveals memristive characteristics in thin films is Argall [4]. Argall's paper shows bowtie I-V curves generated with anodized titanium dioxide film and copper electrodes. Switching is induced by voltage cycling. Within three years in 1971 Chua published the theoretical framework to the memristor, proposed a device symbol and set forth the basic abstract equations that should describe any memristive device [1]. Chua and Kang later generalized the notion of memristance to memristive systems [7]. The common, recurring idea among all memristive systems is that the hysteretic effect of the memristive system decreases as the frequency increases and hence it eventually degenerates into a purely resistive system without memory.

1.2.2 The Hewlett Packard Memristor

The lull in memristor research since 1971 ended when researchers at Hewlett Packard (HP) announced finding the missing memristor in their seminal paper [5]. The paper expounds on experimental results from using a titanium dioxide thin film. The titanium dioxide in proximity to the contacts was found to split into two layers, namely an oxygen deficient layer of TiO_{2-x} and stable TiO_2. The oxygen deficient titanium dioxide layer functions as a donor of electrons while the positive oxygen ions (O^{2+}) are the mobile vacancies. The associated I-V curves exhibit hysteresis along with bipolar switching. Bipolar switching requires voltage reversal to return the device to a prior state. The authors propose an ohmic electronic conduction model where linear ionic drift in a uniform field controls the device resistance. This first abstract circuit model has series dual variable resistors as sketched in Fig. 1.3 (b). In late 2008, Williams writes in the IEEE Spectrum detailing the experimental search for the (till then) "mythical" memristor [3]. The article in Spectrum visualizes memristors in the role of nonvolatile memory elements and two-state field programmable gate arrays with reduced area and lower power.

1.3 Structure and characteristic

1.3.1 Physical structure

The memristor has a metal-insulator-metal (MIM) structure [3], [8]. The metal end plates form the device terminals. The end plates at each end can be made of different materials and dimensions. The plates serve as the boundary to the "insulating" sandwich. The "insulator" is the chemical that contains the mobile vacancies. The word insulator is used only to help compare the memristor to a MIM structure. The chemical species between the plates conducts electronic current. Titanium dioxide [9], copper oxide [10], nickel oxide [11] etc. are used to form this chemical sandwich. Experimentalists work with end plates of various sizes to investigate the impact of area, surface roughness etc. on the memristor characteristic. The thickness of the sandwich is yet another variable that has a large range. Memristors in literature can range from 500nm [12] down to about 50nm [3] or even 30nm [13]. The theoretical limits might be around 10nm according to Strukov [5]. Fig. 1.2 shows a cartoon of the ion migration under the action of an applied external voltage.

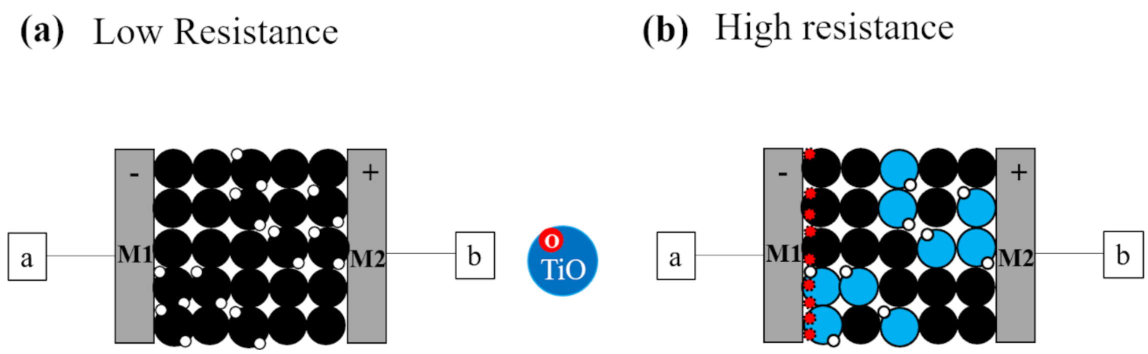

Fig. 1.2 Free ion migration determines device resistance.

In Fig. 1.2 (a), the device is in low resistance. The metal end plates are marked M1 and M2 and associated with device terminals a and b respectively. The large black circles are the neutral TiO_2; where the oxygen atoms are shown as white circles hugging the outline of the black circles. From experiments it is known that only a small fraction of TiO2 can generate free oxygen ions. Hence Fig. 1.2 (a) shows only some of the TiO2 with their oxygen bonds – ready to break free.

In Fig. 1.2 (b) a voltage is applied between the pins a and b. From each of the previously identified TiO2 locations, one positively charged oxygen ion breaks away. This leaves behind a blue-colored negatively charged but immobile TiO. The attached oxygen is shown as a white circle. The mobile positive oxygen ions are shown with a dotted red circle. These ions have drifted to the negative plate of the device. Strukov identifies the oxygen as positively charged [3]. This is also easily verified with an electron shell diagram. Electrons attempting to transit the chemical species now face a large negative field of TiO. The distribution profile of the positive and negative ions determines the device resistance.

1.3.2 Bipolar switching

Bipolar implies the need for a positive and negative voltage across the memristor to program and reset the device. Fig. 1.3 shows the I-V and circuit model.

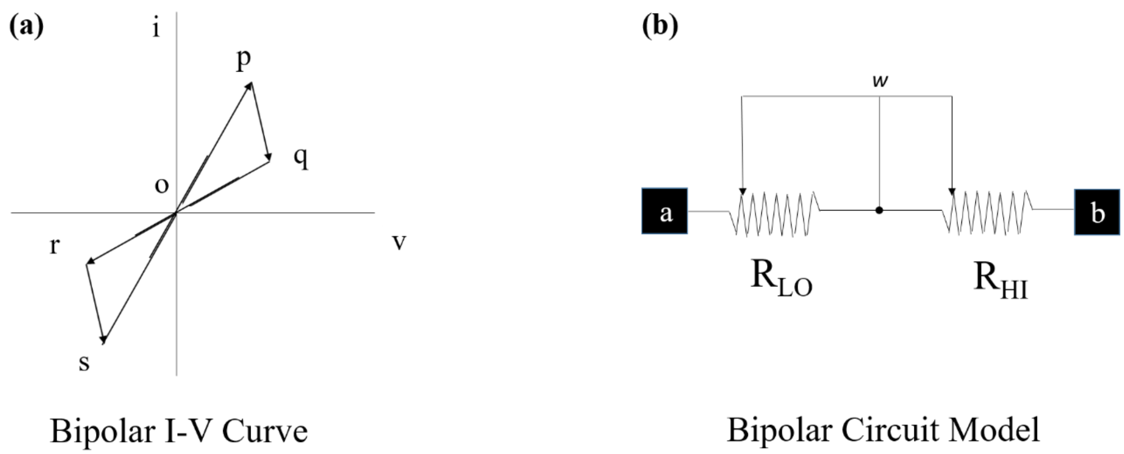

Fig. 1.3 The bipolar (a) I-V curve and (b) rheostat model *[5]*.

Fig. 1.3 (a) shows the I-V curve of the bipolar memristor. When the input voltage is zero, response current is also zero; suggesting that there is no permanent energy storage or generator element within. Assuming the device was parked in the low resistance state, the curve traces **o-p** where it switches to the high resistance state along **p-q**, with lower current. When the stimulus voltage is reduced, the current traces back to the origin along **q-o**. If the voltage were to increase without an excursion to the negative voltage, the current will be low and trace back and forth along **o-q**. The device will never exit the high resistance state if the polarity of the voltage does not reverse. When the applied voltage traverses to the negative, the current will trace **o-r** and eventually switch to the low resistance state along **r-s**. When the voltage increases to zero and crosses over to positive, the locus traces **s-o-p**.

In short, a bipolar memristor can only switch states while transiting the origin, into quadrants one or three.

The popular and accepted model for the memristor was proposed by HP's Strukov and Williams. A sketch is shown in Fig. 1.3 (b). The discussion associates (R_{LO}, R_{HI}) with (R_{ON}, R_{OFF}). The input and output pins are labeled **a** and **b**. The two terminal model has two resistors R_{ON} and R_{OFF} with a short-circuiting slider in between. The slider can short circuit R_{ON}, R_{OFF} or parts of both emulating resistance switching between the low R_{ON} and high R_{OFF}. The variable *w* associated with the slider indicates the time dependent state variable that stores information about the positioning of the slider, which in turn determines the device resistance.

1.3.3 Fingerprints of the Memristor

Adhikari and Chua have codified a set of three simple qualities to identify memristive behavior [14]. The sketched Fig. 1.2 (b) exhibits all the three fingerprints stated below.

1.3.3.1 Fingerprint 1: Pinched hysteresis loop

A pinched hysteresis loop is defined as one that passes through the point (v, i) = (0, 0). The pinched at the origin phenomenon is universal to all memristors independent of the stimulus applied to the device. This definition requires that the device cannot store energy. All the plots in Fig. 1.1 exhibit pinched hysteresis.

1.3.3.2 Fingerprint 2: Hysteresis loop area is inversely proportional to frequency

A memristor will exhibit shrinking lobe area as the frequency of excitation increases. The reason for this is that with increasing excitation frequencies, the mobile ions do not depart from their initial positions farther enough to enter a higher or lower resistance state. Fig. 1.1 (b) shows the lobe area shrinking with increasing excitation frequency.

1.3.3.3 *Fingerprint 3: Pinched hysteresis loop shrinks to a single valued function at infinite frequency*

Fingerprint 3 is a follow-on to fingerprint 2. When the excitation frequency is very high, the I-V curve resembles a line without any lobe. This line may be linear or nonlinear. Fig. 1.1 (b) shows the case where the collapsed lobe is linear.

1.4 Memristors and Computing

Memristors are potential candidates to implement high density, low power and nonvolatile memory elements. In memory circuits, a logic “1” or “0” can be stored as a high or low resistance. Some research is focused on crossbar structures composed of hybrid CMOS/memristor circuits; although most studies generally focus on single memristors. This is starting to change with more researchers experimenting with their own choice of differently sized end plates and sandwich materials integrated into arrays.

Logic applications are an area of interest for researchers. Field Programmable Gate Array (FPGA) circuits may benefit from storing the microprocessor circuit configuration before powering down or to assist recovery, in a smaller and lower power memristor array rather than a traditional flash memory or static random access memory (RAM) [15]. Batas and Fiedler present a digital AND circuit using only memristors [16].

The use of hysteretic devices for analog computing can be traced to the 1960s. Memristors can implement the resistance switching component in mixed signal computing [15] and artificial neural networks [17]. Arithmetic operations can also be performed with device conductance representing the quantities being operated upon [18], [19]. An appropriately mature device model is desirable to support circuit design for such applications.

1.5 Survey of Models

An understanding of the current state of memristor modeling is essential for placing this dissertation's symbolic model in context. Modeling can be broadly classified as discrete and continuous time. Each of these major categories may have uniquely distinguishable methods as sub categories.

1.5.1 Discrete Time

1.5.1.1 Piecewise

An early piece wise linear (PWL) model proposes to define the important segments of the Lissajous figure (or the bowtie curve) as straight lines. The result is an ideal bowtie [20]. Itoh and Chua present chaotic circuits based on PWL models in [21]. The main topic in that paper is bifurcation and chaos rather than the modeling aspect itself. Nevertheless, it develops on PWL modeling that Chua originally proposed in [1]. PWL models are not very interesting in themselves. However, they are easy to use, very suitable for modeling two-state circuit behavior and have low computational complexity.

1.5.1.2 Numerical

Traditional numerical models rely on solving a problem by discretizing fundamental equations and solving them based on initial and boundary conditions. Most real-life problems are only tractable in this way. Numerical solutions however do not provide a closed form solution to readily reveal the characteristics of the device. Closed form or symbolic solutions are computable expressions. A thorough numerical study on memristive phenomenon is presented by Nardi et al. in [22] and [23]. Part I [22] presents the empirical data collected by the authors. Part II [23] creates a numerical model that is used to fit the experimental data. The drift-diffusion equation, Arrhenius law, Einstein relation and the steady state Fourier equation are solved self-consistently using numerical methods, leading to dopant density, temperature and potential maps. The authors show relatively good agreement between modeling and the experiments. Each numerical simulation is just that one simulation. The user will have no idea about how a device state will evolve under different input conditions, unless a suite of simulations is performed under varying conditions.

1.5.2 Continuous Time

Continuously differentiable ordinary differential equations (ODE) are also used for memristor modeling. Many ODE models can only be solved numerically even if their governing equations are specified in continuous time. Inclusion in this section does not imply that a closed form solution exists.

1.5.2.1 The HP model

This commonly referenced memristor model is the dual variable resistor (DVR) model from HP [5]. It has closed form solutions. Their model consists of two series connected resistors and a slider that short circuits portions of the two resistors. Fig. 1.4 relates vacancy migration to resistance. The black circles are stable TiO_2. The blue circles depict negatively charged, immobile TiO. Positively charged oxygen vacancies are depicted in red dots.

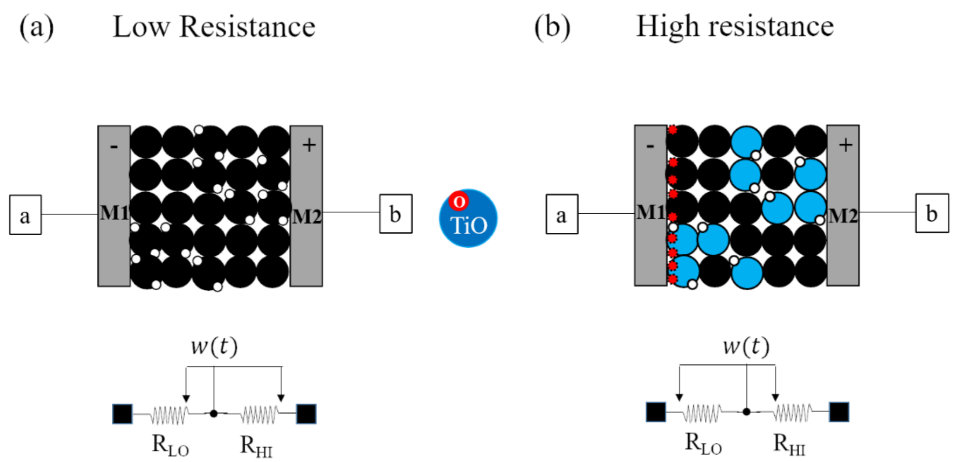

Fig. 1.4 Vacancy migration and dual variable resistance.

Fig. 1.4 (a) shows a cartoon of the vacancy distribution in the top panel along with the low resistance state of the device in the lower circuit diagram. In Fig. 1.4 (b), the vacancies have migrated to one end of the device and the associated circuit diagram shows the rheostat in its high resistance state. The DVR is an improvised circuit abstraction and does not reveal any specifics about vacancy dynamics. The presence of these two resistances cannot be inferred from the solution to HP's governing equations [5]. Equation (1-1) is an algebraic relation and it cannot be solved without the simple ODE in (1-2).

$$v(t) = \left(R_{ON} \frac{w(t)}{d} + R_{OFF} \left(1 - \frac{w(t)}{d}\right) \right) i(t) \tag{1-1}$$

$$\frac{dw(t)}{dt} = \mu_V \frac{R_{ON}}{d} i(t) \tag{1-2}$$

In (1-1) and (1-2),

$v(t)$ is the time dependent voltage across the device,

R_{ON} and R_{OFF} are the low and high resistance,

$w(t)$ is the time-dependent position of the slider representing the boundary between the ion-rich and ion-poor regions of the device,

d is device length,

$i(t)$ is the time-dependent current in the device and

μ_V is the mobility of the vacancies or ions.

The original HP model (1-2) assumes a linear movement of the rigid boundary between device regions that have different vacancy concentrations. Integrating (1-2) with respect to (w.r.t) time t results in $w(t)$ in terms of charge $q(t)$.

$$w(t) = \mu_V \frac{R_{ON}}{d} q(t) \tag{1-3}$$

Inserting (1-3) into (1-1) results in the equation for memristance. Assuming $\mathrm{R_{ON}} \ll \mathrm{R_{OFF}}$, equation (1-1) simplifies as follows.

$$M(q) = R_{OFF} \left(1 - \mu_V \frac{R_{ON}}{d^2} q(t)\right) \tag{1-4}$$

Equation (1-4) is used by many authors to show memristive characteristics. It is a simplification that presents memristance as a function of charge which is in turn a function of time. The presence of time varying charge in (1-4) makes it inconvenient for manipulation in circuit design. Therefore, a solution relating memristance to voltage as a forcing function is desired.

Writing $q(t) = \int i(t)\, dt$, (1-4) becomes $M(t) = R_{OFF} \left(1 - \mu_V \frac{R_{ON}}{d^2} \int i(t)\, dt\right)$. Differentiating each side w.r.t time,

$$\frac{dM(t)}{dt} = -\frac{\mu_V R_{ON} R_{OFF}}{d^2} i(t) = -\frac{\mu_V R_{ON} R_{OFF}}{d^2} \frac{v(t)}{M(t)}. \tag{1-5}$$

This is equivalent to a first order nonlinear ODE of the form $y\, y' = -k\, f$; where y is the desired solution, f is the stimulus, both are functions of time and k is a constant [24].

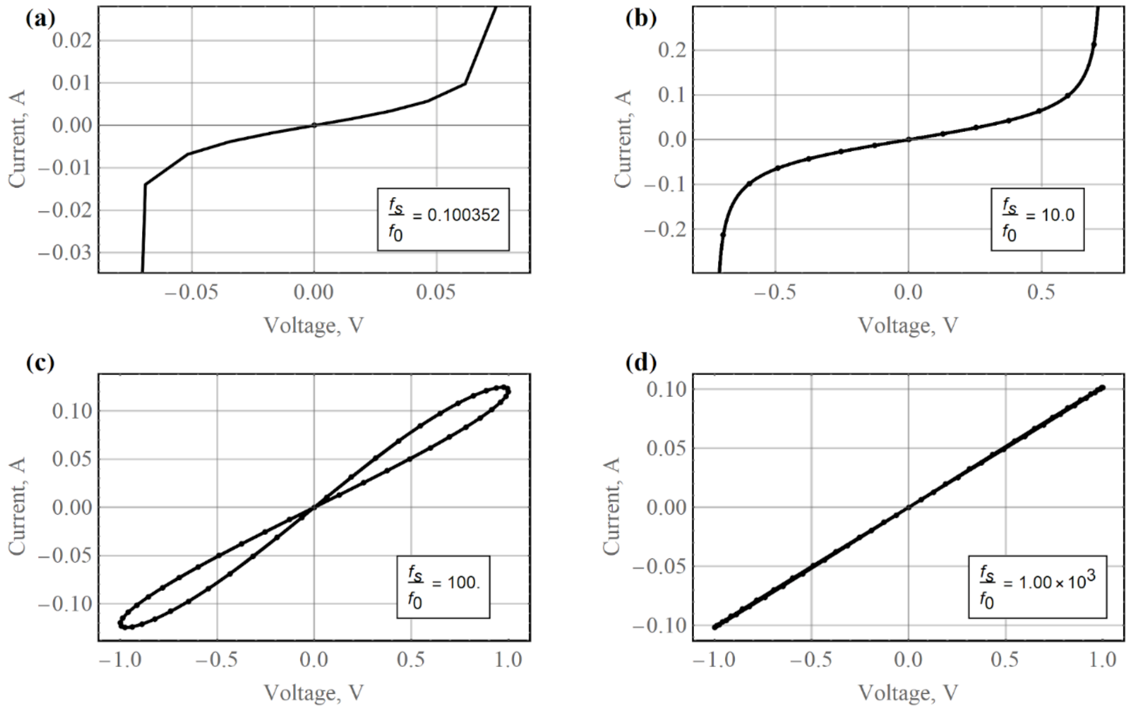

Fig. 1.5: HP model response.

For $v(t) = \sin(\omega\, t)$, the solution to (1-5) is

$$M(t) = \pm\sqrt{\frac{M(0)^2\, \omega + 2\, k\, cos(\omega\, t) - 2\, k}{\omega}}. \tag{1-6}$$

In (1-6), $M(0)$ is known from design or calibration of a product and $k = \frac{\mu_V\, R_{ON}\, R_{OFF}}{d^2}$. Consider the response from the HP model using (1-6) as shown in Fig. 1.5. The plots were generated using an arbitrary $\mu_V = 10^{-14}\, \frac{m^2}{V\, s}$, $R_{ON} = 10\Omega$, $R_{OFF} = 1\ k\Omega$, $d = 32\ nm$ and a forcing function $v(t) = \sin(\omega\, t)$. Under these conditions the natural frequency of the device is estimated to be $f_0 = \frac{\mu}{d^2} = 9.77\ Hz$. Each panel of Fig. 1.5 is generated at a fraction $\frac{f_s}{f_0}$ of the device natural frequency; where f_s is the stimulus frequency. Fig. 1.5 (a) shows that when the stimulus frequency is smaller than the natural frequency, the I-V lobe is incorrectly collapsed. There is no significant change in Fig. 1.5 (b) when the stimulus is an order of magnitude larger. Fig. 1.5 (c) shows that the lobe size has incorrectly increased when the stimulus is 100-times the device natural frequency. It is impossible for the lobe to appear as stimulus frequency increases; this contradicts fingerprint 2. In Fig. 1.5 (d) at 1000-times the device's natural frequency, the I-V curve has correctly collapsed to a straight line. In addition to these mixed correct and incorrect responses, the device model transitions from a collapsed nonlinear resistor at very low frequencies to a collapsed linear resistor at very high frequencies. This transition from linear to nonlinear is unexpected and incorrect.

Meuffels and Soni [25] present a strong case for why the modeling in [5] is insufficient in describing a real system. The authors point out that the notion of a rigid boundary between two regions with sparse and dense vacancies is conceptually weak. They also object to the idea of a linearly moving boundary, although Williams and Strukov circumvent the non-ideality by subsequently employing window functions to modify the movement of the boundary toward the device ends.

Window functions are arbitrary polynomials that modulate the equation for accumulation boundary movement, such that the boundary slows down and asymptotically approaches the end plates of the memristor. Window functions come in many forms. The expression $f(w) = w(1-w)/d^2$ [5] is HP's version of a windowing function. Here variable w is a function of time as in $w(t)$. Joglekar et al. propose $f(w) = 1-(2w-1)^{2p}, p \geq 1$ [26]. Biolek uses $f(x) = 1-(x-\mathrm{stp}(-i))^{2p}, p \geq 1$ with a step defined as $\mathrm{stp}(i) = \begin{cases} 1, & i \geq 0 \\ 0, & i < 0 \end{cases}$ [27]. Corinto et al. discuss a Boundary Condition Model (BCM) that uses HP's basic model, modulated by a variety of window functions [28]. The resulting model almost always can only be solved with numerical methods.

Publications [28], [29] and [30] that promise a symbolic approach invariably uses HP's basic equation paired with HP's-own window functions or that of Joglekar; providing no originality and are solved numerically. Without the manual insertion of nonlinearity, the raw HP model exhibits inconsistent behaviors presented in Fig. 1.5.

Nonetheless equations (1-1) and (1-2) satisfy Chua's definitions for a general memristive system and the ideal generic memristor. The generalized equations are shown below in (1-7) and (1-8) [5].

$$v(t) = R(w(t), i)\, i \tag{1-7}$$

$$\frac{dw(t)}{dt} = f(w(t), i) \tag{1-8}$$

1.5.2.2 The shockwave model

The shockwave model approaches modeling with a generalization of the Burgers' equation [31]. In (1-9), u is mobile ion concentration, D is diffusion coefficient and $f(u)$ is the concentration wave velocity as a function of ion concentration.

$$\partial_t u + f(u)\, \partial_x u = D\, \partial_{xx} u \tag{1-9}$$

Important assumptions in (1-9) are that nonlinear drift dominates diffusion, transverse currents are neglected and local resistance is a function of vacancy concentration. The ideas presented by Tang et al. result in a sharp and discontinuous shock wave front. However, this is at variance with the smoother sigmoid type vacancy evolution that Waser has presented in his surveys [12]. Similarly a discontinuous front is the very objection raised by Meuffels and Soni. This shockwave model therefore serves to demonstrate that even among symbolic methods that seem similar there can be differences in how vacancy profile evolves; yet all of them exhibiting memristive qualities. Tang et al. observe the quadratic dependence of switching speed to device length and the existence of two distinct temporal phases during switching.

1.6 Objectives of Dissertation

The objectives of this dissertation are as follows.

- Develop a simplified transport-based differential equation and symbolic solution. The simplified governing differential equation is the variable coefficient advection (VCA) equation. The VCA, its solution and inferences will be referred to as the computational ion transport model.
- Validate the computational model against independent experimental data. The computational model is further simplified to a form suitable for implementation in the Simulation Program with Integrated Circuit Emphasis (SPICE) and used in circuit simulations.
- Associate the computational ion transport compact model with a computational logistic differential equation (LDE). The LDE and its solution will be referred to as the logistic model. The LDE will be implemented in SPICE and used in circuit simulations.

- Use the computational and logistic models to tackle fundamental issues with the definition of the memristor. This dissertation examines if the memristor can be a fundamental passive circuit element.

The units in this dissertation adhere to the SI units [32].

1.7 Organization of Dissertation

The dissertation is organized as follows.

- Chapter 1 is this chapter which serves as an introduction to the topic of memristors. It contains a survey of contemporary models. This sets the background for the state of the art in the field and places this dissertation in context. Chapter 1 also details the objectives and organization of this dissertation.
- Chapter 2 presents the derivation that transforms the basic transport equation into a variable coefficient equation and presents a symbolic solution. The computational model is used to derive a variety of expressions that demonstrate memristive characteristics. The output of the model is compared against empirical results from independent researchers.
- Chapter 3 associates the computational ion transport model with the computational logistic equation. Memristive characteristics are demonstrated with the logistic model.
- Chapter 4 demonstrates SPICE circuit simulations using the computational and logistic model. A relaxation oscillator that is unique to this dissertation is presented.

Simulations that explore the scope and versatility of the logistic model are presented and discussed.

- Chapter 5 is a review of fundamental findings from this research. This chapter reviews the memristor in the context of the three existing fundamental passive elements namely the resistor, capacitor and inductor. Our findings are demonstrated to be comparable with that of independent researchers. Significant findings that are divergent from the view of some researchers in the memristor community are explained clearly. Such findings are also published in high quality journals.
- Chapter 6 concludes this dissertation and suggests future work.

1.8 Chapter Summary

The memristor is not an invention [2]. It belongs in the class of devices that exhibit a transient lag between applied stimulus and response or cause and effect. The contribution by the researchers at HP is the repeatable rendering of the phenomenon at the nanometer scale. Memristors may find application in implementing binary memory, logic and analog functions. Each application area is nascent and holds potential for discovery and innovation. The progress in each field however will depend on the availability of satisfactory models that can used with the tool suites appropriate for each field. Memristor device modeling is mostly incremental fine-tuning of the HP model with few other original approaches. This dissertation models the memristor with a single governing PDE. The results are abstracted to a logistic functional form. Memristor based computing is explored mathematically and in SPICE, using both the VCA model, its derived simplifications and the logistic model.

2 Computational Ion Transport Model

This chapter presents a simplification to the transport partial differential equation (PDE), resulting in the VCA PDE and a symbolic solution. The solution is validated by back-substitution into the PDE. The discussion in this chapter is substantially drawn from [33] and [34], where we first reported the development and evaluation of this technique.

2.1 Memristor Life Cycle

Prior to deriving a computational transport model, Fig. 2.1 shows a proposed memristor life cycle. This is the framework for understanding the main ion evolution mechanisms considered in this dissertation.

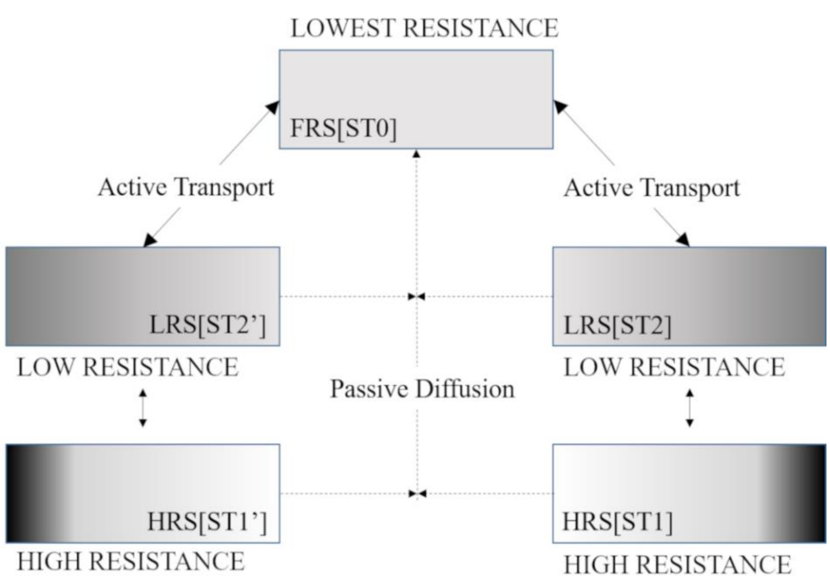

Fig. 2.1 Memristor life cycle.

Consider a device in its fresh and lowest resistance state FRS (ST0). The application of a programming voltage causes the vacancies to migrate either left or right. This results in mirror symmetric states ST[1, 2] and ST[1', 2']. The highest possible resistance along either path is ST1 (or ST1'). State ST2 (or ST2') is some intermediate low resistance state. The mechanism that motivates programming is active transport in the presence of an electric field.

When a programmed device is left on the shelf for an extended time period, the ions naturally diffuse throughout the volume of the device. This passive diffusion is shown in dotted lines. Passive diffusion occurs from regions of high ion concentration toward regions of low ion concentration without any external voltage.

2.2 Definitions

Consider a one-dimensional model of an ideal memristor to be a MIM sandwich with thickness d m. Let the ion concentration at any point within the sandwich be represented by u m^{-3}. This is visualized in Fig. 2.2 which can locate an arbitrary distance along the device length on the x-axis and space time dependent ion concentration along the y-axis.

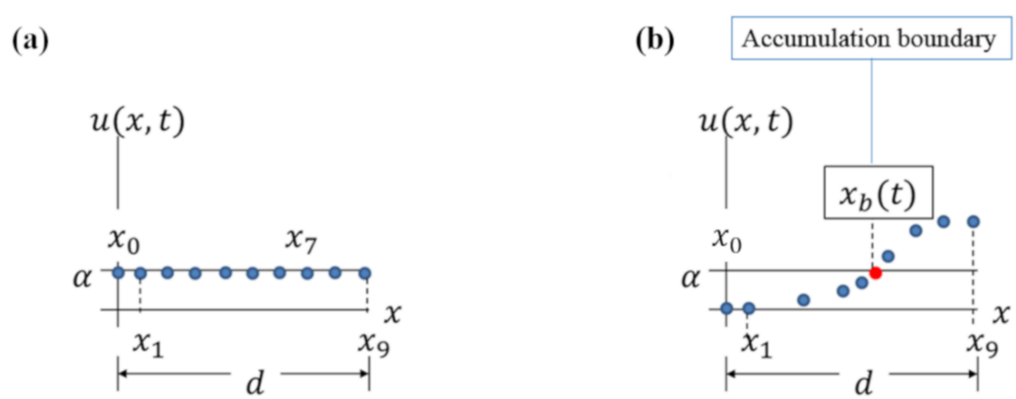

Fig. 2.2 Model of ion migration in the memristor.

Fig. 2.2 (a) shows the device in its low resistance state and has an equal concentration α at all positions. Fig. 2.2 (b) shows the same device after the ions have evolved in the presence of an applied voltage. This evolution profile is qualitatively consistent with the expectation from Williams [3], Waser [12] and Tang [31] among others. The new feature in Fig. 2.2 (b) is the labeled location $x_b(t)$. This is the boundary that separates the ion-rich from the ion-poor region of the memristor; alternatively referred to as w in Williams and Strukov's works. Fig. 2.2 (b) shows that this point always has a concentration equal to the initial distribution α. An expression is later derived to compute the location of $x_b(t)$.

To account for ion migration, let the mobility of the positively charged ions be uniform within this cross-section and represented by μ m^2s^{-1}/V. Ion velocity in the presence of a voltage V will be represented by the Greek character upsilon, υ m/s. The derivation of the simplified VCA PDE follows.

The key assumptions in the derivation are,

- vacancy and electric field are uniform within the device and
- vacancies do not exit the device boundaries.

2.3 Governing Variable Coefficient Advection PDE

2.3.1 Model derivation

Consider the basic transport equation which models the movement of particles under the action of an applied stimulus.

$$u_t + (\upsilon\, u)_x = 0 \qquad \text{(2-1)}$$

In (2-1) all variables are functions of (x, t). Subscripting indicates taking the derivative w.r.t the specified subscript. From Fig. 2.2 it is observed that the concentration u depends on the distance of a location x from the accumulation boundary $x_b(t)$. Therefore, apply the transformation $u(x,t) \rightarrow u\big(x - x_b(t)\big)$ and $v \rightarrow v\big(x - x_b(t)\big)$ and operate.

$$\left(\frac{\partial}{\partial t} + \frac{\partial}{\partial x} v\big(x - x_b(t)\big)\right) u\big(x - x_b(t)\big) = 0 \tag{2-2}$$

$$\frac{\partial}{\partial t} u - x_b'(t) \frac{\partial}{\partial x} u + v \frac{\partial}{\partial x} u + u \frac{\partial}{\partial x} v = 0 \tag{2-3}$$

$$u_t + \big(v - x_b{}'(t)\big) u_x + u\, v_x = 0 \tag{2-4}$$

$$u_t + \vartheta\, u_x + u\, v_x = 0 \tag{2-5}$$

The velocity of the traveling point with constant concentration is termed the characteristic velocity [35]. Applying the transformation $\big(v - x_b'(t)\big) \rightarrow \vartheta$,

$$u_t + \vartheta\, u_x + u\left(\boldsymbol{\vartheta} + \boldsymbol{x_b'(t)}\right)_x = 0. \tag{2-6}$$

$$u_t + \vartheta\, u_x + u\, \vartheta_x + u\, x_b'(t)_x = 0 \tag{2-7}$$

Since $x_b(t)$ is a function only of time, $x_b'(t)_x$ must equal zero. The fourth term of (2-7) is eliminated.

$$u_t + \vartheta\, u_x + u\, \vartheta_x = 0 \tag{2-8}$$

Equation (2-8) has two unknowns u and ϑ. One of the unknowns must be known to find the other. If the third term is retained, there is no symbolic solution. Assume for the moment that $u\, \vartheta_x$ is insignificant compared to the first and second terms giving the simplified PDE.

$$u_t + \vartheta\, u_x = 0 \tag{2-9}$$

The experimental and theoretical work of Williams [5], Waser [12], Larentis [23], Biolek [30] and Tang [31] suggest that a sigmoidal function can satisfy the ion evolution profile.

2.3.2 Solution

In order to develop intuition about the structure of the solution, consider the sample equation $u_t + \vartheta\, u_x = 0$ with $\vartheta = (x/t)$. One solution among many others is $u(x,t) = 1/(1 + e^{-x/t})$. This form is chosen for its ability to demonstrate a sigmoidal temporal ion evolution. Since it resembles a Heaviside step function [36], the mobility μ and electric field E are used to modulate the slope of the sigmoid. The $\left(x - x_b(t)\right)$ term models the movement of the ion boundary. The structure of the solution was inferred from the representation of the Heaviside step [36] and the sigmoid function [37].

$$u(x,t) = \frac{1}{1 + a\, e^{-\frac{1}{d}\mu E\left(\frac{x - x_b(t)}{d}\right)t}} \tag{2-10}$$

In (2-10),

a is a constant that can be evaluated from initial conditions,

d is the device length,

μ is ion or vacancy mobility in $m^2 v^{-1} s^{-1}$,

E is the electric field within the device, defined as voltage per unit device length v/d,

x is any location within the device,

$x_b(t)$ is the moving ion boundary and

t is time.

Defining electric flux $\phi = \int_{t=0}^{T} v(t)dt$, the solution can be expression in its normalized form where concentration is $0 \le u \le 1$ and $0 \le n \le 1$ with $n = \frac{x}{d}$, the normalized distance.

$$u(n,t) = \frac{1}{1 + a\, e^{-f_0\, \phi\, (n - n_b(t))}} \tag{2-11}$$

2.3.3 Error term

From (2-8), the characteristic velocity is constrained to always obey $\vartheta = -(u_t/u_x)$. With the expression for u from (2-10), an expression for characteristic velocity can be found using basic rules of differentiation.

$$\vartheta = x_b'(t) + \frac{x_b(t)-x}{t}. \tag{2-12}$$

From (2-12) it is clear that when the reference point $x = x_b(t)$ then the characteristic velocity is $\vartheta = x_b'(t)$ as expected. Therefore, the proposed approximate PDE in (2-9) can represent ion-migration accurately for an observer located at the accumulation boundary $x_b(t)$.

The third term in (2-8) that has been ignored in the simplification is the single, quantifiable source of error. Fig. 2.3 visualizes the exact and approximate model regions for the PDE in (2-9). The governing equation (2-9) models the ion-boundary exactly. The evolution of ions around the ion-boundary will be approximate.

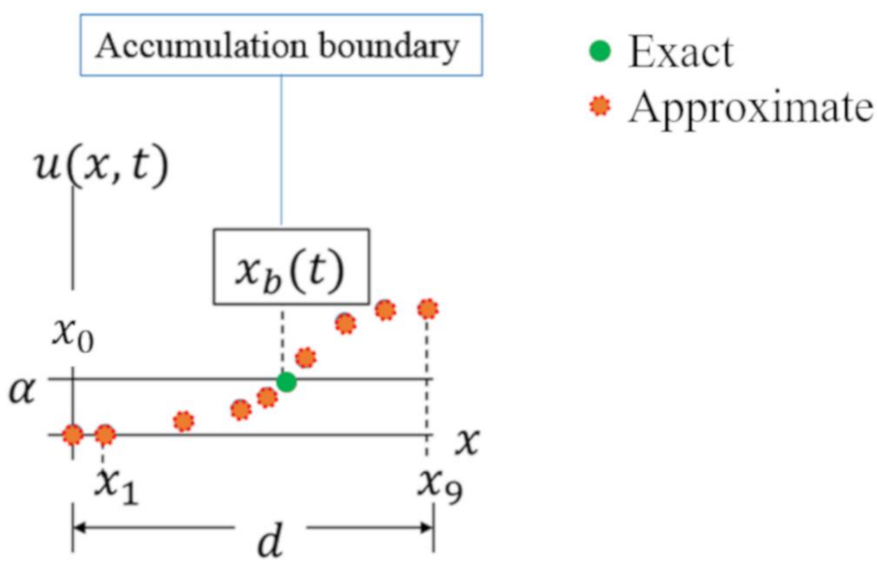

Fig. 2.3 Exact and approximate regions of vacancy evolution.

With the expression for ϑ from (2-12), the error (third) term can be deduced as,

$$u\,\vartheta_x = -\frac{u}{t}. \tag{2-13}$$

The error term becomes small for any reason that causes simulation time to be large such as,

- large device length,
- low ion mobility or
- low programming voltage.

The first two conditions can be enforced through manufacturing restrictions and the third can be achieved by limiting test voltage.

2.3.4 Solution verification

This sub section verifies the proposed solution (2-10) in the context of the PDE (2-9). Constants are also evaluated by using known initial and boundary conditions.

2.3.4.1 Determining a

It is known that $u(x, 0) = \alpha$; which is a fundamental assumption in the derivation. The flux or integral of programming voltage is zero. Substituting this information into (2-10) produces $u = \left(1 + a\, e^{-f_0\, 0\,(n - n_b(t))}\right)^{-1}$ which can be equated to α.

$$\alpha = \frac{1}{1+a}. \tag{2-14}$$

$$a = \frac{1-\alpha}{\alpha} \tag{2-15}$$

2.3.4.2 Boundary conditions

The boundary condition requires that at $t \to \infty$, the ions should accumulate toward an end plate, yielding zero at the evacuating side and the maximum normalized concentration of unity at the accumulating side. Equation (2-16) checks the ion concentration at infinite time at the evacuating (left) side of the device and (2-17) evaluates ion concentration at the accumulating (right) side of the device.

$$u(0,\infty) = \frac{1}{1+a\,e^{-f_0\infty\left(0-n_b(t)\right)}} = \frac{1}{1+a\,e^{\infty}} = 0 \tag{2-16}$$

$$u(1,\infty) = \frac{1}{1+a\,e^{-f_0\infty\left(1-n_b(t)\right)}} = \frac{1}{1+a\,e^{-\infty}} = 1 \tag{2-17}$$

The boundary conditions stand validated.

2.3.4.3 Dimensionality

The dimensions check ensures that the expression for the solution is balanced and unitless in this case. Assigning dimensions within square brackets as is convention and with reference to (2-11),

$$u(n,t) = \frac{1}{1+a\,e^{-f_0\phi\left(n-n_b(t)\right)}} = \frac{[\quad]}{[\quad]+[\quad]e^{-[v^{-1}s^{-1}][v\,s][\quad]}} = [\quad]. \tag{2-18}$$

The solution is dimensionless as expected.

2.3.4.4 Back substitution

Back substitution is guaranteed to pass because of the modeling approach that the characteristic velocity ϑ is always computed from $-\frac{u_t}{u_x}$. For the model to be reasonable, the only requirement is that the function that represents u must be chosen such that it satisfies empirical observation.

2.4 Expressions for Memristor Characteristics

This subsection derives expressions for memristor characteristics, from the computational model.

2.4.1 Computational framework

In order to plot the derived expressions, variable values are needed. To ensure consistency, the following values are always used. Only values that differ from these nominal assignments are called out where necessary.

Table 2.1 Table of default parameter values.

#	Parameter	Symbol	Units	Nominal value
1	Ion concentration	α	m^{-3}	0.2
2	Ion mobility	μ	$\frac{m^2}{V\ s}$	10^{-15}
3	Device length	d	nm	32
4	Fresh device resistance	γ	Ω	100
5	Computational aid	η	-	0
6	Computational aid	p	-	0.99
7	Computed flux	ϕ	$V\ s$	$\int_{t=0}^{T} v(t)\ dt$
8	Calculated natural frequency	f_0	Hz	0.977

In Table 2.1, the natural frequency of the default memristor is calculated using $f_0 = \frac{\mu}{d^2} = 0.977{\sim}1$ Hz. The dimensions of $\frac{\mu}{d^2}\left[\frac{L^2}{V\ s}\ \frac{1}{L^2}\right]$ is Hz/V. However, it is possible to cancel the V^{-1} dimension with the voltage dimension of flux $\emptyset\ [V\ s]$; thereby enabling f_0 to be written as a pure frequency.

2.4.2 Accumulation boundary

In order to use (2-11) as a solution for ion evolution, $n_b(t)$ must be known. Integrating (2-11) over the length of the device at any time will yield the total vacancy count within the device; which must equal the original α. Equating the integral to α and solving for the only unknown results in an expression for $n_b(t)$. In (2-19), all quantities are known except $n_b(t)$.

$$\int_{n=0}^{1} \frac{1}{1 + a\ e^{-f_0\phi(n-n_b(t))}}\, dt = \alpha \tag{2-19}$$

The computer algebra system (CAS) Mathematica is used to find the solution.

$$n_b(\phi) = \frac{1}{f_0\,\phi}\ln\left(\frac{\alpha}{\alpha-1}\frac{e^{f_0\phi\,\alpha} - e^{f_0\phi}}{e^{f_0\,\phi\,\alpha} - 1}\right) \tag{2-20}$$

In (2-20), $\phi = v\,t$ with v representing a DC voltage and t is time. Fig. 2.4 plots the evolution of (2-20). Variable values used for the plot are the normalized $\alpha = 0.2$, $f_0 = 1$ and $v = 1$. Around the origin, each half of the plot shows the ion boundary evolving asymptotically toward either end. This is equivalent to transiting from ST0 to ST1' or ST1 in Fig. 2.1. The initial entry of the ion-boundary into device is shown within the grey bounding box and the direction of travel is shown with the arrow. The significance of the direction reversal of $n_b(t)$ after initial entry into the device is that it contributes to the transient active nature of this seemingly passive device; as will be explained in later in 5.7 Negative resistance explained.

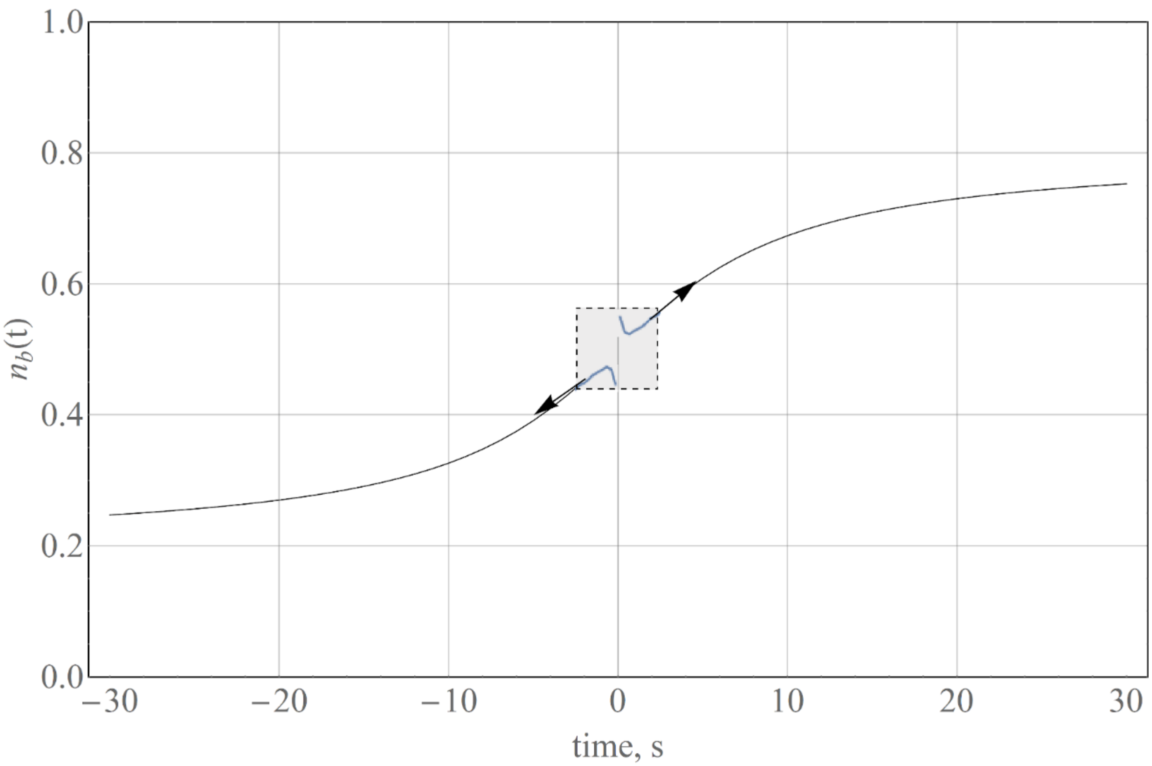

Fig. 2.4 Ion boundary evolution

2.4.3 Vacancy concentration

Solution (2-11) works with (2-20) to generate the ion evolution profile. Fig. 2.5 plots ion evolution in a device with $1\,V$ applied across the terminals. The y-axis is normalized concentration $0 \leq u \leq 1$, while the x-axis is the normalized length along the device $0 \leq n \leq 1$ where $n = x/d$. Each plot marks the location of the accumulation boundary with a dot. The device progressively enters high resistance in the sequence Fig. 2.5 (a) – (c).

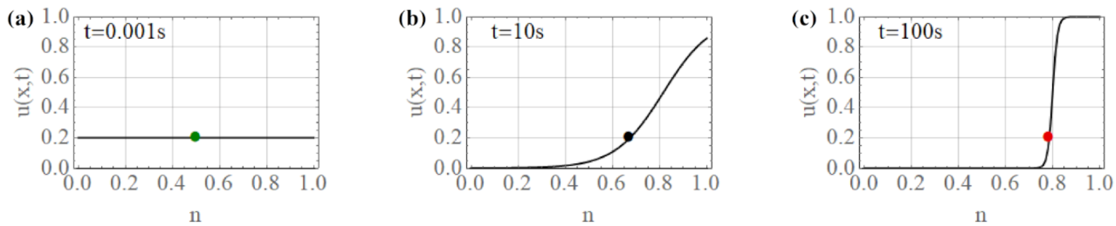

Fig. 2.5 Ion evolution along the normalized length of the memristor device.

2.4.4 Resistance

This subsection derives the device resistance from ion migration. Low resistance is associated with ions distributed evenly throughout the device. The resistance at any location within the device is defined as,

$$r(x,t) = \frac{\gamma}{1+\eta-p\,u(x,t)}. \tag{2-21}$$

In (2-21), γ is the resistance of a fresh device with no vacancies or ions, η is a computational knob to prevent the expression from evaluating to infinity in case $p\,u(x,t)$ evaluates to unity, and p is a computational knob to guarantee that $u(x,t)$ is constrained to less than unity. The resistance across the device terminals can be determined by integrating (2-21) over $0 \leq x \leq d$ or its normalized form $0 \leq n \leq 1$.

$$R(t) = \int_{n=0}^{1} r(n,t)\, dn \tag{2-22}$$

The computation was done with Mathematica. The result can be expressed as the sum of two resistors $R_1(t)$ and $R_2(t)$ quite simply by partial fraction decomposition.

$$R_1(t) = \frac{p^2 \ln(p^2 \left(-e^{\frac{\alpha\, f_0\, \phi}{p}}\right) + e^{f_0\, \phi} + p^2 - 1)}{f_0\, (p^2 - 1)\phi} - \frac{1}{p^2 - 1} \tag{2-23}$$

$$R_2(t) = -\frac{p^2 \log(\left((1 - p^2)e^{f_0\, \phi} - 1\right) e^{\frac{f_0\, \phi\, (\alpha - p)}{p}} + p^2)}{f_0\, (p^2 - 1)\phi} \tag{2-24}$$

$$R(t) = R_1(t) + R_2(t) \tag{2-25}$$

Equations (2-23) and (2-24) use $\gamma = 1$, $\eta = 0$, $\phi = (v\ t)$ and $\frac{\mu}{d^2} = f_0$. Although in this case $\phi = (v\ t)$, the general representation must be $\phi = \int_{t=0}^{T} v(t)\, dt$. Equation (2-25) represents the composite device resistance and is the sum of the individual components. Fig. 2.6 plots (2-25) with $p = 0.99$.

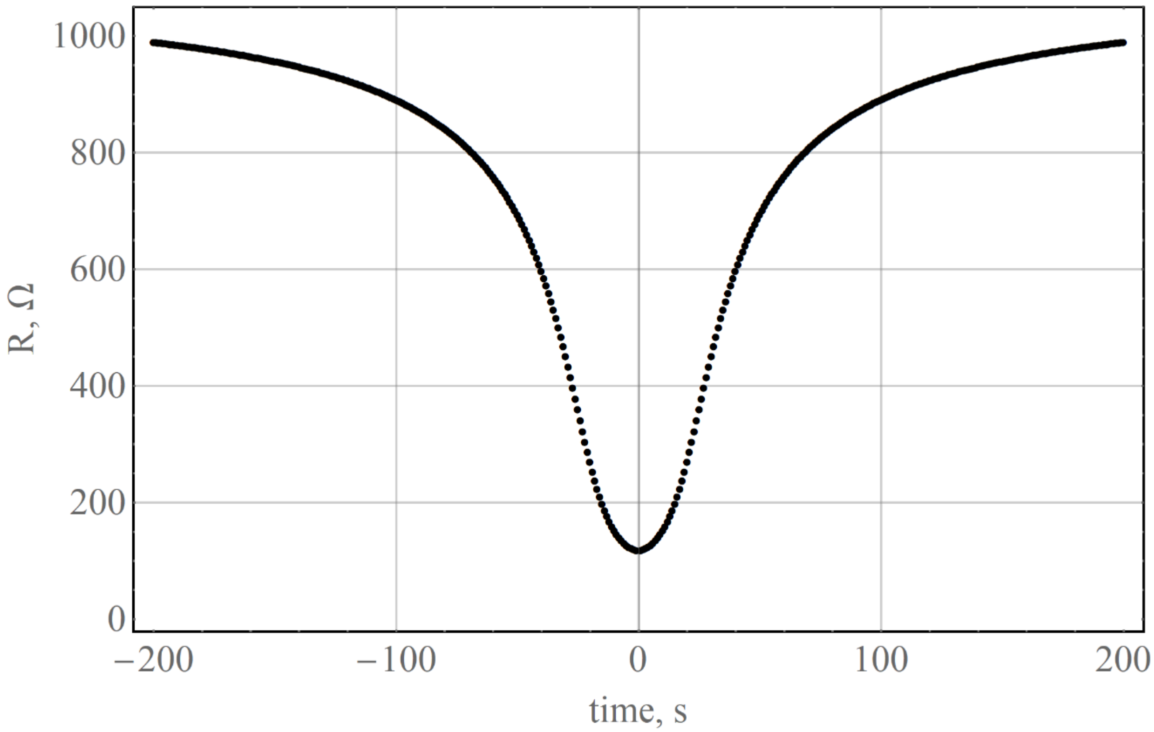

Fig. 2.6 Device resistance as a function of time.

Fig. 2.6 shows resistance evolving from a high value to low and back to high resistance as proposed in Fig. 2.1. The notable result is that the expression for resistance derived from (2-9) has two computable parts (2-25), like the DVR based rheostat from HP.

2.4.5 I-V curves

Current-voltage curves are almost always presented as a signature of memristance. Memristance manifests as lobes in the I-V curve where a specific stimulus results in two responses depending on the direction in which the voltage sweep occurs. Fig. 2.7 plots the simulated current through the device, for a sinusoidal forcing function of $v(t) = 0.1 + 0.5 \sin(\omega\, t)$ and all nominal values from Table 2.1. The unfilled dot indicates the start of while the black filled dot indicates the end of the trace.

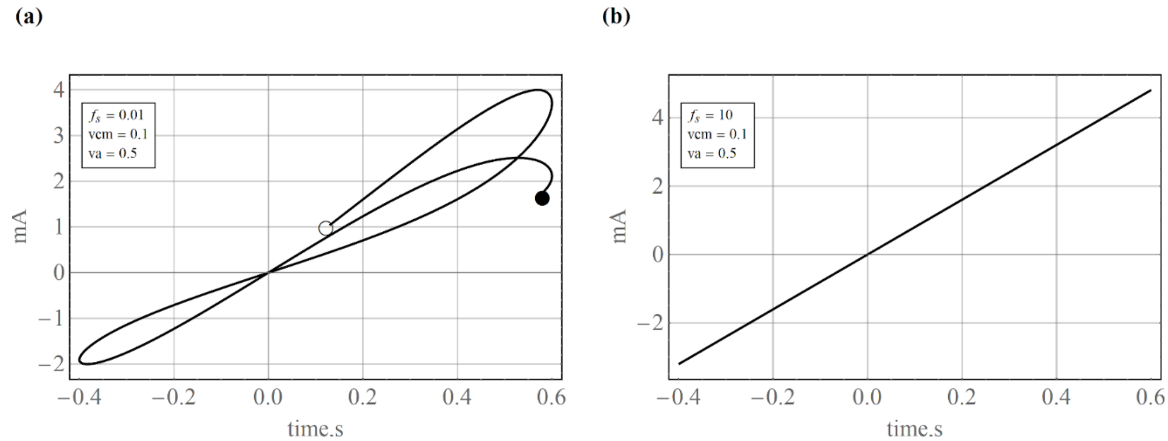

Fig. 2.7 Simulated memristor I-V curves demonstrating the three fingerprints.

Fig. 2.7 (a) shows the I-V plot for 1.3 cycles of the input stimulus which has a dc offset v_{cm} of 100mV. The device natural frequency is about 1 Hz and the forcing frequency is indicated by the variable f_s in the figures. The dc offset is obvious from the asymmetry of the trace along the x and y axis. The first lobe in quadrant 1 is large and shows the device starting in the low-resistance state and entering high resistance. The second lobe in quadrant 3 is much smaller because the dc offset causes the device resistance to increase even when the stimulus is negative. The third lobe in quadrant 1 has a low resistance that is higher than the low resistance associated with the first lobe. The simulation is terminated just prior to reaching the origin. Fig. 2.7 (a) exhibits fingerprint 1 which expects a pinched hysteresis loop as detailed in sub section 1.3.3.1.

Fig. 2.7 (b) uses a stimulus at 10 times the natural frequency of the device; common-mode and amplitude unchanged from Fig. 2.7 (a). The pinched loop has decreased in area compared to panel (a) satisfying fingerprint 2 from sub section 1.3.3.2. In this case the I-V curve has completely collapsed to a straight line, also satisfying fingerprint 3 from sub section 1.3.3.3.

Given that the resistance of a fresh device is about 100 Ω; the plots correctly demonstrate a maximum current of 4 mA in agreement with the calculation $i = 0.5\frac{V}{100}\Omega$. The simulated maximum current is lower because the device is always responding to the 100 mV common mode that constantly pushes it into the high resistance state.

In summary, the computational model can demonstrate the three fingerprints of memristors.

2.4.6 Switching time

Switching or transition time is the time it takes for a memristive device to transition from low resistance to high resistance or vice versa. Symbolic evaluation of transition time from (2-22) is impossible. Therefore, an approximate but novel approach is adopted to estimate the transition time. Assume that Fig. 2.8 shows the evolved state of vacancies in a device.

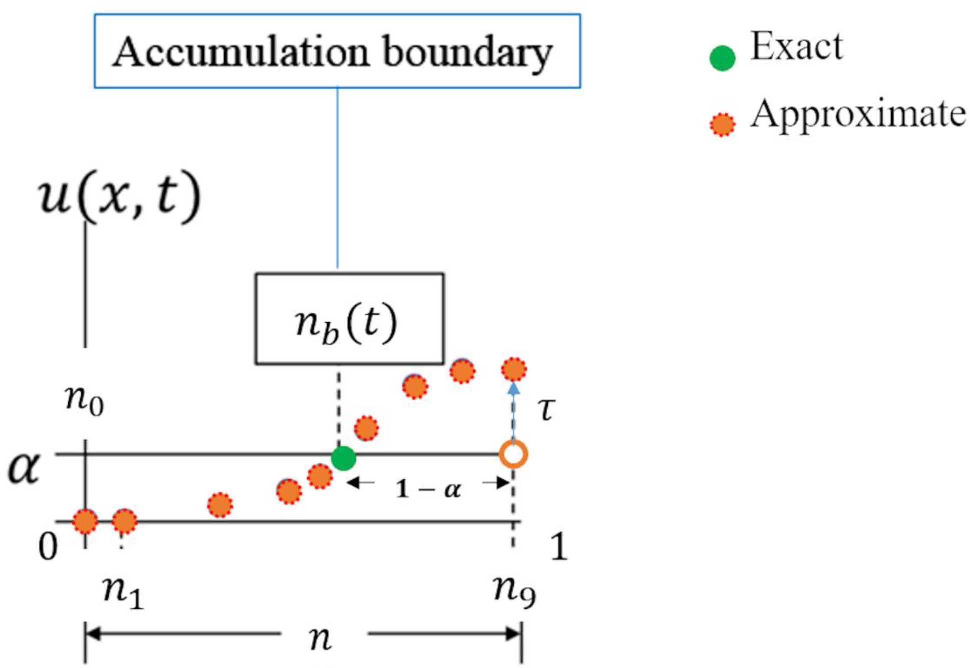

Fig. 2.8 Model for estimating transition time.

It is proposed that the time it takes for the ion concentration at the position $n = 1$ to evolve from its original value of $u(1,0) = \alpha$ to $u(1,\tau) = 1$ is the transition time τ. Constraining the model to work with the resistance at a single position enables the calculations to use (2-21). Low resistance is estimated by setting $u = \alpha$. For convenience assume that the computational aids are assigned $\eta = 0$ and $p = 1$.

$$r_{LO} = \frac{\gamma}{1 - \alpha} \tag{2-26}$$

Similarly, the high resistance is estimated by,

$$r_{HI} = \frac{\gamma}{1-u(1,\tau)}. \tag{2-27}$$

Defining resistance ratio as rr,

$$rr = \frac{r_{HI}}{r_{LO}} = \frac{(1-\alpha)}{1-u(1,\tau)}. \tag{2-28}$$

From (2-11), $u(n,t) = \frac{1}{1+\alpha\, e^{-f_0 \phi\left(n-n_b(t)\right)}}$. It follows that, $u(1,\tau) = \frac{1}{1+\alpha\, e^{-f_0 \phi\left(1-n_b(\tau)\right)}}$; where $n_b(\tau) \sim (1-\alpha)$. Because the concept of transition time applies only with DC excitation, $\phi = V\,\tau$. Substitute for $u(1,\tau)$ in (2-28) and simplify.

$$rr = (1-\alpha) + \alpha\, e^{\alpha\, f_0\, V\, \tau} \tag{2-29}$$

Transition time is obtained after simple algebraic manipulation.

$$\tau = \frac{1}{f_0\, V}\left(\frac{1}{\alpha}\ln\left(\frac{rr}{\alpha} - \frac{1-\alpha}{\alpha}\right)\right) \tag{2-30}$$

Expression (2-30) is the first time in literature that a relationship between transition time vacancy concentration has been quantified [33] and discussed in additional detail in [34]. The salient observations from (2-30) follow.

- Switching time is inversely proportional to the programming voltage. A device can benefit from being operated at a higher voltage to increase its operating speed; limited by the breakdown voltage across the MIM sandwich.
- Switching time is inversely proportional to the device natural frequency f_0. Recalling that natural frequency itself is $f_0 = \frac{\mu}{d^2}$, the inference is that switching is inversely proportional to ion mobility and directly proportional to the square of device length. These findings agree with the linear estimation by Strukov et al. [38], Biolek et al. [27] and Batas et al. [16].

The additional term in (2-30) reveals the influence of ion concentration on transition.

- The nonlinear dependence of switching time is dominated by ion concentration α.
- Switching time is inversely proportional to α [34], except at bounding values of α.

Consider (2-30) with the substitution $rr = \frac{r_{HI}}{r_{LO}}$; where $r_{HI} = \frac{\gamma}{1-p\, u(n,\tau)}$ and $r_{LO} = \frac{\gamma}{1-\alpha}$. This leads to an expression entirely in p and α.

$$\tau = \frac{1}{f_0\, V}\left(\frac{1}{\alpha}\ln\left(\frac{p}{1-p}\,\frac{1-\alpha}{\alpha}\right)\right) \tag{2-31}$$

Although p is usually assumed to be 1 for convenience, it is a computational assist that tunes the model for Coulomb repulsion or van der Waals forces that *disallow* $u(1,\infty) = 1$ [38]. A practical setting for p may be $0.8 \leq\ p \leq\ 1$. Similarly, (2-29) can be expressed in only p and α. Fig. 2.9 plots (2-31) and (2-32).

$$rr = \frac{1-\alpha}{1-p} \tag{2-32}$$

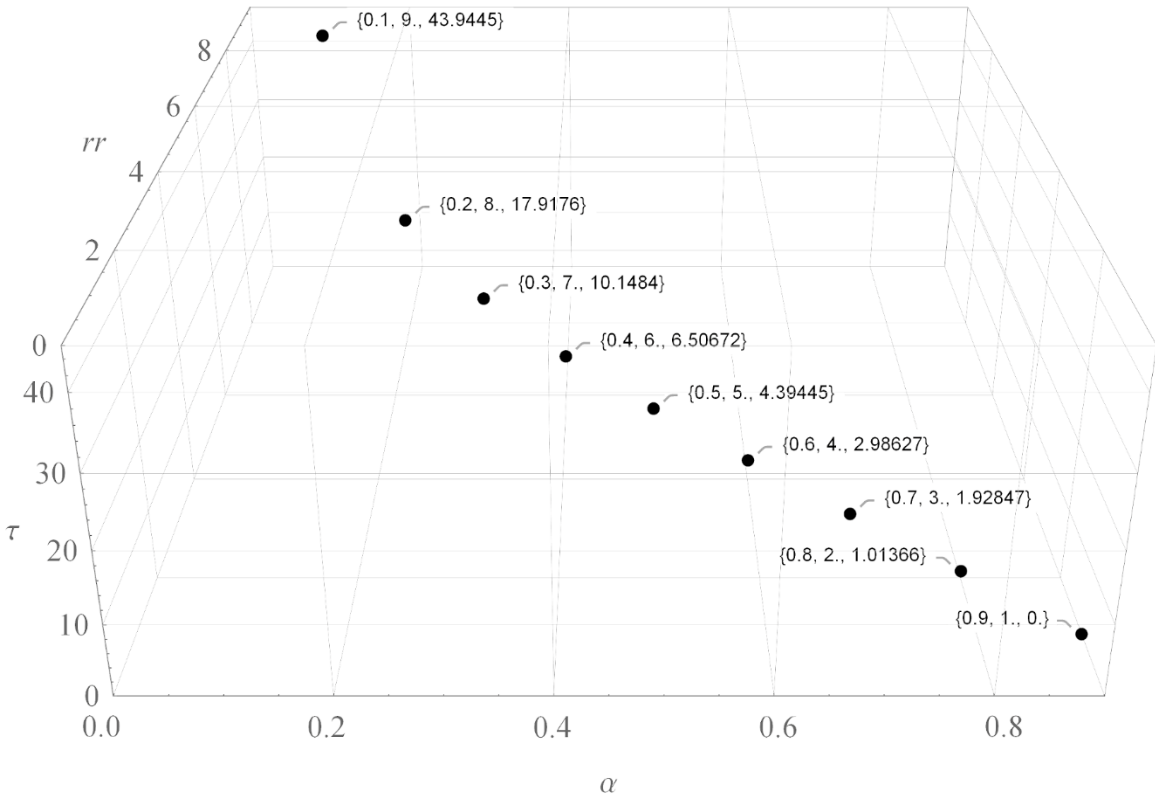

Fig. 2.9 Relationships between ion concentration, switching time and resistance ratio.

The data points in Fig. 2.9 are annotated with (α, rr, τ) in that order. When ion concentration α increases, the resistance ratio and transition time decrease. Therefore, it is not possible to decrease transition time without impacting the resistance switching range for a given chemical species unless ion-mobility, device length or programming voltage are manipulated [33].

2.4.7 Switching energy

Energy awareness is paramount in any modern analog or digital application. From (2-25),

$$E = \int_{t_0}^{t_1} \frac{V^2}{R(t)}\, dt = \int_{t=0}^{\tau} \frac{V^2}{R(t)}\, dt. \tag{2-33}$$

2.4.8 Shelf life

A memristor is referred to as being on the shelf or unused whenever it has zero volts across the device terminals. The computational model in this dissertation assumes that vacancies accumulate and dissipate in time, with some spatial distribution profile along the device length. This is similar to the heat redistribution in a thermally insulated rod. The insulation is analogous to enforcing vacancy conservation which guarantees that vacancies cannot exit the memristor.

Shelf life is modeled with the following "heat" equation.

$$u_t + \mathcal{D}\, u_{xx} = 0 \tag{2-34}$$

The second term in (2-34) models ion dispersal due to concentration gradients. Coefficient $\mathcal{D}$ is the diffusion constant. This PDE can be solved symbolically using Fourier analysis [33].

$$u(x,t) = A_0 + \sum_{i=1}^{\infty} A_n \cos\left(\frac{i\,\pi\,x}{d}\right) e^{-\left(\frac{i\,\pi}{d}\right)^2 \mathcal{D}\,t} \tag{2-35}$$

In (2-35) A_0 and A_1 are coefficients that can be determined using a knowledge of the initial conditions. Variable i is the iterator, $\mathcal{D}$ is diffusion coefficient, d is device length. Literature suggests that memory resistance retention can stretch from 5 to 11 years [39], [40], [41]. Consider Fig. 2.10 which demonstrates the dissipation of ions during shelf time. The initial distribution of vacancies was described by $f(n) = \frac{1}{1+e^{s\left(n-n_b(t)\right)}}$. Given that the device must be in its high resistance state at the start of the simulation, $n_b(t) = 1 - \alpha$. The variable s represents slope of the vacancy profile. This slope is a function of the accumulated flux from prior programming, namely $s = f_0\,\phi$.

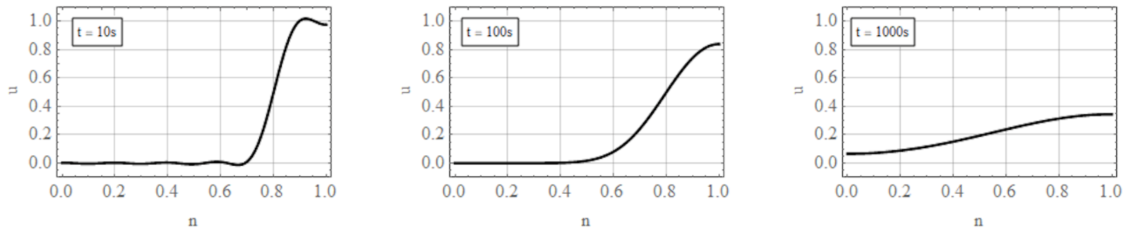

Fig. 2.10 Ions dissipating during shelf time.

The three panels of Fig. 2.10 demonstrate that vacancies dissipate over time solely due to the concentration gradient. Normalized simulation parameters were $\mathcal{D}/d^2 = 100\mu$, $\alpha = 0.2$ and $s = 100\ V \cdot s$.

While an ideal device modeled by (2-9) is non-volatile, a more practical volatile device can be modeled by combining terms of (2-9) and (2-34).

$$u_t + \vartheta\, u_x + \mathcal{D}\, u_{xx} = 0 \tag{2-36}$$

From the discussions up to this point, it should be clear that during programming of a memristor, the active transport of ions can be modeled by the first two terms of (2-36). Memristive un-programming due to disuse can be modeled by equating the sum of the first and third terms to zero.

2.5 Model Validation

Switching time is a convenient and often reported parameter against which the model in this dissertation can be benchmarked. Switching speed is a function of ion mobility, temperature, voltage and device length. Second order effects like surface roughness at the interfaces, nonuniformity of the electric field between the plates, local heating effects that affect mobility etc. are expected to play a significant role in determining device switching time. Only a numerical approach can tackle the problem when second order effects are considered. Such methods are outside the scope of this dissertation. The following calculations assume room temperature, since it is not usually reported. The following results based on (2-30) are published [33].

Table 2.2 Validation of transition time against independent empirical data.

					Transition time τ(s)		
#	**Reference**	**Oxide**	**Volts(V)**	**[1]Mobility**	**Reported**	**This dissertation**	**% Error**
1a	[23] Nardi	HfO_x	1.2	10^{-08}	04 μ	03.20 μ	-20
1b	"	"	1.0	$0.22\text{x}10^{-8}$	15 μ	20.00 μ	33
1c	"	"	0.8	$0.19\text{x}10^{-8}$	20 μ	21.70 μ	8.5
2	[5] Strukov	TiO_2	1.0	10^{-14}	10 m	10.00 m	0.0
3	[42] Lu	$Ag/a - Si$	3.2	10^{-08}	1.2 m	1.180 m	1.6
4	[29] Biolek	TiO_2	1.0	10^{-14}	500 m	448.0 m	10.4

[1] Mobility was estimated from among various sources. Rows 1b and 1c used arbitrarily scaled mobility to accommodate the dependence on electric field.

2.6 Chapter Summary

The computational ion transport model presented in this chapter is derived from the traditional transport equation. Long channel length, low mobility or programming voltage are the justifications for ignoring a term in the PDE that computes the gradient of the characteristic wave velocity. This simplification permits a Heaviside step or logistic function like symbolic solution. This solution to the governing equation is validated against the PDE. The solution is then used to demonstrate and derive expressions for a variety of memristor characteristics; each showing good correlation to the works of independent researchers. The problem of memory volatility is addressed by observing a correspondence between the popular heat dissipation problem in physics and ion dissipation in a concentration gradient. The heat equation is reformulated with variables appropriate to vacancy migration and solved symbolically. The resulting solution is shown to exhibit ion dissipation as expected. Largely, this chapter quantified the memristor life cycle with governing equations and solutions.

3 Computational Logistic Model

This chapter presents the transition from ion transport to abstract logistic modeling. The discussion is substantially drawn from [43] where we first reported the development and evaluation of this technique.

3.1 Background

Expressions such as (2-10) in the computational ion transport model are very similar to a smooth Heaviside step function [36] or the logistic/sigmoid function [37]. These functions take on the same shape as the ion evolution profile. Abstract functions have the advantage that they decouple a model from the underlying operating mechanism. The focus is on generating life-like responses with none of the physics. Abstract models can be computationally simpler than physical models, provide a level of generality and sometimes clarity.

Model abstraction is not new. In their work associating memristive response to Abel, Riccati and Bernoulli dynamics, Biolek et al. propose that sigmoidal functions may be useful in representing memristor behavior [30]. A sigmoidal model from Saminathan et al. is also known [44]. Saminathan uses the sigmoid like a window function $f\big(w(t)\big)$ to modulate the HP equations as shown in (1-8). Ascoli et al. study local-activity in memristors as observed by HP, using polynomial functions [45].

Corinto et al. have presented hypergeometric and gamma function solutions to the HP equations [28]. These researchers have laid the foundations for studying memristors from a non-linear dynamics perspective using abstract modeling.

3.2 Motivation

Memristors have been reported to exhibit chaotic response even in contemporary literature [46], [47], [48]. This property has purportedly been used in secure communications [48]. Although the computational ion transport model *does* exhibit the presence of an active phenomenon within the device the solution is well behaved and being first order, does not exhibit any chaotic response. While fractional calculus has been used to demonstrate memristive chaos [49], [50], these techniques tend to be deeply mathematical and are inaccessible to the general circuit design community. Miranda et al. have demonstrated memristive hysteresis using a double diode based logistic model [51], [52]. Corinto et al. have presented some research based on traditional nonlinear dynamics [53], [54]. With these efforts as backdrop, this dissertation explores the ability of the standalone logistic equation to exhibit memristive qualities including chaotic response.

3.3 The Logistic Function

The ion evolution profile along the device resembles a traveling logistic function as seen in Fig. 2.5, where a shallower distribution is associated with low resistance and a steeper distribution maps to high resistance. Consider the following textbook logistic function which has been slightly modified to include memristor parameters.

$$R(t, n_b(t)) = s \frac{R_{max}}{1 + c\, e^{-m\, f_0\, n_b(t) \int_{t=0}^{T} v(t)\, dt}} \tag{3-1}$$

In (3-1), $R(t, n_b(t))$ is the memory resistance as a function of time and the location of the accumulation boundary, R_{max} is the maximum possible resistance of the device from empirical observations, c is an arbitrary constant is determined by the minimum resistance, m and s are free variables that can tune the device response, f_0 is the natural frequency of the device and $\int_{t=0}^{T} v(t)\, dt$ calculates electric flux. Variable c can be determined by equating $R\big(t, n_b(t)\big)\big|_{t=0}$to a numerical value for R_{min} and solving. Variable m can be arbitrarily chosen to match the device's temporal response from empirical data. Variable s is useful for arbitrary scaling of the amplitude of the function.

It was determined through simulations that computations can be simplified by disregarding $n_b(t)$ and relying on m to tune the model.

$$R(t) = s \frac{R_{max}}{1 + c\, e^{-m\, f_0\, \int_{t=0}^{T} v(t)\, dt}} \tag{3-2}$$

Equation (3-2) is identical to (3-1) except for the discarded $n_b(t)$ term in the exponent of e in the denominator. Consider Fig. 3.1 wherein the temporal response of (2-25), (3-1) and (3-2) are compared. Fig. 3.1 used $R_{max} = 2.5k\ \Omega$, $f_0 = 1\ Hz$, $c = 2$, $\alpha = 0.2$, $p = 0.9$ and a programming voltage of 1 V DC. A careful choice of tuning parameters m and s produced an acceptable match between the computational ion transport and the two variations on the computational logistic model. The conclusion is that the logistic form in (3-2) without any reference to the ion boundary is sufficient to demonstrate memristive characteristics. It is also possible to relate some of the free variables to the computational ion transport model. For example c can be found by equating $R(0)_{(3\text{-}2)}$to $R(0)_{(2\text{-}21)}$; where the subscript are equation numbers. Solving $s\frac{R_{max}}{1+c} = \frac{\gamma}{1-\alpha}$, for c produces $c = \frac{s\,R_{max}(1-\alpha)-\gamma}{\gamma}$. Additionally, if $R_{max} = \frac{\gamma}{1-p}$, then it is possible to reduce further as $c = s\frac{(1-\alpha)}{(1-p)} - 1$. Validation with an I-V curve is reserved for the SPICE modeling section.

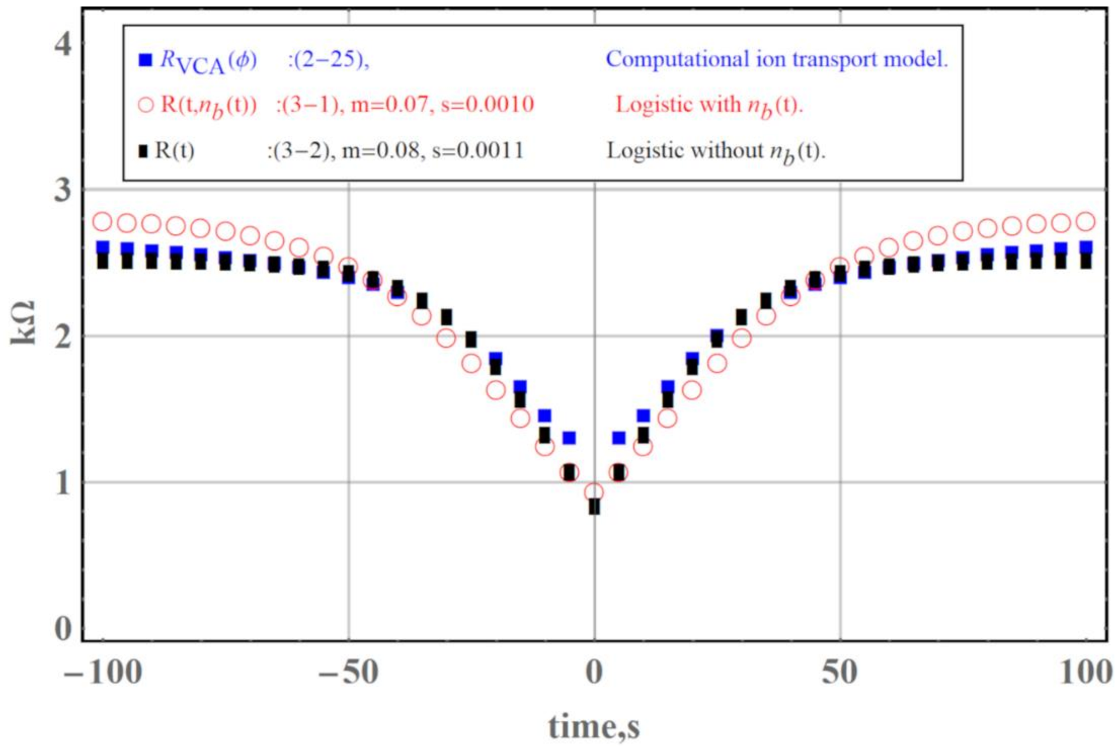

Fig. 3.1: Transient resistance-time curves comparing computational ion transport, logistic and simplified logistic models.

3.4 The Logistic Equation

The sigmoid function is a solution to the ODE $y' = \mu\, y(1-y)$ [37] where y is a function of time and μ is an arbitrary constant. Associate y with R and evaluate the left-hand side (LHS) of the said ODE for R from (3-2).

$$R' = \frac{c\,m\,s\,f_0\,R_{max}\,v(t)\,e^{m\,f_0\,\int v(t)\,dt}}{\left(c+e^{m\,f_0\,\int v(t)\,dt}\right)^2}. \tag{3-3}$$

The RHS can be evaluated similarly.

$$\mu\, R(1 - R) = \frac{\mu\, s\, R_{max}\left(1 - \frac{s\, R_{max}}{1 + c\, e^{-m\, f_0\, \int v(t)\, dt}}\right)}{1 + c\, e^{-m\, f_0\, \int v(t)\, dt}} \tag{3-4}$$

To be valid, equations (3-3) and (3-4) must be identical for some value of μ that can be solved for. The governing logistic equation can be written as follows.

$$R' = \mu\, R(1 - R) \colon \mu = \frac{c\, m\, f_0\, v(t)}{c + (1 - s\, R_{max})\, e^{m\, f_0\, \int v(t)\, dt}} \tag{3-5}$$

The leading term μ is sometimes called the Malthusian parameter. Equation (3-5) is shown with a general $\mu(t)$ which simplifies to a constant if the programming voltage is DC. Biolek's research into the Bernoulli Parameter State Map (PSM) resembles (3-5). For $v(t) = 1$ and $s = 1/R_{max}$, μ evaluates to $\mu = m\, f_0$, a constant.

3.5 The Logistic Map

Memristor models to date such as the HP [5], VCA [33], [34], VTEAM [55] etc. are differential equations of the first order. First order models do not readily exhibit sensitive dependence on initial conditions. Memristive circuits on the other hand have been reported to exhibit a rich variety of dynamics by Strukov [5], Petras [49] and Corinto et al. [53], [54]. The logistic map makes it feasible to model the memristor's purported sensitivity to initial conditions. A map is a discretized version of a continuous function. Consider the following first step where the function is replaced by the n^{th} iterate.

$$\frac{R_{n+1} - R_n}{\Delta t} = \mu\, R_n(1 - R_n) \tag{3-6}$$

Simple algebraic manipulation produces an expression for R_{n+1}.

$$R_{n+1} = R_n(1 + \mu\, \Delta t) - \mu\, R_n^2\, \Delta t \tag{3-7}$$

Let $\hat{\mu} = (1 + \mu\, \Delta t)$ from which it follows that $\Delta t = \frac{\hat{\mu}-1}{\mu}$. Substituting these into (3-7),

$$R_{n+1} = \hat{\mu}\, R_n \left(1 - \left(1 - \frac{1}{\hat{\mu}}\right) R_n\right) \tag{3-8}$$

Let $\hat{R}_n = \left(1 - \frac{1}{\hat{\mu}}\right) R_n$. Then it also follows that $R_n = \frac{\hat{\mu}}{(\hat{\mu}-1)} \hat{R}_n$; implying that $R_{n+1} = \frac{\hat{\mu}}{(\hat{\mu}-1)} \hat{R}_{n+1}$. Make these substitutions into (3-9).

$$\hat{R}_{n+1} = \hat{\mu}\, \hat{R}_n \left(1 - \hat{R}_n\right) \tag{3-9}$$

Equation (3-9) is the discrete analogue of (3-5) and is a textbook study for chaotic responses [56]. Parameter $\hat{\mu}$ elicits oscillations for different values. Traditionally an orbit diagram accompanies (3-9). The orbit diagram plots $\hat{R}_{n+1}$ against the independent variable $\hat{\mu}$. Due to sensitivity to initial conditions, any given $\hat{\mu}$ will display many $\hat{R}_{n+1}$ for the first few iterations, subsequently settling down to a more finite set as the number of iterations increase. Consider the orbit plot in Fig. 3.2 generated with a normalized seed of $R_n = 0.99$, where the first 30 of 300 iterations were discarded. With $s = 1/R_{max}$, $\hat{\mu} = m\, f_0$, where $\hat{\mu}$ will be influenced by the physical parameters that determine the device natural frequency; namely device length, localized and variable ion mobility and potential gradients. Therefore, the variability in $\hat{\mu}$ is a source of the chaotic response.

Fig. 3.2 shows that the device is single valued until $\hat{\mu} = 3$, with period doubling after. When $\hat{\mu} > 3.4$, the device takes on one among four values, and for $\hat{\mu} > 3.57$ the map is chaotic. The plot itself is the same as found in any introductory textbook on dynamical systems and shows the orbit plot of the discretized logistic equation, adapted to the context of memristor modeling.

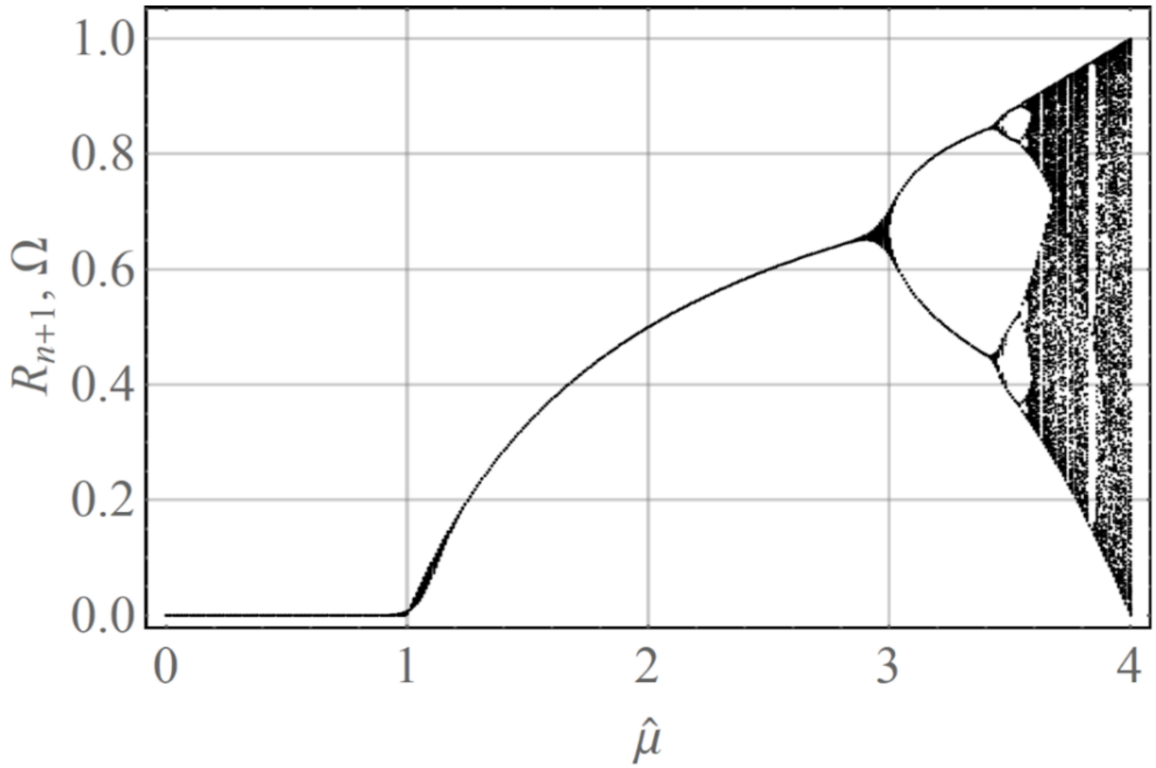

Fig. 3.2 Orbit plot for (3-9).

3.6 Relation to fluid dynamics

The logistic form relates to other well-known equations that find application in fluid dynamics. The Abel ODE of the first kind $y' = f_0 + f_1\, y + f_2\, y^2$ appears in Biolek's study [30]. With $f_0 = 0$ and $f_2 = -f_1$, the ODE reduces to the logistic differential equation. May discusses the logistic equation from the perspective of the "simplest nonlinear difference equation" with applications in studying fluid turbulence [57]. Ion transport resembles fluid flow, suggesting the use of fluid dynamics techniques to be applied to uncover memristor dynamics.

Fig. 3.3 is a phase plot of the logistic difference equation. The plot shows the response of a memristor that has been parked at some arbitrary resistance by the application of a voltage. The programming voltage determined the value of μ. Each of the two panels shows the key parameter values as insets. Panel (a) shows a very stable normalized resistance of 0.5 for all iterations. Panel (b) on the other hand shows that the resistance exhibits what might be characterized as a “flicker” over each iteration. The plot is to be interpreted to mean that during a programming, there can be no expectation that the same deterministic resistance will be achieved at a given iteration. This is the unpredictability with programming memristors that is addressed by Naous et al. with specific emphasis on the variability in switching time [58]. The authors point out the disparate needs of digital design and neuromorphic designs. Digital design prefers repeatability where accurate thresholds translate into a measure of robustness. Neuromorphic implementations thrive on unpredictability. The authors suggest that the innate stochasticity of memristors can prove to be an alternative to external noise injection in the cases where unpredictability is an advantage. The general topic of stochasticity, probabilistic switching and its importance in neural networks is discussed by the same authors in [59].

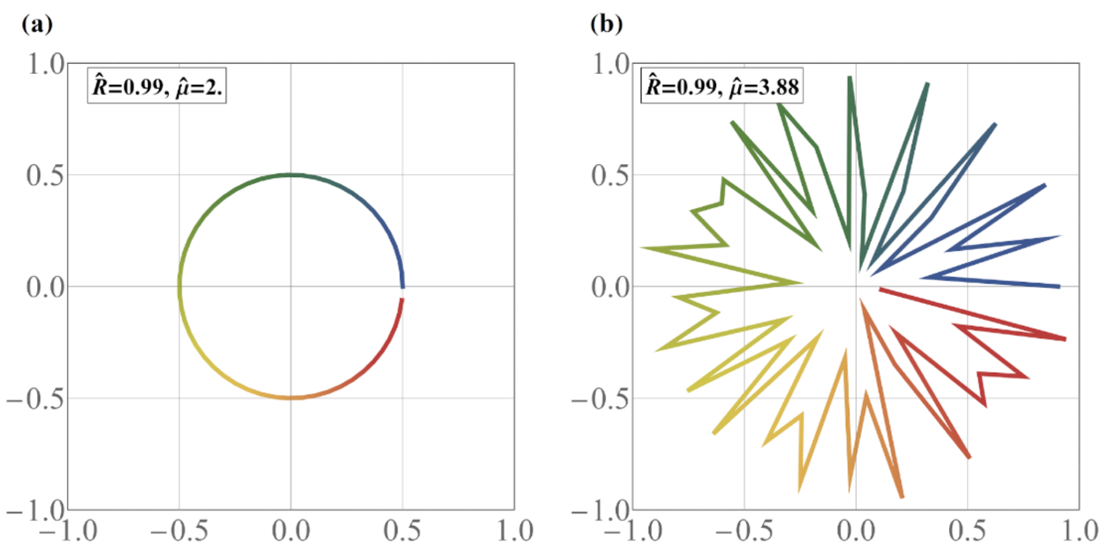

Fig. 3.3 Phase plot of $\hat{R}$ evolution.

3.7 Origin of oscillatory response

It is well known that it requires a second order differential equation to have any oscillatory solutions. Second order systems can transfer energy between orthogonal states. Consider the ordinary logistic equation in the continuous domain.

$$R' = \mu R(1 - R) \tag{3-10}$$

Multiply the outer terms into the bracketed terms.

$$R' = \mu R - \mu R^2 \tag{3-11}$$

The term in R is a function of time as in $R(t)$. Differentiating w.r.t time and transposing terms,

$$R'' - \mu R' + 2\mu R R' = 0. \tag{3-12}$$

In this form, the following observations can be made.

- The proposed logistic equation is second order due to the R'' term. This second order nature allows oscillatory solutions that are essential for representing chaotic evolution.
- The proposed logistic equation is nonlinear due to the $R R'$ term. This nonlinearity is essential to reproducing memristor characteristics such as asymptotic approach to high and low resistances, development of a negative differential resistance during state transitions and hard switching.

3.8 Chapter Summary

This chapter presented the case for transitioning from ion-transport PDE based modeling into an abstract nonlinear ODE domain. This proposed transition is supported by simulations showing that the logistic differential equation and function can represent memristive behavior as fairly as the ion transport model. The logistic model has the advantage that it is used extensively for approximating fluid flow problems, making prior and continuing developments in the field available for use with memristors. In addition to generating memristive characteristics, the logistic form has been shown to reproduce the chaotic and oscillatory response that empiricists have claimed. Contemporary research has had to resort to fractional order modeling to mimic the rich dynamical behavior of memristors. Fractional order models are very inaccessible to circuit designers. In this context, logistic based modeling can be much more mature, easier to understand and accessible to the circuit design community.

4 SPICE Model

This chapter presents SPICE modeling of the memristor. The discussion is substantially drawn from [60] and [43] where we first reported these developments. The purpose is to present the transition from the computational ion transport model through an intermediate Abel differential equation model to finally the logistic model. The Abel and logistic models are implemented in SPICE.

4.1 Background

Computational models require a mathematical program for implementing them. Circuit designers however work with SPICE to simulate electrical networks consisting of devices. Therefore, the model in this dissertation is implemented in SPICE to allow testing in circuit networks. One of the first memristor SPICE models by Biolek et al. implements HP's DVR model modulated by window functions [27]. Batas et al. present a behavioral two-terminal SPICE model using only independent sources [16]. Batas et al. demonstrate their model in a memristor-only AND gate. Mahvesh et al. present a similar SPICE model and demonstrate a low pass filter and an integrator [61]. Berdan et al. demonstrate a model that combines nonvolatile and volatile characteristics [62]. Their model is abstract and does not relate directly to physical parameters of the device. To be relevant for circuit designers, SPICE based modeling is the next logical step for any physical or abstract model.

4.2 Simplified Computational Ion Transport

The theoretical model for resistance in 2.4.4 is still too complicated for implementing in SPICE. A major contributor to this complexity is the expression for accumulation boundary (2-20); which can be simplified.

Consider the reasonable approximation $\alpha \ll 1$. Starting from (2-20),

$$n_b(\phi) = \frac{1}{f_0\,\phi}\ln\left(\frac{\alpha}{\alpha-1}\frac{e^{f_0\phi\,\alpha}-e^{f_0\phi}}{e^{f_0\,\phi\,\alpha}-1}\right) = \frac{1}{f_0\,\phi}\ln\left(\frac{\alpha}{\alpha-1}\frac{e^{f_0\phi\,\alpha}\left(1-e^{-f_0\phi(\alpha-1)}\right)}{e^{f_0\,\phi\,\alpha}\left(1-e^{-f_0\,\phi\,\alpha}\right)}\right) = \frac{1}{f_0\,\phi}\ln\left(\frac{\alpha}{\alpha-1}\frac{\left(1-e^{-f_0\phi(\alpha-1)}\right)}{\left(1-e^{-f_0\,\phi\,\alpha}\right)}\right). \tag{4-1}$$

For $\alpha \ll 1$, $\frac{\alpha}{\alpha-1} \to -\alpha$. During any programming, flux is expected to be large, hence $e^{f_0\phi} \gg 1$. Using these two relations, consider replacing the numerator $1 - e^{-f_0\phi(\alpha-1)} \sim 1 - e^{f_0\phi} \sim -e^{f_0\phi}$. In the denominator, $e^{f_0\phi\,\alpha}$ is being moderated by the small α; suggesting a more linear replacement $e^{f_0\,\phi\,\alpha} - 1 \sim \phi$; similar to the linear approximation for a diode curve beyond the diode threshold voltage V_{TH}.

$$n_b(\phi) = \frac{1}{f_0\,\phi}\ln\left(-\alpha\frac{-e^{f_0\phi}}{\phi}\right) = \frac{1}{f_0\,\phi}\ln(\alpha) + \frac{1}{f_0\,\phi}\ln\left(e^{f_0\phi}\right) - \frac{1}{f_0\,\phi}\ln(\phi) \tag{4-2}$$

Given that $\alpha \ll 1$, the first term $\frac{1}{f_0\phi}\ln(\alpha)$ is small for large $f_0\phi$ and can be ignored. The remaining terms form the approximation to the ion boundary, referred to henceforth as $\hat{n}_b(t)$ or $\hat{n}_b(\phi)$.

$$\hat{n}_b(\phi) = \frac{1}{f_0\,\phi}\ln\left(e^{f_0\phi}\right) - \frac{1}{f_0\,\phi}\ln(\phi) = 1 - \frac{1}{f_0\,\phi}\ln(\phi) \tag{4-3}$$

The term $1/f_0$ can be replaced by an arbitrary constant q_{n_b} to control the inflection, and an arbitrary overall scaling factor s_{n_b} has been added to control the final asymptote.

$$\hat{n}_b(\phi) = s_{n_b}\left(1 - \frac{q_{n_b}}{\phi}\ln(\phi)\right) \tag{4-4}$$

Consider Fig. 4.1 comparing the ion boundary from the full computational model and the approximate model, generated with $s_{n_b(t)} = 0.2$ and $q_{n_b(t)} = 1.025$.

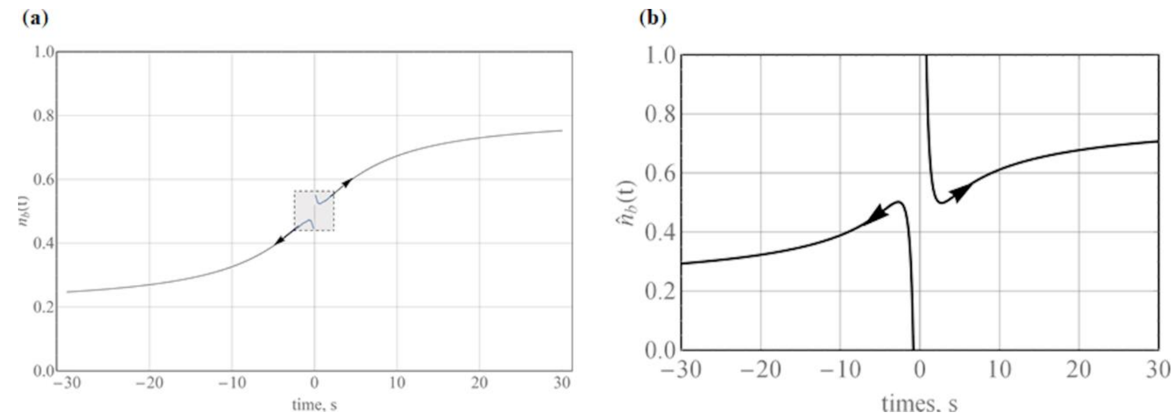

Fig. 4.1 Ion boundary evolution from (a) full ion transport model (2-20) and (b) simplified expression (4-4).

In Fig. 4.1 (a), the ion boundary is seen to very rapidly approach from infinity, reverse direction and asymptotically approach the final position. The same desirable response is observed in Fig. 4.1 (b). This simplified expression for $\hat{n}_b(t)$ can be used to evaluate the total resistance across the device; starting from (2-21).

$$R(\phi) = \int_{n=0}^{1} \frac{\gamma}{1+\eta-p\,u(n,t)} :\ n_b(t) \rightarrow (4\text{-}4) \tag{4-5}$$

Setting variables that are inconsequential in this context to 0 or 1 as appropriate; $\eta = 0$, $\{\mu, \gamma, d, \hat{s}_{n_b}, \hat{q}_{n_b}\} = 1$ and $V\ t = \ \phi$ results in the following final expression.

$$R(\phi) = \frac{p \ln\left(a e^{\phi\left(1-\frac{\ln(\phi)}{\phi}\right)} - p + 1\right)}{(p-1)\phi} - \frac{p \ln\left(\frac{a}{\phi} - p + 1\right)}{(p-1)\phi} - \frac{1}{p-1} \tag{4-6}$$

In its general form.

$$R(\phi) = \ C - f(\phi) \colon n_b(t) \sim 1 - \frac{1}{\phi}\ln(\phi) \tag{4-7}$$

While simple, (4-7) is informative. It confirms that memristors are devices with a resistance proportional to the amount of accumulated flux [34]. Equation (4-7) opens memristor modeling to any function that satisfies the general form as long as the results can be tuned to match memristive characteristics.

4.3 Structure of SPICE Model

The implementation in SPICE is generic as shown in Fig. 4.2 and uses behavioral components for the computations. Fig. 4.2 (a) shows a voltage-controlled resistor, where the device resistance is modulated by electric flux. The electric flux is generated by a behavioral component that calculates the difference in voltage between the two pins, and a second component that integrates this voltage to generate flux. A capacitor C_P is attached to each of the device pins to model parasitic lead capacitance. Parasitic lead inductance is expected to be insignificant at the low kHz natural frequency of the device and therefore excluded from the modeling. Device resistance $R(\phi)$ can be defined as any appropriate function. Fig. 4.2 (b) is the symbol view. It consists of the two device pins (a,b) and additional debug pins. Pin ϕ allows the user to view the flux. The pin-mode toggles in binary to indicate if the flux is positive (1) or negative (0). The pin-v_{ab} offers visibility into the voltage difference between the input pins. As indicated in the symbol, the ion boundary can be moved toward either end plate and the model user must ensure that the stimulus is controlled such that the device is operated between low and any one of the two high resistances only. The modeling expression for $R(\phi)$ in the rest of the discussion in this section is the logistic form with minor enhancements.

$$R(\phi) = \max\left(R_{min}, s\frac{R_{max}}{1 + c\, e^{-m\, f_0\, (\phi+\phi_0)}}\right) \tag{4-8}$$

The only new term in (4-8) compared to (3-2) is ϕ_0 which stores any initial flux from prior programming. The max() function ensures that the resistance can never compute to a negative number in the event of any errors in setting up the expression. The basis for this structural modeling was published in [34].

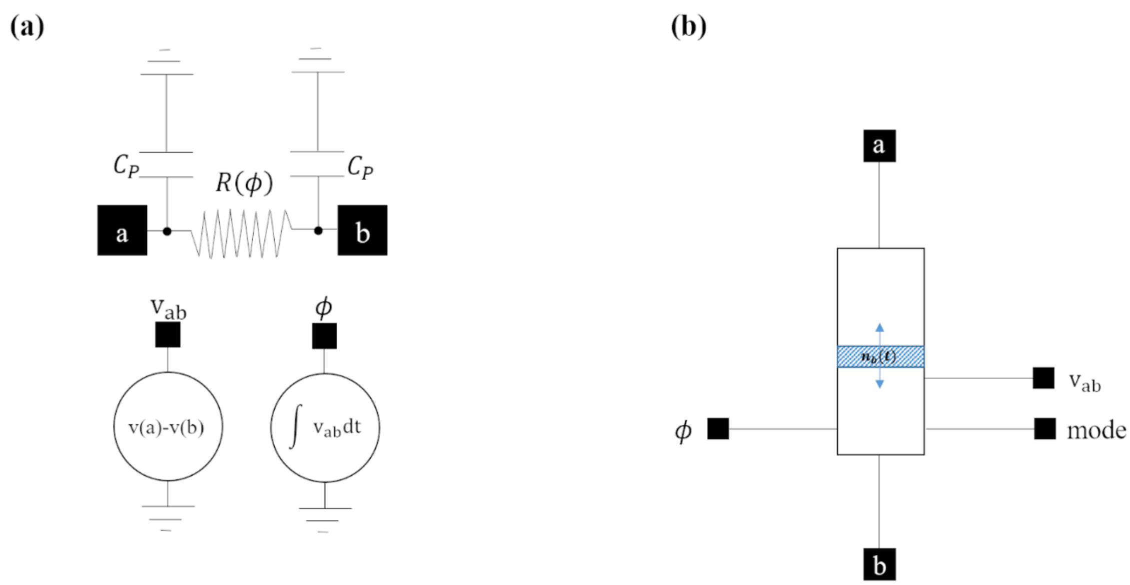

Fig. 4.2 Generic SPICE model.

4.4 Relaxation oscillators

4.4.1 Background

This dissertation has explored a variety of circuits in the computational and SPICE domains. A first exploration in computational circuit modeling showed the expected automatic bandwidth reduction and noise suppression in a memristive low pass filter [33]. The first SPICE model exploring the proposed modeling construct from Fig. 4.2 was used to implement an R-M-R relaxation based multifunction oscillator [60]. That circuit used the justification provided by (4-7) to implement $R(t) = R_0 + abs\left(\frac{R_{max}}{R_{min}}\ \phi\right)$.

Relaxation oscillators are nonlinear and produce square waves. Triangular waveforms may be obtained as an intermediate output. Relaxation oscillators find application in digital clock generation, monostable pulse generation, pulse width modulation etc. Memristor based relaxation oscillators are an active area of research. This is because using a memristor allows constructing time-constant generators using only scalable memory resistors without needing capacitors. Capacitors tend to take up large layout area in CMOS.

Zidan et al. presented one of the initial memristor based reactanceless oscillator designs [63]. Zidan et al. employ an architecture where the output of a digital AND gate drives the memristor whose output is compared to a specified threshold by two comparators. Lu et al. present an active current conveyor-based emulator that functions as an oscillator [64]. Ranjan et al. present a Chua's oscillator which is an active circuit implementation of memristive characteristics [65]. Li et al. present a memristive chaotic oscillator [47]. Their system is modeled like the Lorenz equations traditionally used to demonstrate chaos. The specific model for the memristor implements a positive feedback mechanism. Fouda et al. present a two-gate oscillator with two operational amplifiers [66], a variation on Zidan's original reactanceless oscillator. Corinto et al. have studied memristor oscillators as dynamical systems [67].

4.4.2 Abel model-based relaxation oscillator

The first study with (4-7) was the implementation of a multi-function generator [60]. The specific model used to represent the memristor was motivated by Biolek's work which suggested that Abel differential equations could model memristors [30]. An Abel differential of the first kind has the form, $y' = f_0 + f_1\, y + f_2\, y^2 + f_3\, y^3, f_3 \not\equiv 0$ [68]. Here, y and f are functions of t; the derivative is w.r.t t. Consider a practical case where $f_0 = f_2 = 0$ and $f_3 \ll 1$ such that $f_3\, y^3 \to 0$ and can be ignored from an engineering perspective.

$$y' = f_1\, y \tag{4-9}$$

Let $y = m\, f_0 \int_0^T v(t)\, dt$, where m is a free tuning variable and f_0 represents the natural frequency of the memristor. The applications presented in this dissertation are relaxation oscillators where each half cycle can be visualized as applying a DC voltage of either positive or negative polarity across an R-Memristor-R topology. The "R" is a traditional passive resistor. This DC voltage causes the voltage across the memristor to evolve as a *ramp* for small amplitudes; suggesting $v(t) = t$ in any half cycle. For a DC stimulus, (4-9) evaluates as follows.

$$y' = m\, f_0\, T \tag{4-10}$$

$$y = \frac{1}{2} m\, f_0\, T^2 \tag{4-11}$$

The governing equation (4-9) is satisfied when the coefficient f_1 is,

$$f_1 = \frac{2}{T} \tag{4-12}$$

The coefficient necessary to satisfy the equation for any stimulus can be calculated if the function representing the resistance is known. Another nonlinear functional representation for $R(t)$ is $R(t) = R_0 + e^{m\, f_0\, \int_0^T v(t)\, dt}$; where R_0 is the initial low resistance. Checking for Abel compliance is easy when flux computation is treated as an indefinite integral so that the derivative can be determined.

$$R'(\phi) = 2\, m\, f_0\, R_0\, t\, e^{m\, f_0\, t^2} \tag{4-13}$$

$$f_1 \boldsymbol{R(t)} = \frac{2\, m\, f_0\;\; t\;\; e^{m\, f_0\, t^2}}{R_0 + e^{m\, f_0\, t^2}}\;\left(\boldsymbol{R_0 + e^{m\, f_0\, t^2}}\right) \tag{4-14}$$

Equation (4-14) confirms that for $f_1 = \frac{2\, m\, f_0\;\; t\;\; e^{m\, f_0\, t^2}}{R_0 + e^{m\, f_0\, t^2}}$, the proposed function $R(t)$ satisfies the Abel equation of the first kind. Fig. 4.3 validates that the proposed function that satisfies the memristor equation, does produce the correct response. For an input sine wave (black, broken line), the electric flux (red, dot-dash) peaks at the half cycle and reduces to zero at a full cycle. The resistance exhibits a minimum and maximum as expected. The response in Fig. 4.3 was generated computationally with $R_0 = 1$, $m = 1$, $f_0 = 1$ and $v(t) = \sin\,(t)$ at a stimulating frequency of $f_s = \frac{1}{2\pi}$.

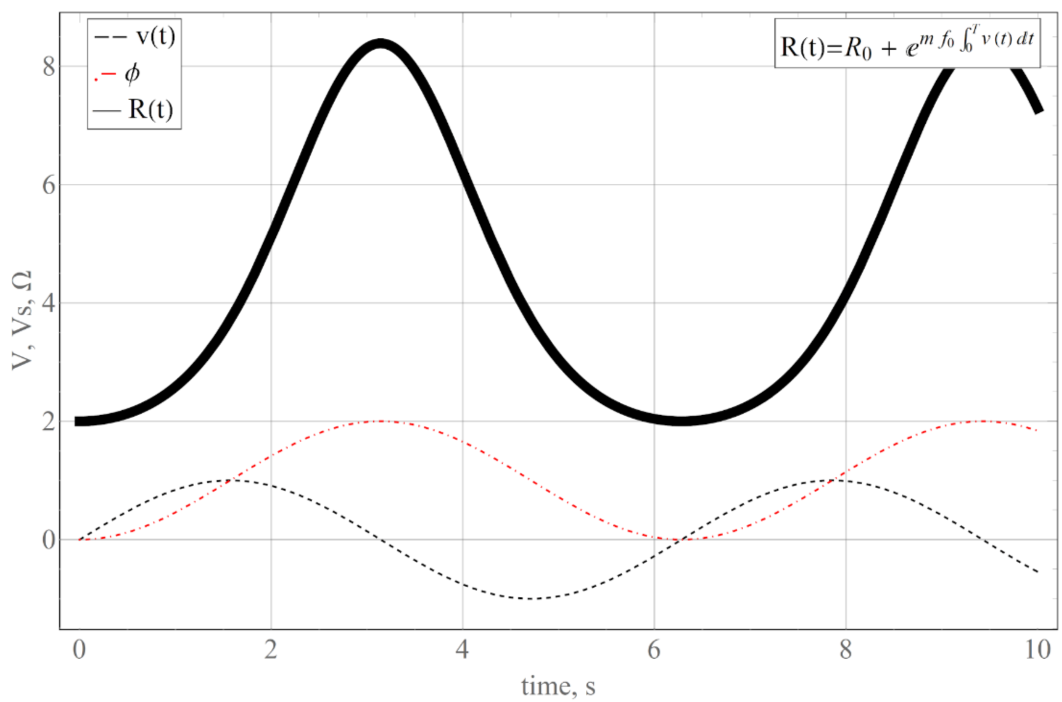

Fig. 4.3 Response of Abel based memristor model.

4.4.2.1 Circuit analysis

In the Abel circuit model, the memristor is modeled with $R(t) = R_0 + e^{m\, f_0 \int_{t=0}^{T} v(t)\, dt}$. Here R_0 is an initial minimum resistance. The polarity of the memristor model does not affect the results because the model will always initialize from a low resistance and evolve toward the high resistance.

The multifunction oscillator circuit is in Fig. 4.4. The circuit can be visualized as consisting of three main building blocks namely the time-constant generator, the comparator and switches to control signal flow. The comparator has two inputs. The negative input is fed with a reference voltage v(ref). The positive input is connected to one of two pins of the memristor such that the output will toggle when the selected input crosses the reference threshold. Switches SW2 and $SW\hat{2}$ are arranged such that they route the correct pin of the memristor into the positive input of the comparator.

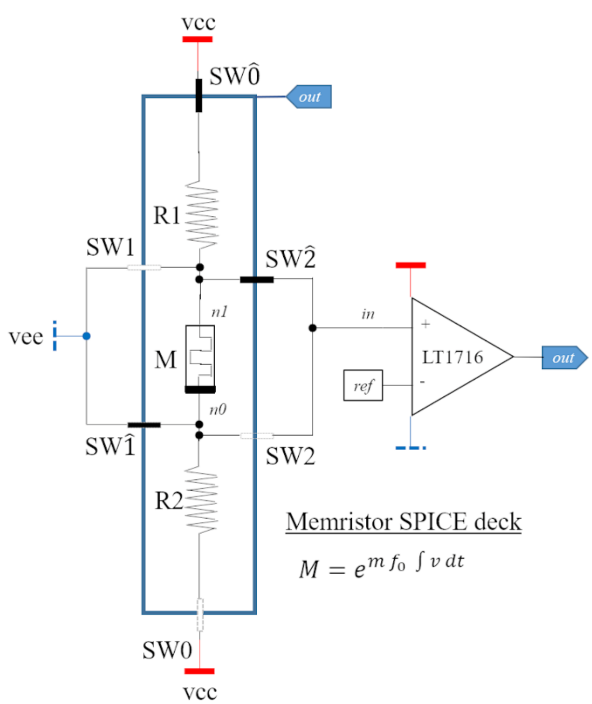

Fig. 4.4 Multifunction oscillator in SPICE.

The reference v(ref) is a single value. The design relies on inherent comparator offset to detect and switch states. The listing of component values is provided in Table *4.1*. The switches are only specified for their typical ON resistance as found in their respective datasheets. The resistors R[2:1] were specified as 1% tolerance and 0.1W rating. The power supply was implemented with an ideal voltage source.

Table 4.1 Table of component values for the Abel oscillator.

#	Component	Symbol	Unit	Value
1	Resistors	R1, R2	kΩ	1
2	Switches, True	ADG1612 $SW[2:0]$	Ω	1
3	Switches, Complimentary	ADG1611 $SW[\hat{2}:\hat{0}]$	Ω	1
4	Memristor	M	Ω	Fig. 4.5
5	Power	vcc, vee	V	$\pm$4.5

4.4.2.2 Function

The circuit in Fig. 4.4 is shown with switches $SW[\hat{2}:\hat{0}]$ closed. One can assume that an output low from the comparator closes $SW[\hat{2}:\hat{0}]$ while an output high will close $SW[2:0]$. The time-constant path is vcc-R1-M-vee. The memristor is initially in the low resistance state, due to which the voltage v(in) will be below the reference v(ref). As the memristor increases in resistance, v(in) increases above v(ref). When v(in) exceeds v(ref) by some amount determined by the comparator offset, the comparator output to toggles low to high. This event causes $SW[2:0]$ to close and opens $SW[\hat{2}:\hat{0}]$. The active time-constant ladder is now vcc-R2-M-vee; forcing the memristor to alter its state from high-resistance to low resistance. This transition causes v(in) to decrease. Once again when v(in) falls below v(ref) by some offset, the comparator output transitions high to low. Thus, a full cycle of oscillation is complete and continues to repeat. The transient response is confirmed by the SPICE plot of Fig. 4.5 where the input to the comparator is a triangular wave and the output is a square wave as expected. The subsequent Fig. 4.6 documents the effect of input common mode on output frequency.

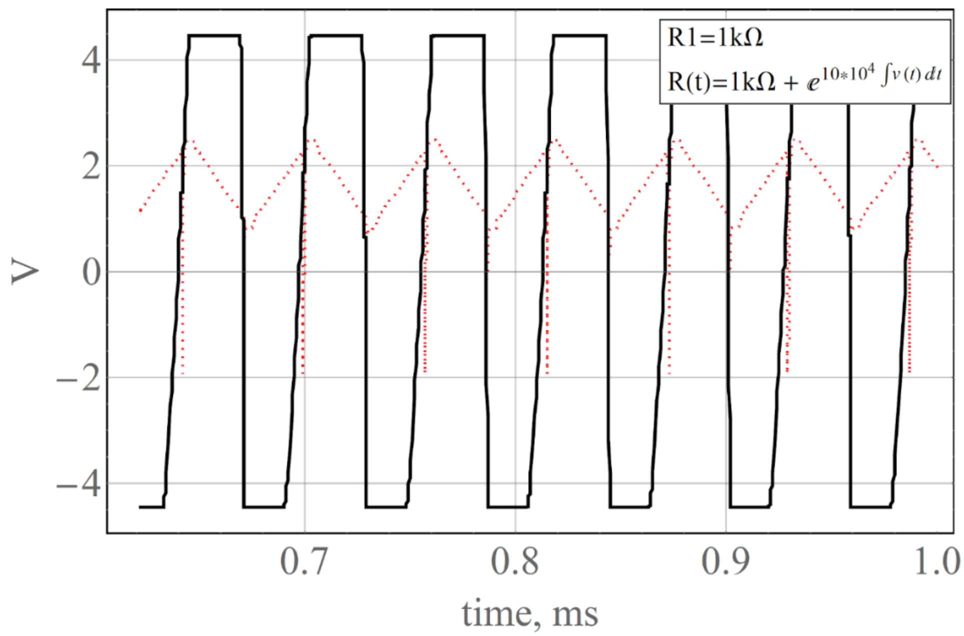

Fig. 4.5 Oscillator input and output.

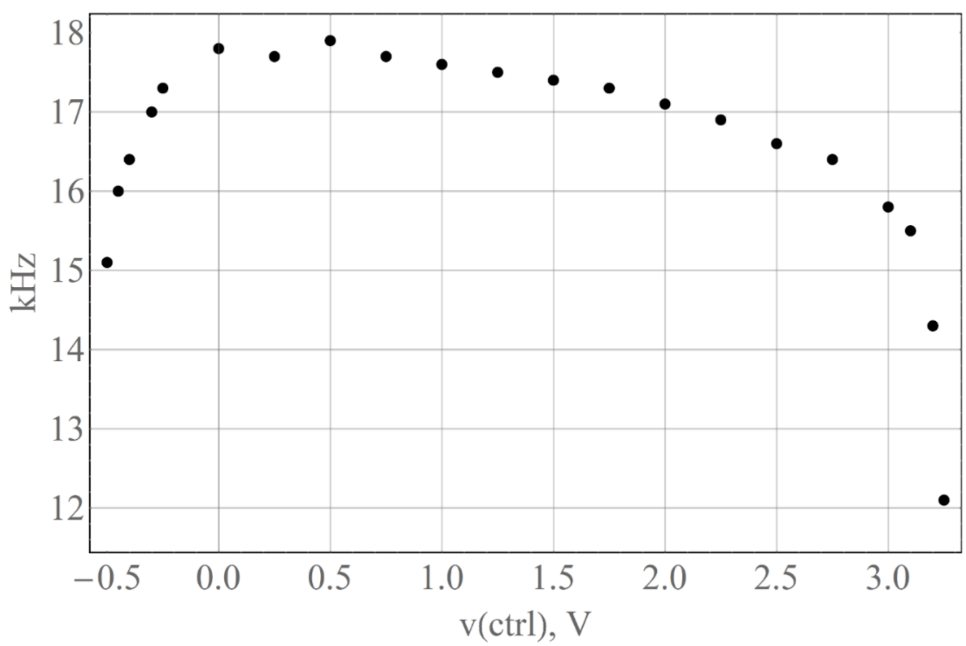

Fig. 4.6 Frequency vs. control voltage for multifunction oscillator.

Fig. 4.6 demonstrates that when the common mode is "virtually" controlled by the v(ref), the oscillation frequency changes. Palmer has demonstrated that comparator offset increases as the input common mode of a signal approaches the power supplies [69]. The memristor oscillator's frequency decreases when the control voltage deviates from the center of the power supplies. This is expected because the increasing offset requires that the voltage on (n0, n1) transition a wider (offset) dead band; resulting in a larger transition time or equivalently lower frequency. A circuit as in Fig. *4.4* could be used as a simple, compact indicator for the onset of common-mode induced offsets.

4.4.3 Logistic model-based relaxation oscillator

This dissertation improves upon [60] to study a power and reliability aware R-M-R relaxation oscillator where the memristor uses the logistic model [43]. Consider Fig. 4.7 showing the proposed oscillator in each of the two possible states. The design is composed of three distinct building blocks. The following discussion references Fig. 4.7 (a). The power supply is composed of the positive vcc and negative vee where vee = -vcc.

Component U is a comparator that produces an output in response to the difference between the input nets net-mem and net-ref. Whenever v(mem) > v(ref), v(out) is vcc. Conversely, for v(mem) < v(ref), vout is vee. The core of the design is the time-constant circuit composed of R1-M-R2. The comparator responds to the voltage at one end of the memristor M, compared to a reference voltage. The switches multiplex the appropriate power supply into the R-M-R ladder, route the correct threshold voltage into the comparator and tap the correct end of M into the positive input of the comparator.

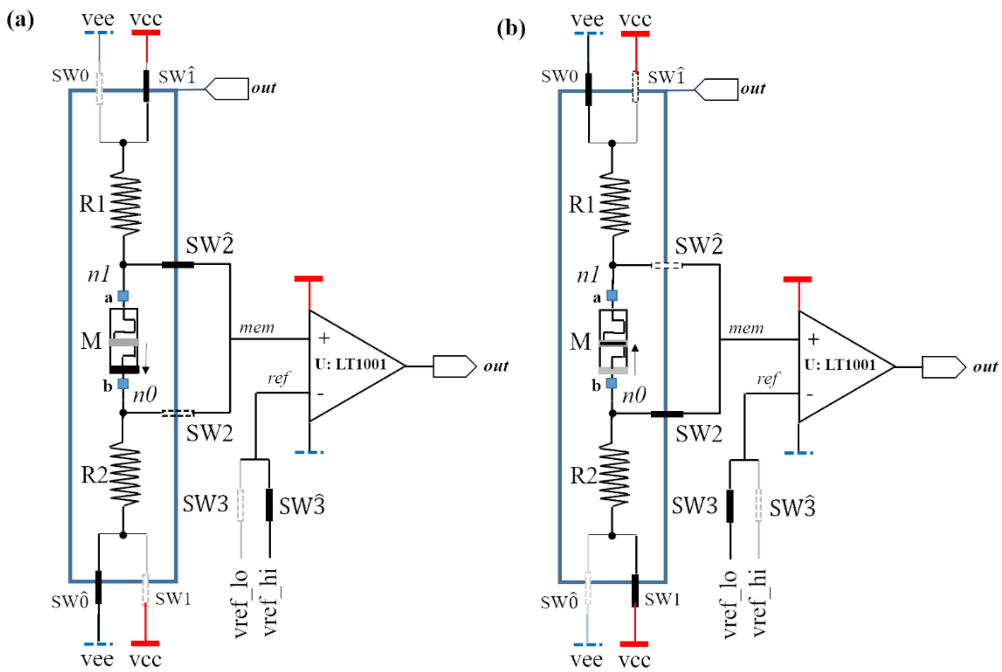

Fig. 4.7 The R-M-R relaxation oscillator.

The active path at any given time is either vcc-SW1̂-R1-M-R2-SW0̂-vee or vcc-SW1-R2-M-R1-SW0-vee. The net with the higher potential from among (n0, n1) is switched into the positive input of the comparator.

This floating memristor design guarantees that the current in the device is bi-directional over a full cycle. This mitigates the damaging effects of electromigration in a practical integrated design. When current constantly flows in one direction integrated structures suffer erosion of physical material resulting in opens in metals, bridging between adjacent lines, localized heating and increased resistance; all of which can alter circuit response compared to the intended design. Integrating memristors into very large scaled integrated circuits is an active area of research [70], [71], [72] that can benefit from the proposed reliability aware design practice.

The use of a single comparator U minimizes active components and reduces power consumption. Integrated CMOS switches with minimal on resistance, were chosen for the simulations. The complete listing of component values as implemented in LTSpice is shown in Table 4.2.

Table 4.2 Table of component values associated with Fig. 4.7.

#	Component	Units	Value	Tolerance	Notes
1	Vcc	V	$\pm$3V	NA	Ideal
2	Comparator	NA	LT1001		
3	Resistors R#	Ω	1k	$\pm$1%	Generic
4	Switches	NA	ADG1611 ADG1612	-	
5	Memristor	NA	Function	-	Custom

4.4.3.1 Circuit analysis

Any floating device design adds an additional level of complexity due to temporally evolving voltages at both device pins. In this design, the memristor must respond to the integral of the voltage across the pins. Consider Fig. 4.8 (a) where the memristor is connected to the dual power supplies through fixed resistors. The nets (n0, n1) will evolve as shown in Fig. 4.8 (b); diverging nonlinearly around the imaginary virtual ground and asymptotically approach the final values which will be determined by simple voltage division. As visualized in Fig. 4.8 (b), it is now possible to locate a nominal value $vmid$ and assign a threshold around it at $vmid \pm va$. Fig. 4.8 (c) superimposes a triangular wave on the linear portion of the swing from $vmin$ to $vmax$. The switching thresholds can be controlled by using a comparator whose high threshold is $vmid + va$ and low threshold is $vmid - va$.

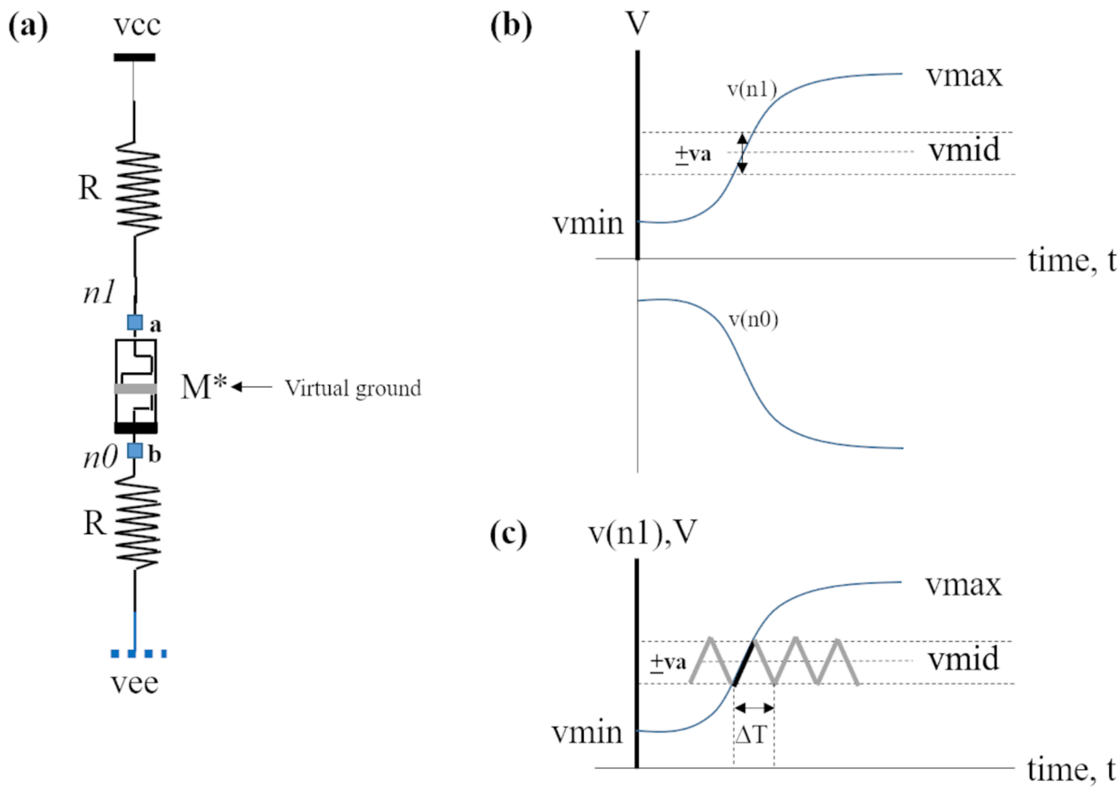

Fig. 4.8 Deconstructed R-M-R ladder for analysis.

The voltage across the device follows from simple voltage division.

$$v_{ab}(t) = (vcc - vee)\frac{R(t)}{2R + R(t)} \tag{4-15}$$

The minimum and maximum voltages across the memristor are,

$$\big(v_{ab}(0), v_{ab}(\infty)\big) = \left((vcc - vee)\frac{R_{min}}{2R+R_{min}}, (vcc - vee)\frac{R_{max}}{2R+R_{max}}\right). \tag{4-16}$$

In (4-16), R_{min} and R_{max} can be determined from experiments. Equation (4-15) can only be solved numerically after substituting (3-1) for $R(t)$. A continuous function $f(t)$ can be fitted to the numerical solution and subsequently manipulated. The time derivative of the function $f'(t)$ is the rate at which the voltage evolves across the device. From Fig. 4.8 (c),

$$f'(t)|_{t=0}\left(\frac{\Delta T}{2}\right) = 2\ va\ . \tag{4-17}$$

In (4-17), the only unknown quantity is ΔT; since $f(t)$ is known from the curve fitting exercise and va is known from the high and low thresholds that are applied into the comparator. A fit of the order 8 returned the following polynomial.

$$f(t) = 2.01 + 1538.10\ t + 7509021.54\ t^2 + 2.21 \times 10^{10}\ t^3 - 1.01 \times 10^{14} t^4 + 1.35 \times 10^{17} t^5 - 8.71 \times 10^{19} t^6 + 2.76 \times 10^{22} t^7 - 3.47 \times 10^{24} t^8. \tag{4-18}$$

The computed frequency of oscillation is,

$$f_{osc} = \frac{f\prime(t)}{2(2\ va)}\,. \tag{4-19}$$

Consider Fig. 4.9 which shows a comparison between the estimated oscillator frequency and that measured from a SPICE simulation. Computation is straightforward and based on (4-19). Given that the SPICE waveform is a square wave, the FFT feature in LTSpice was used to locate the fundamental frequency of oscillation. Therefore the said comparison is between the computed f_{osc} from (4-19) and the fundamental frequency estimated from the FFT of the square wave. The FFT was evaluated after discarding the first 10s of cycles. Nevertheless, some insignificant residual error from finite edge rates is to be expected. For example, repeating the experiment with a higher bandwidth comparator that produces sharper edge rates will result in different numbers; but certainly not different enough to alter the inferences.

Fig. 4.9 shows that the frequency of oscillation is inversely proportional to the amplitude of oscillation, as expected from (4-19). It is also observed that the fit is better at lower frequencies or higher amplitudes.

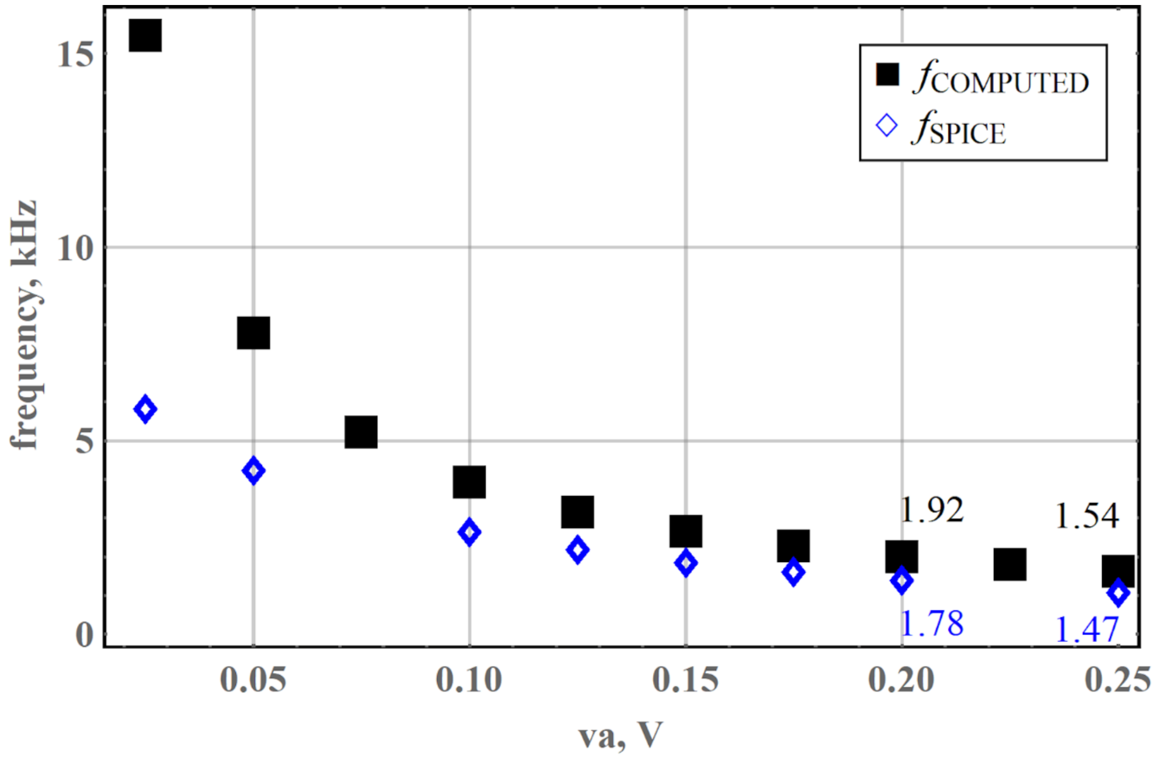

Fig. 4.9 Computed frequency of oscillation compared to SPICE response.

This is attributed to the following practical circuit limitations.

- The comparator in the circuit is gain-bandwidth limited at greater than 1 kHz according to the datasheet.
- Parasitic contributors in the SPICE models are not part of the computed estimation, making the computed response have a higher frequency compared to the more practical SPICE based simulation.
- Comparator offset, however minute is proportionally an increasing part of the swing amplitude. This makes the error large at low amplitude and high frequency.

4.4.3.2 Function

The LT1001 comparator that implements threshold detection was chosen for its low offset of $15\mu V$-$60\mu V$. The datasheet recommends that power supply could be as low as $\pm 3.5V$

although the simulations were done with $\pm 3V$ without any noticeable adverse response. All switches were implemented with the ADG 16-series of integrated circuit switches. ADG1611 is of type PMOS and active low enabled. ADG1612 is of type NMOS and active high enabled. The specified on resistance is in the 3Ω to 4Ω range worst case and well below the memory resistance and fixed R resistance values; which are in the 1 kΩ to 3 kΩ range.

As described alongside Fig. 4.2, ideal behavioral components are used to implement the mathematical operations. This usage of behavioral components allows circuit imperfections such as noise figure, bandwidth limitations, input offsets, nonlinearity when operating closer to the power supplies, effect of common-mode on offsets etc. to be ignored. These imperfections should not be a major contributor to memristor emulation; where the objective of the emulation is only to study the memristor model, not circuit performance in the presence of practical device imperfections.

Consider Fig. 4.10 showing the waveforms across the memristor and the comparator output. A triangular waveform exists across the memristor as predicted in Fig. 4.8 (c). The discrete resistor in the simulation is set to $R = 1\ k\Omega$. The memristor model used $R_{max} = 10\ k\Omega$, $f_0 = 1\ kHz$, $c = 9$, and $\phi_0 = 0$. Panel (a) was generated with thresholds spaced 200 mV around a common-mode of 1.5 V while in panel (b), the simulation used reference voltages spaced 250 mV around a common-mode of 1.5 V. Close inspection shows some switching noise on the triangular waveform at the point where it reverses direction. The output of the comparator is a square wave. The switching noise into the comparator is also seen to cause a ledge on the rising and falling edges of the square wave; although there is no non-monotonicity. In both simulations, the duty cycle is an acceptable 52%.

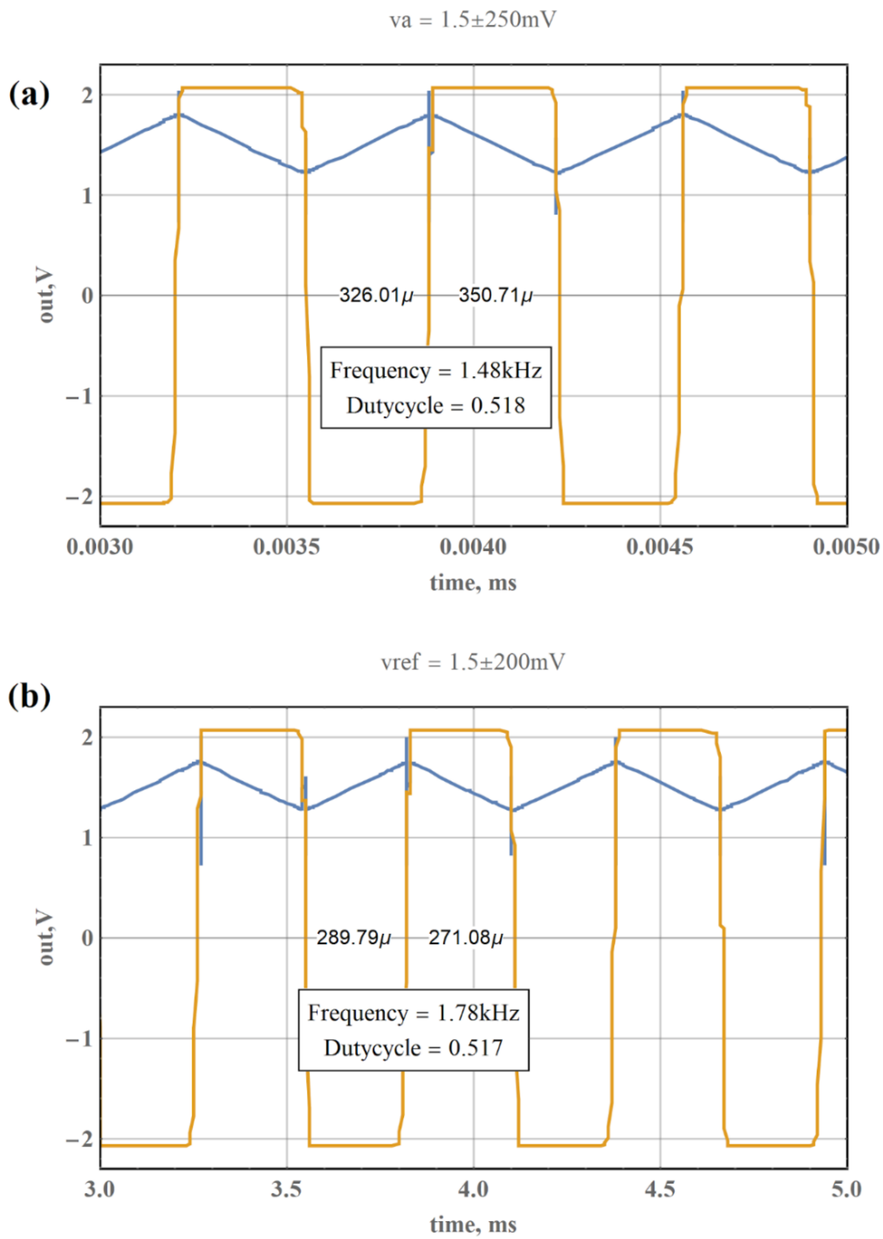

Fig. 4.10 Simulated oscillator output.

Fig. 4.10 plots voltages produced at the internal nets of the oscillator with respect to time. It is also possible to visualize the transfer of resistance between the low and high resistance; resulting in the generic I-V curve.

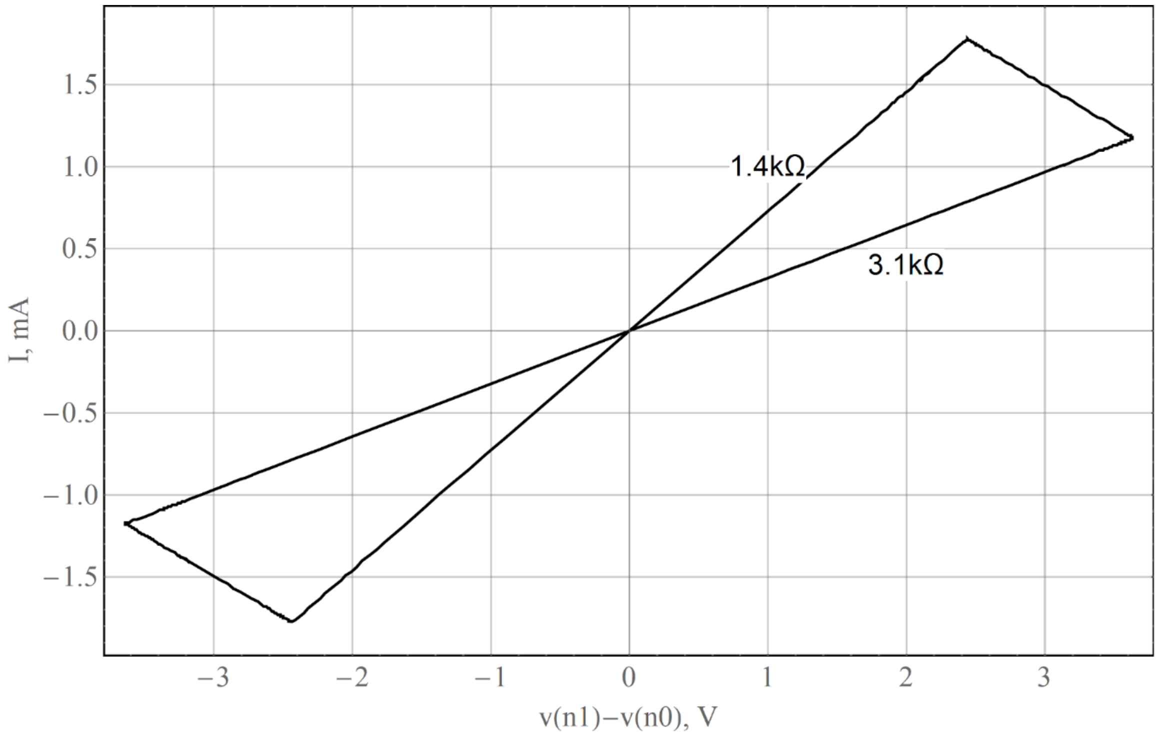

Fig. 4.11 I-V plot of the memristor within the logistic based memristor oscillator.

The oscillator circuit used $R[1,2] = 1\ k\Omega$ and the memristor was implemented using (4-8) with variable values $R_{max} = 10\ k\Omega$, $f_0 = 1\ kHz$, $c = 9$, initial flux $\phi_0 = 0$ and the inconsequential lead capacitance is $C_{mem} = 15f\ F$.

4.5 Scope of the logistic model

4.5.1 I-V curves

The conclusive proof of memristive behavior is the emergence of I-V curves with lobes caused by hysteresis under sinusoid excitation. Unlike traditional active or passive circuit elements, the memristor has no DC I-V curve. The only DC I-V information is a point at (0V, 0A) [73]. Consider Fig. 4.12, demonstrating I-V traces for various stimulus frequencies. The stimulus is $v(t) = 1\sin(\omega\ t)$; where $\omega = 2\pi\ f_s$, f_s being the stimulus frequency. All three fingerprints can be identified from the figure. All lobes are pinched at the origin, satisfying fingerprint 1 (1.3.3.1). Hysteresis loop area is inversely proportional to frequency of excitation, satisfying fingerprint 2 (1.3.3.2). The pinched hysteresis collapses to a single valued function at a frequency *much higher* than the device natural frequency, satisfying fingerprint 3 (1.3.3.3). The region of negative differential resistance (NDR) is pronounced in the device response to 0.1kHz.

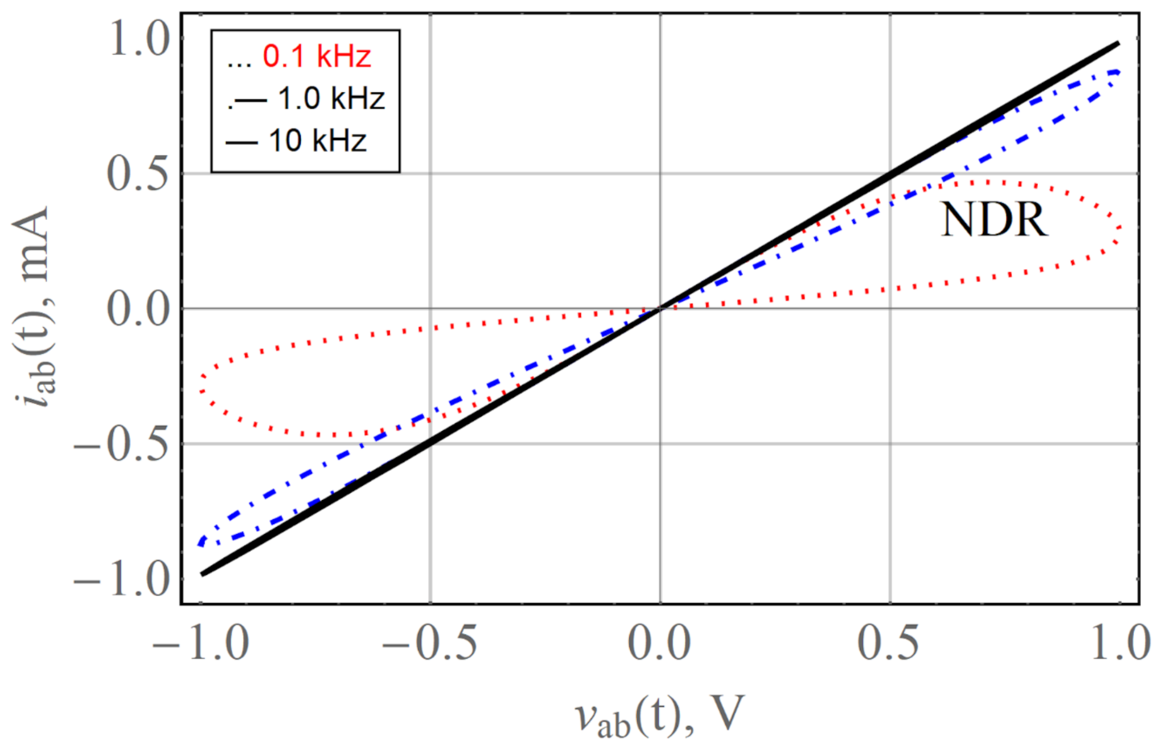

Fig. 4.12 Memristor SPICE I-V.

A reasonable rule of thumb is to consider ten times the device natural frequency as "much higher than the device natural frequency." Fig. 4.12 was generated using (4-8) with memristor parameters set as $s = 1$, $R_{max} = 10\ k\Omega$, device natural frequency $f_0 = 1\ k$Hz, $c = 9$ so that $R_{min} = 1\ k\Omega$, initial flux $\phi_0 = 0\ Vs$ and $C_P = 15\ fF$.

4.5.2 Sensitivity to temperature

Temperature dependence can be introduced into the model through the Einstein-Nernst relation for mobility [38].

$$\mu(T) = \frac{q}{k\,T}\,D \tag{4-20}$$

In (4-20), μ is ion mobility, q is electronic charge, k is Boltzmann constant, D is diffusion constant and T is temperature. Consider Fig. 4.13 that demonstrates the memristor's response to temperature.

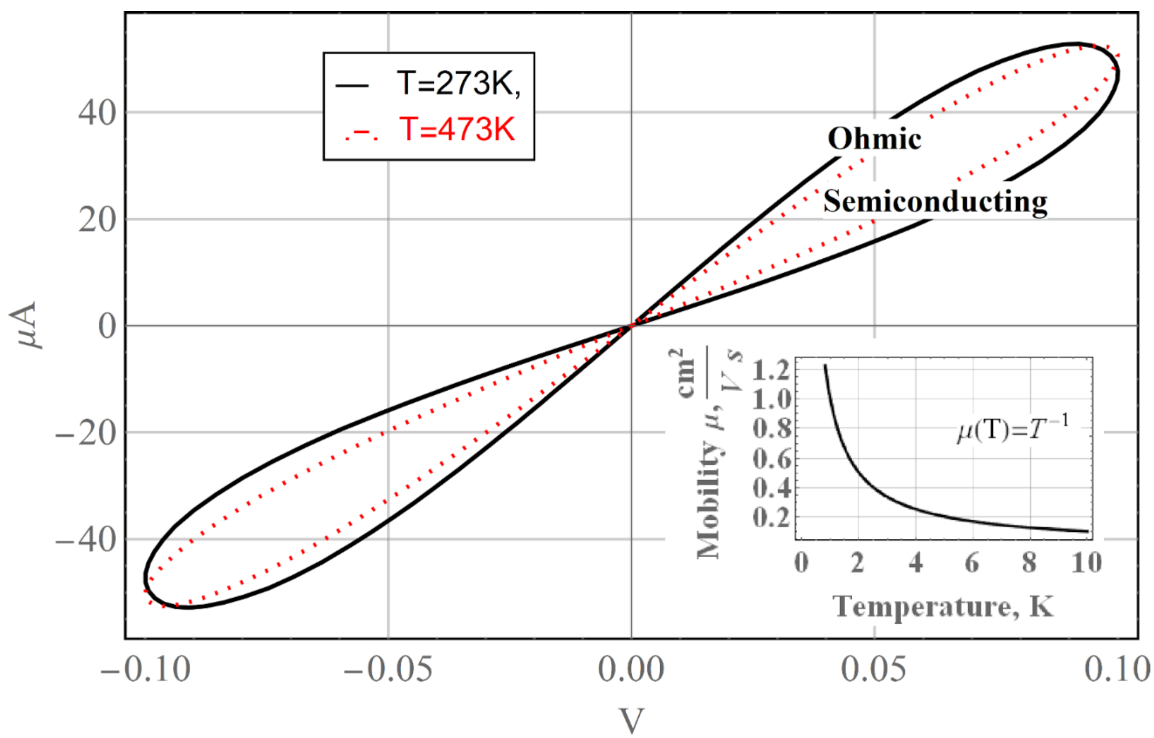

Fig. 4.13 Temperature dependence of the memristor based on the logistic model in SPICE.

The logistic model can accept R_{max} and R_{min} resistances as direct inputs or they can be related to some of the physical parameters of the device as explained in 3.3 after (3-2). Fig. 4.13 was generated with variable values $s = (1 + 10^{-3}T)$, $R_{max} = 10\ k\Omega$, device natural frequency $f_0 = 1\ k\text{Hz}$, $c = 9$ so that $R_{min} = 1\ k\Omega$, initial flux $\phi_0 = 0\ Vs$ and $C_P = 15\ fF$.

The free variable s has been used to model the natural tendency of ohmic material to exhibit a resistance proportional to temperature. The free variable expressed as $s = (1 + 10^{-3}T)$ is an arbitrary choice and can be replaced by any more accurate expression that reflects empirical data. The logistic equation on the other hand naturally captures the semiconducting behavior in the high resistance state, observed empirically by Walczyk et al. [74]. The reasoning for the ohmic and semiconducting response is simple. When the device temperature increase, the ion mobility decreases as predicted by (4-20). Decreased ion mobility manifests as a lower natural frequency of the device. This causes the high resistance to be not as high as with lower temperature. Thus, the lower boundary of the lobe moves up. The natural increase in ohmic resistance, modeled by s will cause the low resistance to be higher, thus moving the upper edge of the lobe lower. The overall result is a narrower lobe.

4.5.3 Current mode operation

Memristors are usually used with a stimulus voltage. Sometimes memristors are operated in current mode where an accurate current is pumped into the device. Researchers have used this type of design to create oscillators or timing storage cells [75], [76]. The current causes a voltage to develop across the device, which in turn results in the migration of ions as per the normal mechanism of drift in the presence of an applied voltage. It is shown below that the logistic model responds similarly in current mode as in voltage mode. Consider the original definition of the memristor, where memristance is,

$$M = \frac{d\phi}{dQ} = \frac{\frac{d}{dt}\int v(t)\,dt}{\frac{d}{dt}\int i(t)\,dt}. \tag{4-21}$$

The RHS of (4-21) shows that the stimulus can be either a voltage as in the numerator or a current as in the denominator. With a steady current sourced into the device, $\int v(t)\, dt$ can be replaced by $\int i(t)\, R(t)\, dt$; which can be just $\int R(t)\, dt$: $i(t) = 1$ for the DC case. This prework allows for rewriting (3-2) with $m = f_0 = 1$ for simplification.

$$R(t) = s \frac{R_{max}}{1 + c\, e^{-\int R(t)\, dt}} \tag{4-22}$$

For the remaining discussion the dependence of R on time is implied; and we will dispense with writing time explicitly as an argument to R. Using the transformation $R^{-1} \to G$, where G represents conductance, and some algebraic manipulation,

$$e^{-\int G^{-1}\, dt} = \frac{s}{c} R_{max}\, G - \frac{1}{c} \tag{4-23}$$

Take the natural log of both sides, differentiate w.r.t time and desensitize any remaining constants that do not play into the results.

$$G'G = 1 - G \tag{4-24}$$

Equation (4-24) is also like an Abel equation of the second kind with $g(x) = f_2(x) = 0$ and $f_0(x) = f_1(x) = 1$ [77]. This is a first order nonlinear ODE of the traditional form $y'y = 1 - y$; which has a known closed form solution [78].

$$G = 1 + W(e^{-1-t+C_1}) \tag{4-25}$$

In (4-25), W is the Lambert function or otherwise called the ProductLog. Fig. 4.14 shows the response of (4-25) computed for G^{-1} to obtain R. Constant C_1 can be used to tune the initial value or minimum resistance. The plot shows the expected sigmoid response similar to the voltage mode excitation. Lambert functions are known to be relevant for modeling memristors, from Biolek's work [30].

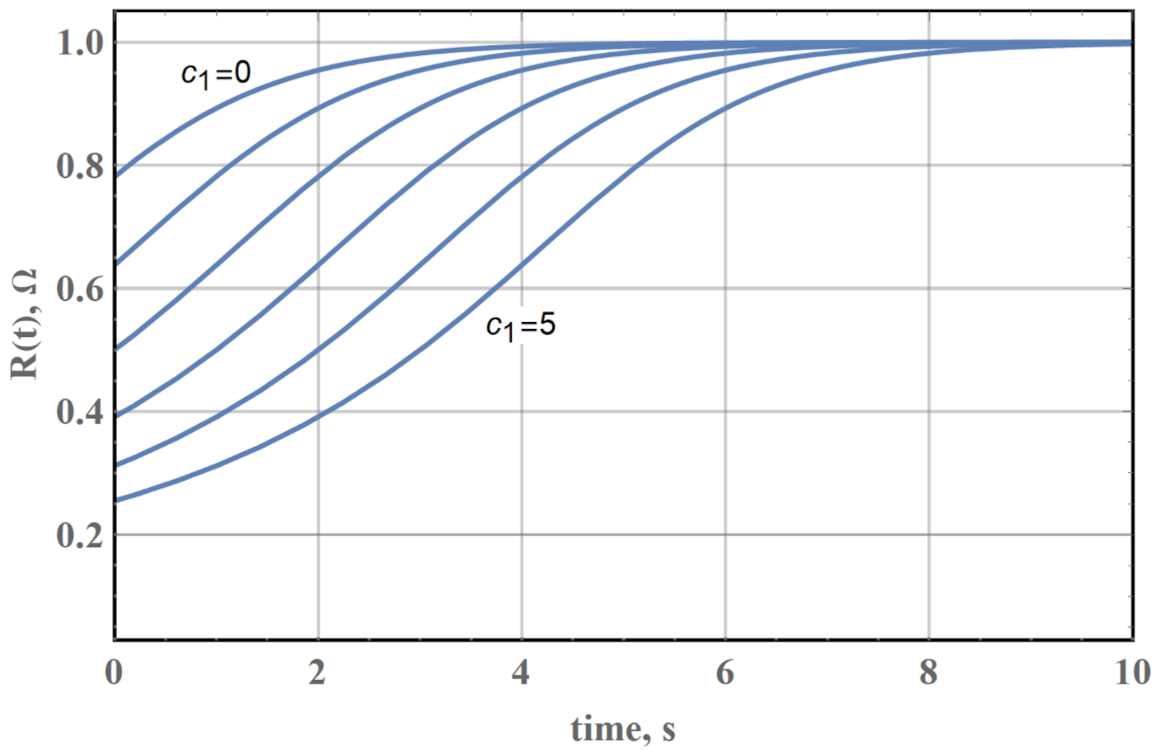

Fig. 4.14 Evolution of memory resistance with a constant current input.

4.5.4 Integration with external nonlinear elements

As evidenced in Fig. 4.12, the memristor model as presented degenerates into a linear resistor at stimulus frequencies much higher than the natural frequency of the device. Empirical data suggests that the collapsed I-V curve may also be nonlinear [22], [74], [79]. Nonlinearity can be introduced into the logistic model by integration into a circuit network that uses nonlinear elements. Recent research suggests that the chemical-metal interface may exhibit a rectifying single valued characteristic at high frequencies [72], [80]. The logistic model can replicate this characteristic when paired with a double-diode circuit. Consider Fig. 4.15 where an I-V lobe at 10Hz is shown collapsing into a nonlinear single valued function at a higher stimulus frequency of 100 Hz. The circuit that produced this effect is shown in the inset. The blue boxed region now represents the new nonlinear memristor model, with external pins ($\hat{a}$, $\hat{b}$).

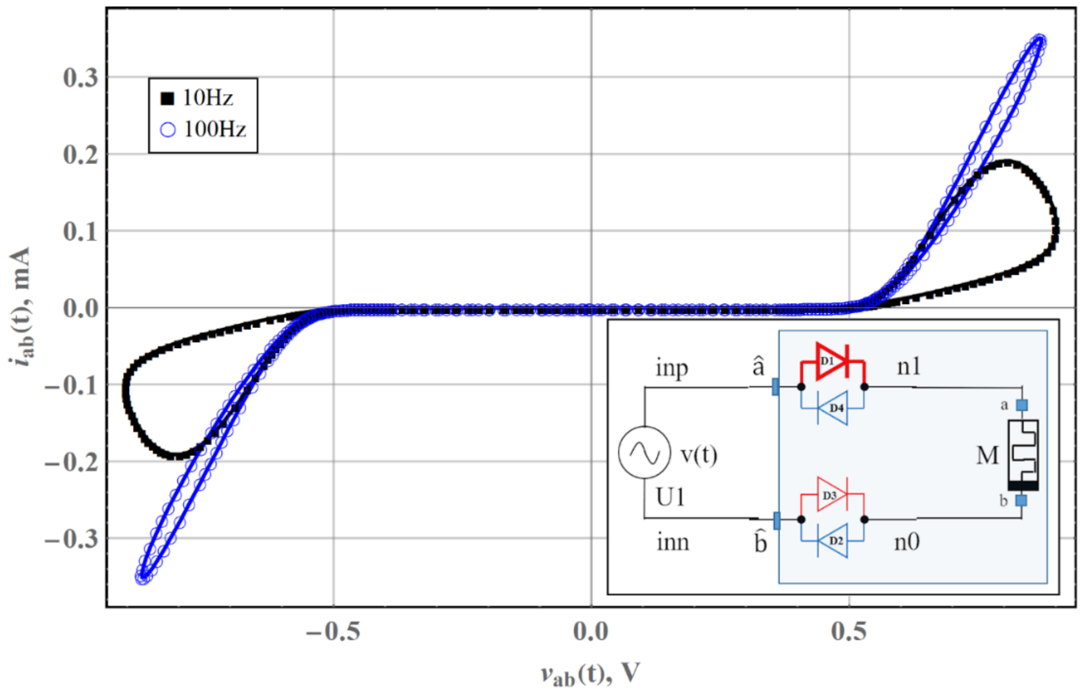

Fig. 4.15 I-V curve of a nonlinear memristor emulator with back-to-back dual diodes.

Fig. 4.15 was generated with $R_{max} = 6\ k\Omega$, $f_0 = 1\ kHz$ and $c = 9$. The circuit used 1N4148 diodes to implement nonlinearity. During the positive half cycle of stimulus, diodes D2-D2 conduct while D3-D4 conduct during the negative half cycle of the stimulus. Floating the memristor ensures that each pin of the device experiences a similar drop from the power supply. The circuit topology is borrowed from Corinto et al. who proposed a passive circuit model for the memristor [81], [82]; although such a passive implementation has been demonstrated to violate basic fingerprints [83]. The proven defect with the passive model does not affect the proposed nonlinear modeling because the core memristor model is the one developed as part of this dissertation and validated in 4.3 and 4.4 using SPICE.

4.5.5 Empirical modeling

Any model is useful when it can be tuned to reproduce empirical data. To verify the usefulness of the logistic model, a curve fit is attempted to Strukov's experimental results. The I-V curve is the response from their Pt-TiO2-Pt device. The logistic model is unable to reproduce the finer details of the hard switching at approximately 0.75V. Transient features during hard switching are influenced by localized electric fields, temperature and mobility variations due to hotspots and characteristics of the chemical-metal interface at the device ends. Being a symbolic model, the logistic abstraction does not and is not intended to model these fine grained interactions. All three fingerprints are evident in Fig. 4.16 where $R_{max} = 2.5\ k\Omega$, $c = 22$, $f_0 = 2\ kHz$ and $v(t) = \sin(2\,\pi\,90\,t)$.

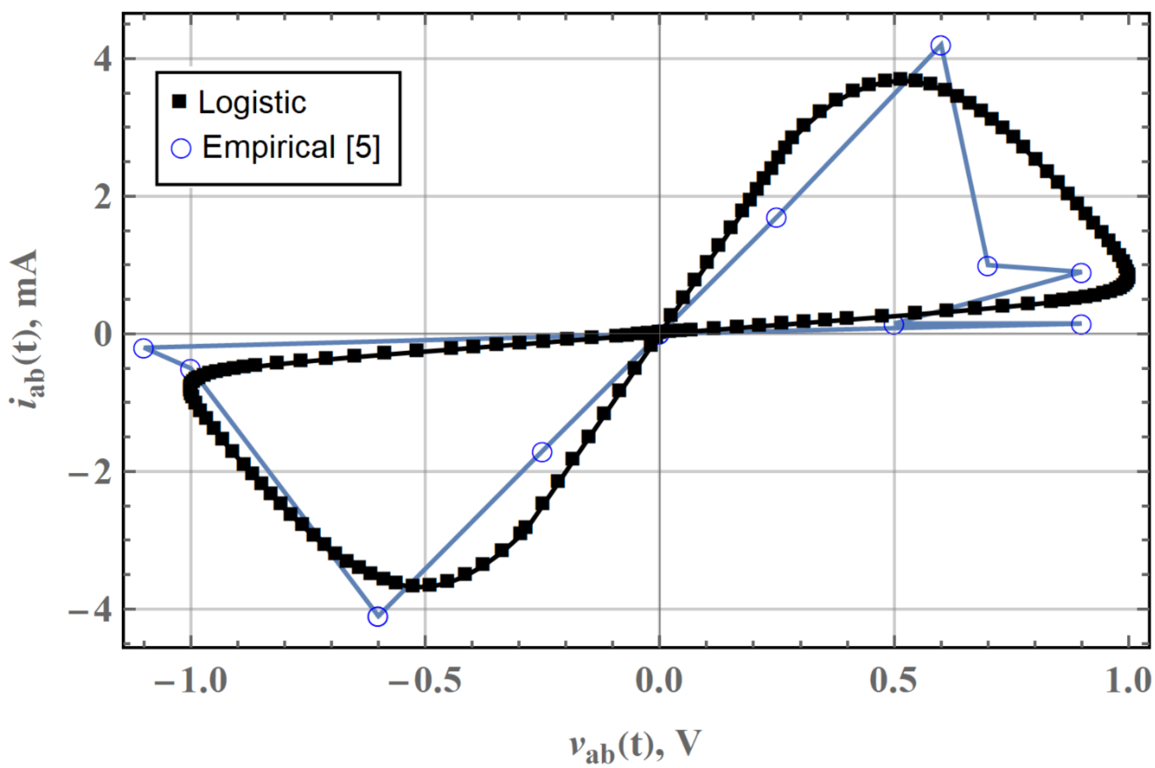

Fig. 4.16 I-V curve fit to Strukov's experimental data for TiO2.

4.6 Chapter Summary

SPICE based modeling is essential to make a new device available to the design community to experiment with. This chapter presented a SPICE model that conforms to the frame work from the computational and logistic modeling; yet is flexible and scalable. The components of the model can be populated with device models of any complexity. The main components are a simple integrator to generate electric flux or the integral of the stimulus voltage and a voltage-controlled resistor. The voltage-controlled resistor has been demonstrated in a non-trivial oscillator circuit with an Abel and finally the logistic model. Chapter 3 presented the ability of the logistic equation and function to demonstrate basic memristor characteristics that other models could not. This chapter has expanded on the scope of the logistic model to include the ability to respond correctly to temperature, produce a voltage when a current mode stimulus is applied and interact with nonlinear circuit elements; all in SPICE. This is a significant improvement to other models in literature.

5 Fundamental Issues

This chapter is primarily a review of the memristor in the context of fundamental passive circuit elements. The discussion is substantially drawn from [34], [43] and [84]. The discussion first creates a framework for clearly identifying fundamental passive circuit elements; which may seem off-topic. However, this is necessary in order to set the backdrop against which research output of this dissertation can be analyzed. The objective is to demonstrate that the nonlinear ion-transport and logistic modeling in this dissertation illustrate that the memristor is neither fundamental nor passive.

5.1 Background

The memristor was postulated as a fundamental passive device in 1971 [1]. A search on IEEE Xplore reveals four publications about memristors in the 36 years from 1971-2007 [1], [7], [85] and [86]. The memristor did not captivate the research community based on this initial response to Chua's original postulate [1]. It took the multi-pronged publication blitz from HP in 2008 to re-energize the topic; whereupon the device claimed a coveted status among the three known fundamental passive circuit elements namely the capacitor, resistor and inductor in that order.

5.2 Fundamental passives

The three fundamental passive devices that a contemporary electrical engineer is familiar with are the capacitor denoted by symbol C in units of farad (F), resistor denoted by symbol R in units of ohm (Ω) and inductor denoted by symbol L in units of henry (H). They are fundamental because none of them can be modeled by any combination of the other two; hence atomic. They are passive because they do not exhibit characteristics like power amplification or negative impedance. For a two pin element, either of these qualities will hint at the ability to produce a current that flows in a direction opposite to an applied potential difference, exhibit dynamic or static negative resistance, power amplification etc. Therefore, the basic question is whether there can be a new fundamental passive circuit element that cannot be produced by any combination of the existing fundamental passive elements.

5.3 Method to locating existing elements

The existing elements can be predicted by applying methods from Newtonian physics to electrical charge which is the fundamental entity in electrical engineering. The mathematical pattern that emerges in locating the existing three fundamental passive elements provides the guidance for predicting and identifying any new fundamental passive circuit element. Newtonian mechanics is applied to represent charge in various states of motion in Fig. 5.1. Lower case notations are used for charge, voltage and current because they can in general be functions of time. Upper case notation denotes a time invariant constant.

Electric charge can exist as a monopole. Charge can therefore be separated from its reference plane by applying some energy to achieve this separation. The work done in separating charge from its reference plane is now the stored potential of the charge. This potential appears as the voltage (V) across the physical entity that maintains separation as in Fig. 5.1 (a). The phenomenological constant that relates charge (Q, coulomb) to voltage (V, volt) is capacitance (C, farad). A capacitor does not produce or respond to a magnetic field.

$$v_C = C^{-1}\, q \tag{5-1}$$

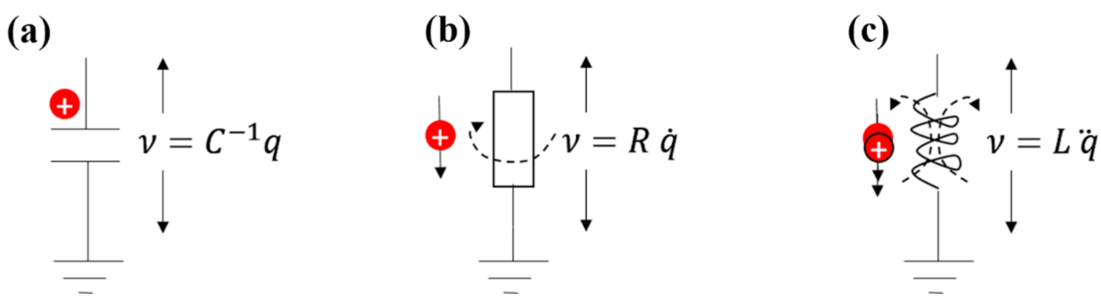

Fig. 5.1 Charge in various states of motion.

Fig. 5.1 (b) shows charges flowing from a higher to lower potential, very similar to the constant speed motion of an object in a viscous medium. The governing equation in its familiar notation is $v = i\,R$. The phenomenological constant is resistance R with the units of ohm (Ω). The relationship in the resistor, in differential over-dot notation follows.

$$v_R = R\,\dot{q} \tag{5-2}$$

A resistor generates a magnetic field in response to the current through the device, but it will not produce a voltage if stimulated with a magnetic field.

In classical mechanics, acceleration is the rate of change of velocity; which in electrical domain is a rate of change of current as in Fig. 5.1 (c). The physical element which converts the rate of current into a potential is the inductor. The phenomenological constant is inductance L with the units of henry (H). The relationship in the inductor, in differential over-dot notation follows.

$$v_L = L\,\ddot{q} \tag{5-3}$$

In addition to generating a time-varying potential across the device pins, the inductor produces a time-varying magnetic field in response to the current through the device. The potential across the device pins can be related to the magnetic flux using Faraday's law. Faraday's law states that the potential ϵ across the inductor is equal to the negative of the rate of change of *magnetic flux* ϕ_B.

$$\epsilon = -\dot{\phi}_B \tag{5-4}$$

The negative sign in (5-4) expresses the idea that the voltage developed across the device is in a direction as to oppose the change in current through the device. This manifests as the very familiar kickback across inductive components. One can also relate (5-3) to (5-4) because both expressions are expressing voltage.

$$\ddot{q} = L^{-1}\left(-\dot{\phi}_B\right) \tag{5-5}$$

The above discussion suggests a two-dimensional sketch to visualize the placement of fundamental devices w.r.t one another in a grid of derivatives of voltage and charge. Such a representation is called the period table of fundamental elements; a terminology attributed to Chua [87]. The rules for filling the cells are,

1. Only one fundamental element can occupy a cell. Rule 1 takes guidance from the well-established periodic table of chemical elements where atomic number is used to populate the grid.

2. Only steady state behavior is admissible to uniquely identify a device. Transitory characteristics are not admissible for uniquely defining a device. Rule 2 follows the existing rules for C, R and L as evidenced by the phenomenological constants in (5-1)-(5-3).

5.4 Periodic table of fundamental devices

A detailed periodic table was developed and published as part of this dissertation in [84]. The discussion in this subsection incorporates improvements arising from further study and to facilitate elegant representation. Fig. 5.2 is the frame of the updated periodic table of fundamental circuit elements. The thick blue dashed center line separates the grid into two halves. The left half serves to locate components that respond to magnetic fields. The right half serves to locate components that respond to electrical inputs. A component such as the capacitor that only responds to charge (or an electric field) will appear only in the right half grid. The cells of the grid will be populated with the standard symbol of the component that satisfies the constitutive relation for a specific cell.

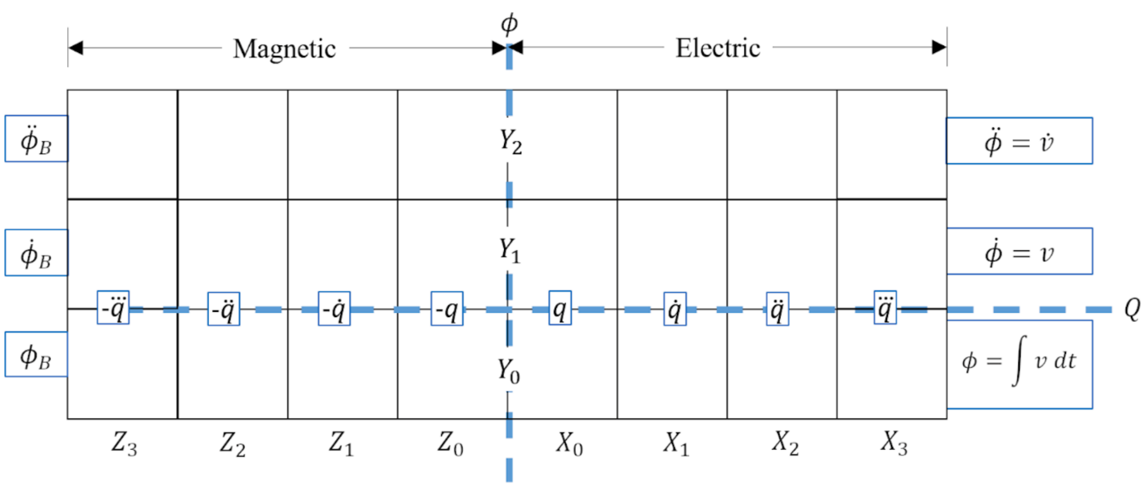

Fig. 5.2 The frame of the periodic table of fundamental circuit elements.

5.4.1 Frame

Fig. 5.2 is presented as an empty frame to stage the introduction of information. The frame of the periodic table is annotated with upper case alphabets X_n along the x-axis and Y_n along the y-axis. The subscript n numbers each segment along the named axis. The subscripting was chosen to start from zero so that the physical quantity associated with that segment of the grid is the nth derivative of the physical quantity; where n is also the subscripting of the frame label. For example, the cell (X_2, Y_2) relates physical quantities ($\ddot{q}$, $\ddot{\phi}$) along its axes.

5.4.2 Axes

The x and y axis are in thick blue dashed lines. The origin is the crossing point of both. The y-axis has two units, the magnetic flux ϕ_B on the left side and the electric flux ϕ on the right side. Each segment of the y-axis plots a successive derivative of the appropriate flux. Electrical flux, defined as the integral of voltage follows from noticing the equivalence from the constitutive relation of the inductor; shown below after integrating the left side from (5-4).

$$\int \epsilon \, dt = -\phi_B \tag{5-6}$$

The memristor community interprets $\int \epsilon \, dt$ as electric flux ϕ; starting with Chua [1]. This association makes it convenient to designate the two y-axis as both flux; magnetic on the left side and electric on the right. On the other hand, it encourages the pitfall of substituting electric flux for true magnetic flux. Such a pitfall results in visualizing an inductor that works without true magnetic flux [88].

The x-axis plots negative and positive electrical charge on either side of the bisecting y-axis. Each segment of the x-axis represents a successive derivative of q, moving away from the origin.

The grid is a graphical expressions-generator. The product of the x-axis quantity and any cell content equals the y-axis quantity.

5.4.3 Existing fundamental elements

Consider Fig. 5.3 which locates the known fundamental passive elements.

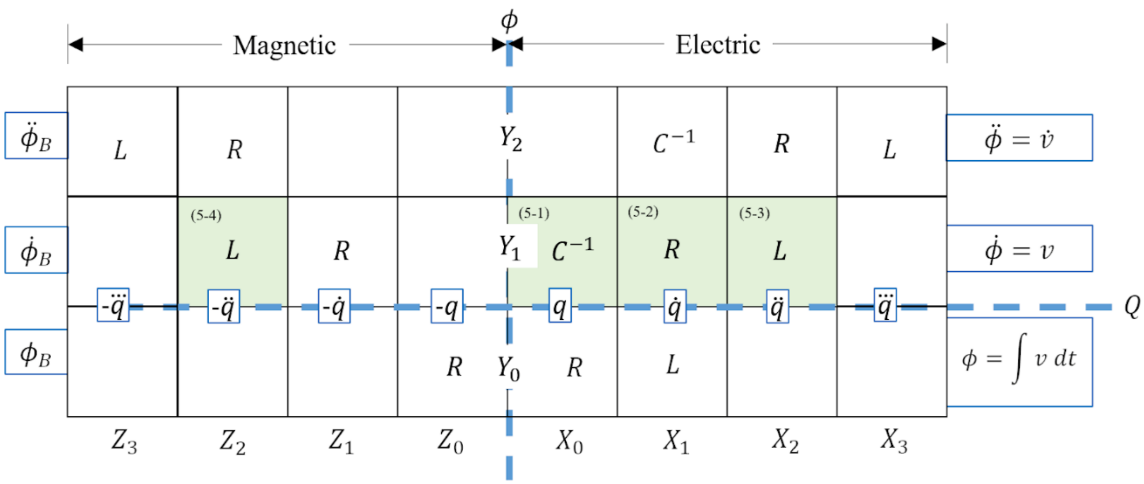

Fig. 5.3 Periodic table with C, R and L located.

In the electric side of the grid, the traditional three fundamental passive elements are found along cells (X_{0-2}, Y_1) which satisfy the constitutive relationship identified by the inset equation numbers. The capacitor exists only on the electric side, while the inductor and resistor make an appearance on the magnetic side as well. Although the resistor appears on the magnetic side, it only produces a magnetic field in response to a current in the device; not vice versa. Therefore, the resistor's box has a white background to indicate that its appearance on the magnetic side does not correspond to a constitutive relation. Only the inductor responds to a magnetic stimulus to produce a current through the device and a potential across the device; and hence appears in its own light green background in cell (Z_2, Y_1). Thus, the inductor has a constitutive relation in the magnetic and electric planes in (Z_2, Y_1) and (X_2, Y_1).

It can be easily verified that rows $(Y_{-n}$:$Y_0)$ and $(Y_2$:$Y_n)$ where $n > 1$, are mathematical abstractions of the fundamental passive elements represented by their true constitutive relationships only along ($X_{-n:n}, Y_1$). Abraham presents a detailed discussion [84].

5.4.4 New fundamental elements

With a well-defined grid, it is now possible to search for the existence of new fundamental elements.

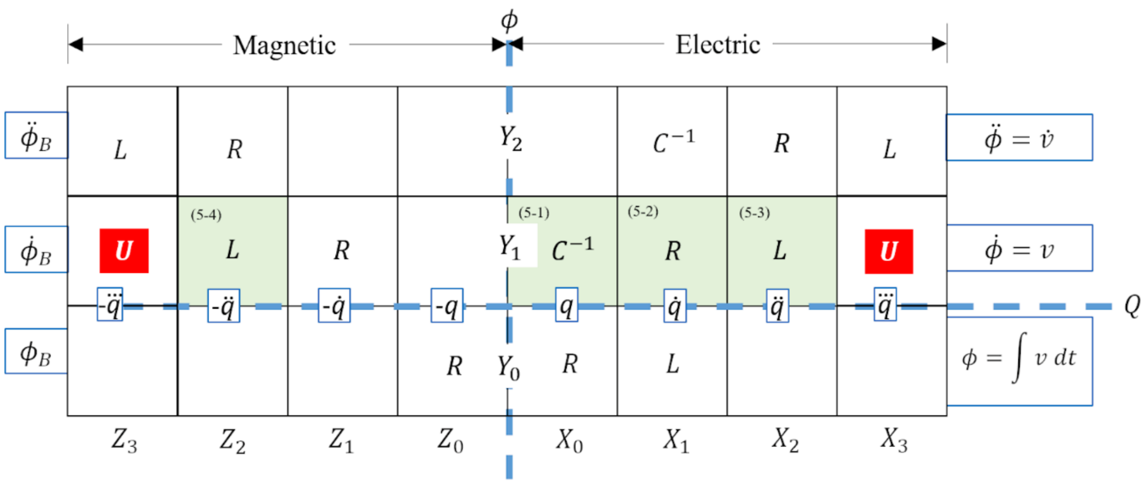

Fig. 5.4 Locating a new fundamental element in the periodic table.

If there is a new fundamental element, it could appear in (X_3, Y_1) with the following constitutive relationship; on the electric side.

$$v = U\,\ddot{q} \tag{5-7}$$

This means that the voltage is $v = U\ \frac{d^2}{dt^2}i$. Consider some scenarios with this hypothetical device.

- If a constant current is pushed into the device, it develops zero volts across it. This is symptomatic of an inductor.
- If a variable current is pushed into the device, the voltage across the device is some function in time. Let this time varying current input be $i = \sin(t)$. The voltage across the device will be $-\sin(t)$. When the current into the device is increasing the voltage across the device is decreasing. Only an active device can do this. A passive device on the other hand would always produce a voltage that opposes the stimulus impressed on it.

It may be that there can be a new fundamental passive device that responds only to magnetic fields. Such a device could exist in (Z_3, Y_1). The constitutive relation for such a device follows.

$$\dot{\phi}_B = U\,(-\ddot{q}) \tag{5-8}$$

Equation (5-8) can be stated in the familiar form, $\dot{\phi}_B = U\left(-\frac{d^2}{dt^2}i\right)$.

- Once again consider a constant current input, to which the hypothetical device responds with 0 tesla; which is an unphysical device that produces zero magnetic field to a current flow.
- If the input is a predetermined example like $i = \sin(t)$, the output will be $\dot{\phi}_B = -\sin(t)$; implying that $\phi_B = \cos(t)$. The interpretation is that when the current is zero, the flux is maximum and when the current is peaked, the flux is zero. Only an

unphysical device with contradicting DC and AC characteristic can occupy the magnetic side cell (Z_3, Y_1).

Such a device with contradicting behaviors cannot be fundamental nor passive. It can be emphatically stated that there are only three fundamental passive devices and no more. Hence the squares $([Z_3,\ X_3],\ Y_1)$ show the hypothetical unknown phenomenological constant U in a red backdrop.

5.4.5 Memristor in the periodic table

Memristance is defined as a rate of change of flux to rate of change of charge, each being a function of time. The expression can be written with each term expressed as a derivative w.r.t time.

$$M = \frac{d\phi}{dq} = \frac{\dot{\phi}}{\dot{q}} \tag{5-9}$$

Consider Fig. 5.5 which shows the memristor in relation to other fundamental devices, based on its constitutive equation in (5-9); placing it in (X_1, Y_1).

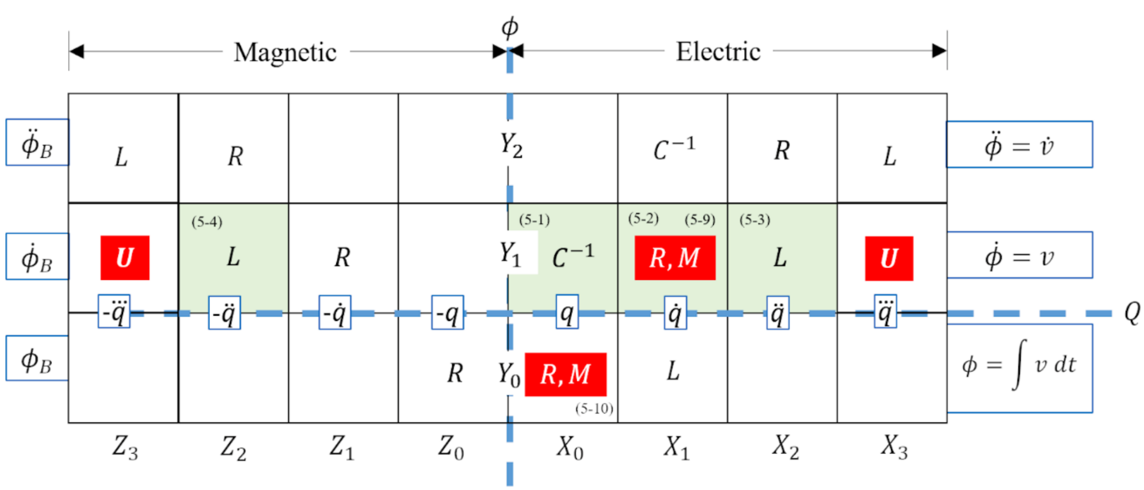

Fig. 5.5 Memristor in the periodic table.

The memristor cohabits with the resistor in (X_1, Y_1) violating Rule 1. Integrating (5-9) produces an expression for memristance in terms of electric flux and charge.

$$M = \frac{\int \dot{\phi}\, dt}{\int \dot{q}\, dt} = \frac{\phi}{q} \tag{5-10}$$

Equation (5-10) places the device in (X_0, Y_0), alongside the mathematical abstraction for the resistor. A strict interpretation of Rule 1 immediately disqualifies the memristor from being a fundamental element. Strukov et al. and others present the memristor located in (X_0, Y_0) in their influential papers [5], [89], [90]. Therefore, this cell merits additional scrutiny.

The examination begins by relaxing Rule 1 such that a newly proposed entity may cohabit with the mathematical abstraction of another device. Within this new framework, the first concern readily presents itself in the form of measurability. Electric potential and current are the only readily measured quantities in electrical engineering. Electric flux or area under the curve is not a fundamental measurement; rather it is an abstract idea resulting from "abstraction by integration" [84]. The mathematical operation of integration requires some form of passive or active computation. Therefore the memristor cannot stand alone as an atomic entity; it must be supported by some other computational element, unlike existing C, R and L. Due to both these objections the memristor must be rejected from occupying (X_0, Y_0) and (X_1, Y_1).

5.5 Atomicity and ion transport

The discussion thus far has been bound to the periodic table; suggesting the need to prop the memristor with computational logic whether active or passive. The ion transport model upon evaluation shows the existence of a negative resistance that torsions in the complex plane [34]. Fig. 5.6 shows a complex plane plot of the DVR model components $R_1(t)$ and $R_2(t)$ from (2-23) and (2-24) respectively; normalized to the maximum resistance. Corresponding points from each component resistance is shown with the same marker. The markers may visually seem to have the same value due to the plot being generated around time $-0.6s \leq t \leq 0.6s$ where the resistance differential is only about 125Ω. The inset true copy of Fig. 2.6 shows the absolute true impedance. In addition to datapoints that torsion in the open complex plane, other data points lie along the real axis where one component is positive and the other negative. Such negative resistances disqualify the memristor from being a fundamental passive. The negative resistance is not a modeling artifact. The physical cause for the negative impedance will be discussed in 5.7 Negative resistance explained.

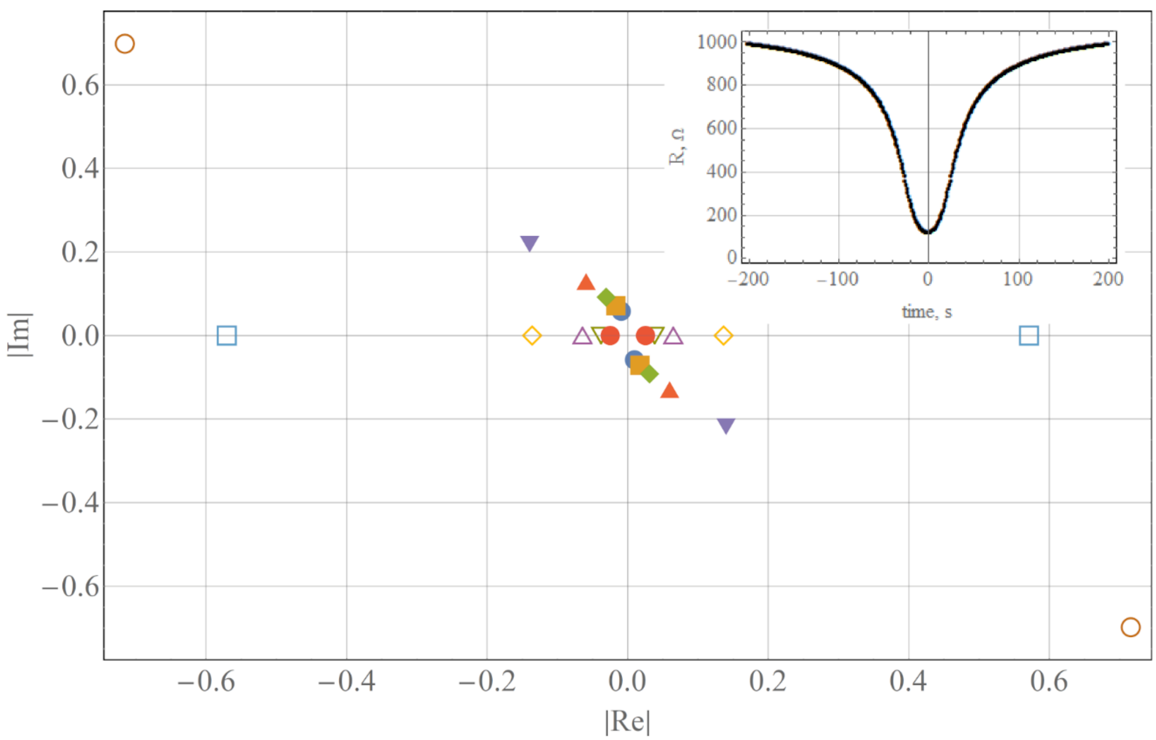

Fig. 5.6 Complex plane plot of DVR model.

5.6 Additional anomalies

A handful of researchers have dismissed the claim of the memristor to be a fundamental passive element, based on theoretical and empirical observations. The concern about integral of voltage being interpreted as flux which can be confused with magnetic flux, as expressed in this dissertation surrounding (5-6) has been voiced by Vongehr et al. [88]. Ventra and Pershin state in their research that sometimes I-V curves may not cross the origin [91]; contradicting Chua's statement that if its pinched, it's a memristor [79]. Sundquist et al. study the memristor from thermodynamic considerations and conclude that the memristor cannot be passive because it violates the second law of thermodynamics [92]. They categorically state that as defined, Chua's memristor is an unphysical device [93]. Violation of Landauer's principle, absence of magnetic flux, ever changing definitions etc. have surfaced as additional objections [94]. The common denominator is that the memristor exhibits the characteristics that cannot be reconciled with a passive resistance.

5.6.1 The passive memristor model

If the memristor is a fundamental element, there can be no combination of existing passive elements that reproduce its behavior. Nevertheless some research has explored and publicized this possibility [81], [82]. This type of model does exhibit hysteresis, but it does not have any memory [83]. This singular point prevents further consideration of this type of circuit. Kiyama et al. point out that all zero crossings after the initial simulation start of this passive circuit do not satisfy fingerprint 2 that requires $(v, i) = (0,0)$. They further discuss that fingerprint 1 might be flawed in its definition; the correct approach being to normalize the calculated area w.r.t the stimulus frequency.

5.6.2 The incomplete statement of fingerprint 1

Fingerprint 1 defines the first signature of the memristor as the pinched hysteresis loop. In the I-V plane it implies (v, i) = (0,0). Chua also presents this relation as the only valid DC I-V characteristic of the memristor [73]. This definition is trivial and includes all passive elements. Furthermore, this definition is incomplete because it includes the cases where a device might exhibit (v, i) = (0,0) but loses memory; invalidating it as a memory resistor [83]. This incomplete statement leads to unsustainable claims like the passive memristor model.

5.6.3 The trivially stated fingerprint 2

Fingerprint 2 states that hysteresis lobe area decreases as frequency increases. The statement is correct, but it is true anytime frequency increases. Consider a sinusoid of the form $v = \sin(\omega\, t)$. The area under the curve over one-unit cycle of stimulus will always decrease with increasing frequency for a fixed amplitude. By inference the area under the curve for a resistor that is stimulated with a sinusoid must also behave similarly. A memristor differs from a simple resistor by virtue of exhibiting amplitude scaling within the half cycle. Consider the I-V plot in Fig. 5.7 where the input voltage is shown dashed black and the current is bold black. The memristor was modeled with the logistic expression. The frequency of excitation increases from left to right.

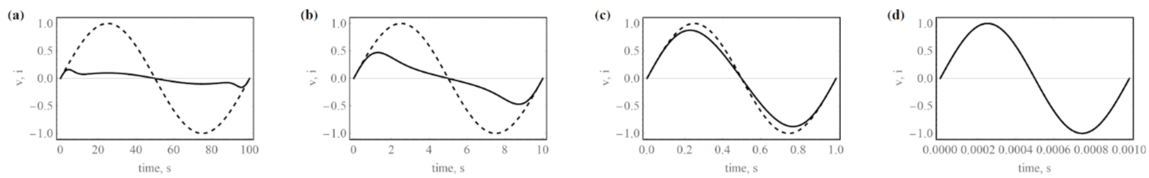

Fig. 5.7 Memristor current- and voltage-time curves.

The lobe in any I-V curve is caused by the differing rise and fall time for the currents in each half cycle. Although a rise-fall difference exists with a half cycle in Fig. 5.7 (a), the area under the curve is small. This translates to a visually small I-V lobe even though the excitation frequency is low. Scanning through the panels, it is observed that the area under the curve for current, increases relative to amplitude of the stimulus although the actual area is decreasing in the time-domain due to increasing frequency. This increase in amplitude relative to the stimulus, coupled with the decreasing area due to the horizontal time shortening results in the *initially increasing*, *then decreasing* area for lobes. These ideas are presented pictorially in Fig. 5.8 using the logistic model where $R_{max} = 10\ k\Omega$, $c = 9$, $m = 1$ and $f_0 = 20\ Hz$.

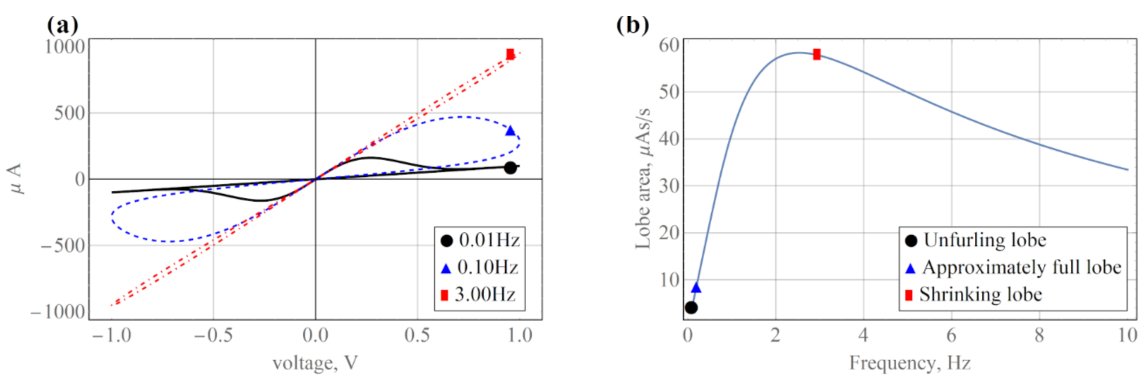

Fig. 5.8 (a) I-V curves over increasing frequencies and (b) lobe area vs. frequency.

In Fig. 5.8 (a) and (b), the corresponding information is located by like-markers. The natural frequency of the memristor was set to 20 Hz. When stimulated with a sinusoid of

0.01 Hz, the unbroken black trace in Fig. 5.8 (a) shows that the I-V curve area is visually small caused by the device transitioning to the high resistance state, early in the cycle. The time-normalized lobe area in Fig. 5.8 (b) is correspondingly small. When the stimulus frequency is 0.1Hz, the I-V curve looks visually large. However, the time-normalized lobe area indicates only a slight increase w.r.t the one at 0.01 Hz. The normalized area peaks at 2 Hz or one-tenth of the device natural frequency, although visually the lobe area in the I-V curve is already decreasing. This visual anomaly in Fig. 5.8 (a) is caused because time is implicit in the I-V plot.

Given that memristors are time-sensitive resistors, the correct method is to normalize the computed area under the current curve, to the time period; upon which it can be observed that the lobe area initially increases, reaches a peak and then decreases to asymptotically zero [83].

5.7 Negative resistance explained

The computational ion-transport model hints at a physical mechanism that can explain the appearance of negative resistance. That mechanism is the movement of the ion-boundary coupled with the fact that the memristor is a two-terminal device. Consider the illustration in Fig. 5.9 which views the memristor from the ion-transport perspective. The y-axis in the plots is the vacancy concentration and the x-axis represents the length of the device. The two plots show ion evolution over time where the device transitions from a low resistance in Fig. 5.9 (a) to some higher resistance in Fig. 5.9 (b). Below each plot is the dual variable resistor model. Panel (a) shows ions distributed evenly throughout the device length causing the DVR model to be two equal series resistors R_1 and R_2 at time $t = 0$.

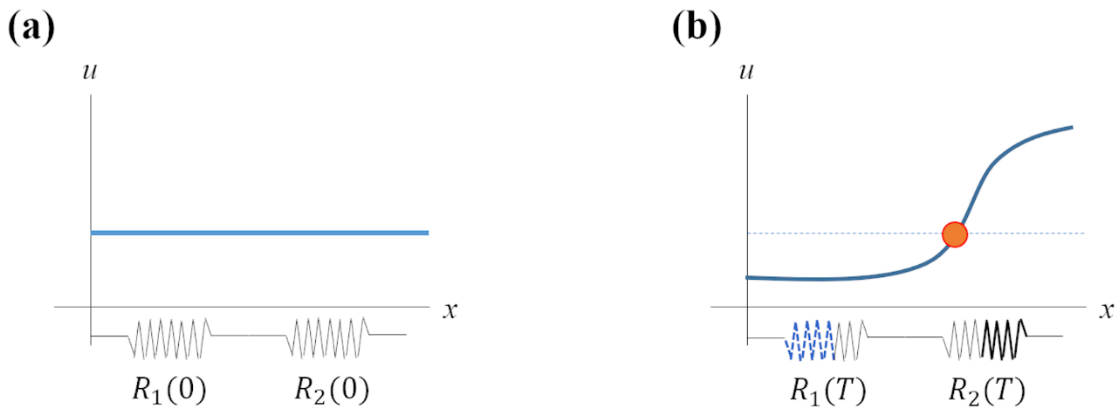

Fig. 5.9 Negative resistance explained by ion transport.

In Fig. 5.9 (b), the ions have gathered to the right end plate under the action of some external voltage at some future time $t = T$. The red dot is the itinerant ion boundary. Ions to the left of the boundary have evacuated to the right. This requires the resistance R_1 to decrease. In a two-terminal model, the only way this can happen is for a negative resistance to manifest and reduce the value of $R_1(0)$ to a lower $R_1(T)$. The negative resistance is indicated in the sketch by the blue dotted segment of R_1. Similarly, $R_2(0)$ must increase to $R_2(T)$; which is indicated in the sketch by thick segment of R_2. The negative resistance is made necessary by the two-terminal construct of the memristor. The presence of the negative resistance makes the device exhibit an anomalous active character. The negative resistance is not an artifact of modeling caused by a mathematical function returning a negative value. It is a necessary physical response due to the two-terminal nature of the memristor.

5.8 What is the memristor?

This dissertation has presented an ion-transport model that displays the emergence of negative resistance within a memristor. The subsequent logistic model does not exhibit negative resistance directly because it is a single expression which does not model the memristor in a DVR form. However, the associated second order governing ODE exhibits nonlinearity and offers an explanation sustained oscillatory solutions associated with active devices and circuits. It can be predicted with reasonable confidence that if the logistic model is split into two parts each emulating one part of the DVR, then the negative resistance will become evident. The challenge is to identify the proper location that can divide the logistic based memristor into two pieces. With the ion-transport model, this divider was easily identified as the ion-boundary.

At its core the memory resistor is a composite circuit where a mux selects between different resistors. Consider the sketch in Fig. 5.10 (a) where a mux selects between a low and high resistance. The integrator U1 is necessary to control the selection process and U2 is essential to implement hysteresis. The implementation in Fig. 5.10 (a) produces the I-V curve shown in Fig. 5.10 (b). Notice the presence of thresholds at v_L and v_H. Kvatinsky et al. incorporate such hard thresholds into their VTEAM model [55]. These features require the use of active elements for implementation.

Memristor emulation has always needed active circuitry [1], [65], [95], [96], [97], [98], [99]. The only exception is the incorrect passive modeling where the I-V curve is pinched but the device loses memory.

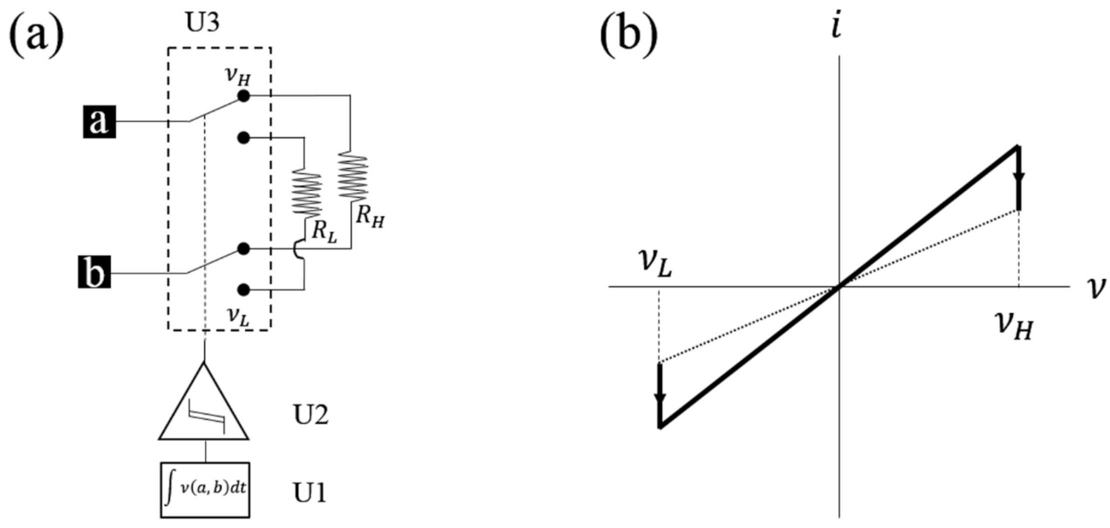

Fig. 5.10 Memristor composite.

5.9 Chapter Summary

This chapter evaluated the memristor's claim about being a fundamental passive element. A periodic table of fundamental elements was generated from basic Newtonian principles. This periodic table is shown to be a superset of the periodic table that proponents use to classify the memristor as a fundamental element. Two simple rules were proposed to test the suitability of a location in the periodic table for locating the memristor. All locations in the periodic table were found to be unsuitable to hosting the memristor. The ion transport model and the logistic model were then re-examined in the context of passivity. Both the models developed in this dissertation were able to correctly predict the anomalous active nature of the memristor. The ion transport model was also able to suggest a mechanism by which this negative resistance manifests.

6 Conclusion and Future Work

This dissertation has focused on contributing to the field of memristor modeling and circuit design. The initial ion-transport PDE model was abstracted to a dynamical logistic ODE and both were successfully used in SPICE circuit simulations that demonstrated a non-trivial relaxation oscillator.

6.1 Conclusion

Devices that have demonstrated hysteresis historically were researched. This was followed by a discussion about HP's memristors in terms of its theory, physical structure, switching mechanism and contemporary modeling strategies. These strategies are found to be haphazard. No researcher has developed a single coherent model such that it exhibits general memristor characteristics sufficiently and is usable in SPICE simulations. This finding served as the motivation for this dissertation.

6.1.1 Computational Ion Transport

The fundamental physical model is adopted to be a two-dimensional structure with ions that migrate between end plates. This led to proposing a life cycle for memristor consisting of active transport based programming and passive diffusive un-programming. Diffusive un-programming is solved using techniques from thermodynamics.

The popular transport equation was simplified to represent the governing equation for active transport under the action of an applied programming voltage. The logistic-like solution was validated and subsequently manipulated to derive expressions that reproduce the rich set of memristive characteristics including resistance.

The significant contributions are listed below.

i. The use of the generic transport equation and a closed form symbolic solution to model ion migration within the device.
ii. The ability to generate derived expressions for ion concentration, resistance, transition time, switching energy etc.
iii. Proving the validity of HP DVR model, which has until now been assumed without proof.

6.1.2 Logistic Model

The solution of the ion transport model is a logistic function. This paved the way for proposing that the logistic function could itself be an expression to model memory resistance. The transition into the logistic model was done through an intermediate Abel ODE. It is shown that the logistic ODE is a special case of the Abel ODE. It was then demonstrated through calculated resistance-time plots that the ion-transport based resistance can be emulated by the logistic function with few tuning knobs. The dissertation proves that the governing equation to this proposed abstracted logistic function model is the logistic ODE. This enables the generation of a discrete logistic map that can exhibit the sensitivity to initial conditions observed in empirical publications.

The primary contributions from this logistic modeling are as follows.

i. Establishing a connection between the ion-transport PDE model and the logistic ODE.
ii. Identification of an ODE that can inherently captures the memristor's nonlinearity and reported oscillatory responses.
iii. The ability to model sensitivity to initial conditions.

6.1.3 SPICE

A SPICE based implementation is essential to validate any theoretical model by applying them easily in circuit networks. A universally applicable behavioral SPICE model was implemented. An Abel ODE model and the logistic model were both deployed into the universal SPICE construct. Both models were used to simulate a relaxation oscillator. The logistic model was exercised to exhibit traditional I-V curves, sensitivity to temperature, current mode operation, empirical data fitting and the ability to incorporate into circuit networks with nonlinear components. This allows the logistic model to be enhanced by integrating it with existing nonlinear components as needed. The oscillator performance was validated over a wide range of operating frequencies against analytical calculations. The impact of common-mode on frequency was computationally predicted, reproduced in simulation and favorably compared against independent literature.

The significant contributions in SPICE are as follows.

i. Demonstrating that the logistic model can be easily represented in SPICE.
ii. Simulation of a non-trivial, low power and reliability aware relaxation oscillator.
iii. Development of an accurate modeling methodology for the relaxation oscillator.

6.1.4 Fundamental Issues

The ion-transport and logistic model enable tackling fundamental and contentious issues associated with memristors. One such is the question whether memristors are truly fundamental passive circuit elements.

The ion-transport model shows that the memristor does resemble the up-till-now assumed dual variable resistor model. The ion-transport model also shows the emergence of negative resistance within the device as a key mechanism that enables transition between resistance states. The two-terminal nature of the memristor that dispenses with a control terminal, makes the emergence of negative resistance inevitable. The ion-transport model also exhibits rich dynamics in the complex plane as predicted by Chua in 1971. This complex dynamics arises from the peculiar property that when a clean zero-crossing sinusoidal voltage is imposed on the memristor, the resulting current does not undergo a full phase shift. The current undergoes variable rate, non-monotonic amplitude transitions within the zero crossing points.

The logistic model displays memristive qualities just like the ion-transport model. It exhibits the occasionally reported sensitivity to initial conditions in addition to all the usual memristor qualities.

Significant contributions in the realm of fundamental issues are as follows.

i. The ability to convincingly report that the memristor is neither fundamental nor passive.

6.2 Future Work

This work is mainly theoretical with a practical SPICE and circuit design component. Therefore, there is ample opportunity to make further progress in multiple areas.

6.2.1 Theoretical

At the current stage of development, the ion-transport model and the logistic model have only been shown to be equivalent by overlaying numerical values for resistance. The transport model has not been shown to exhibit sensitivity to initial conditions. The logistic model on the other hand has not been shown to exbibit negative resistance. Currently the commonality between both is the use of the logistic function to model ion transport and express an abstraction of the resistance. A significant next step will be to explore the theoretical connections between the ion-transport PDE and logistic ODE governing equations.

6.2.2 SPICE

The relaxation oscillator implemented in this dissertation has the obvious advantage that it works from the power supply without loading the output of the comparator. This has the disadvantage that comparator switching noise is introduced into R-M-R network through the gates of the switches. The oscillator network can benefit from the following improvements.

i. The use of full complementary switches to lower the noise coupling.
ii. Edge rate control on the comparator output to reduce switching noise.
iii. Alternate yet-to-be determined architectures that avoid switching the current in R-M-R at the positive and negative peaks of the triangular wave.

iv. Multiple memristor based oscillating networks.

The memristor is hard to describe quantitatively, compared to traditional passive or active electronic components. This dissertation has presented a strong foundation based upon mature transport equations. The research has been modularized into a theoretical modeling component and a practical SPICE implementation. Opportunities for improvement and further development of the model are identified for each module. While the memristor is an electronic device, memristance is a phenomenon that exists at many scales ranging from the monolithic device at micro to cosmic macro scales as evidenced by the analemma curves. It is expected that the methods developed in this research may find applicability in studying the phenomenon at these many scales.

7 References

[1] L. Chua, "Memristor-The missing circuit element," *IEEE Trans. Circuit Theory*, vol. 18, no. 5, pp. 507-519, Sep 1971.

[2] T. Prodromakis, C. Toumazou and L. Chua, "Two centuries of memristors," *Nature Mater*, vol. 11, no. 6, pp. 478-481, 06 2012.

[3] R. S. Williams, "How we found the missing memristor," *IEEE Spectrum*, pp. 29-35, December 2008.

[4] F. Argall, "Switching phenomena in titanium oxide thin films," *Solid State Electronics*, vol. 11, no. 5, pp. 535-541, 1968.

[5] D. B. Strukov, G. S. Snider, D. R. Stewart and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, pp. 80-83, May 2008.

[6] E. W. Weisstein, "Eric Weisstein's world of Astronomy," 1996. [Online]. Available: http://scienceworld.wolfram.com/astronomy/Analemma.html. [Accessed 14 10 2014].

[7] L. O. Chua and S. M. Kang, "Memristive devices and systems," *Proceedings of the IEEE,* vol. 64, no. 2, pp. 209-223, 1976.

[8] R. Waser and A. Masakazu , "Nanoionics-based resistive switching memories," *Nature Materials,* vol. 6, pp. 833-840, November 2007.

[9] T. B. Gruenwald and G. Gordon, "Oxygen diffusion in single crystals of titanium dioxide," *J. Inorg. Nucl. Chem.,* vol. 33, no. 4, pp. 1151-1155, 04 1971.

[10] S. O. Kang, S. Hong, J. Choi, J.-S. Kim, I. Hwang, I.-S. Byun, Y. S. Kim, W. Kim and B. H. Park, "Layer-to-island growth of electrodeposited Cu2O films and filamentary switching in single-channeled grain boundaries," *J. Appl. Phys,* vol. 107, no. 5, 01 2010.

[11] H. D. Lee and Y. Nishi, "Reduction in reset current of unipolar NiO-based resistive switching through nickel interfacial layer," *Appl. Phys. Lett,* vol. 97, no. 25, 11 2010.

[12] R. Waser, R. Dittman, G. Staikov and K. Szot, "Redox-Based Resistive Switching Memories – Nanoionic Mechanisms, Prospects, and Challenges," *Adv. Mater.,* vol. 21, no. 25-26, pp. 2632-2663, 06 July 2009.

[13] H. Schroeder and D. S. Jeong, "Resistive switching in a Pt/TiO2/Pt thin film stack – a candidate for a non-volatile ReRAM," *Microelectron Eng,* vol. 84, no. 9-10, pp. 1982-1985, 10 2007.

[14] S. P. Adhikari, M. P. Sah, H. Kim and L. O. Chua, "Three fingerprints of memristor," *IEEE Transactions on Circuits and Systems-I: Regular Papers,* vol. 60, no. 11, pp. 3008-3021, 2013.

[15] J. J. Yang, D. B. Strukov and D. R. Stewart, "Memristive devices for computing," *Nat Nano,* vol. 8, no. 1, pp. 13-24, 01 2013.

[16] D. Batas and H. Fiedler, "A Memristor SPICE Implementation and a New Approach for Magnetic Flux-Controlled Memristor Modeling," *IEEE Trans. Nanotechnol.,* vol. 10, no. 2, pp. 250-255, 03 2011.

[17] L. Chua, "Memristor, Hodgkin–Huxley, and Edge of Chaos," *Nanotechnology,* vol. 24, no. 38, 02 09 2013.

[18] F. Merrikh-Bayat and S. B. Shouraki, "Memristor-based Circuits for Performing Basic Arithmetic Operations," in *World Conference on Information Technology*, 2010.

[19] M. Laiho and E. Lehtonen, "Arithmetic Operations within Memristor-Based Analog Memory," in *Cellular Nanoscale Networks and Their Applications (CNNA), 2010 12th International Workshop on*, 2010.

[20] D. Wang, Z. Hu, X. Yu and J. Yu, "A PWL Model of Memristor and Its Application Example," in *Communications, Circuits and Systems, 2009. ICCCAS 2009. International Conference on*, 2009.

[21] M. Itoh and L. O. Chua, "Memristor Oscillators," *International Journal of Bifurcation and Chaos,* vol. 18, no. 11, pp. 3183-3206, 01 11 2008.

[22] F. Nardi, S. Larentis, S. Balatti, D. C. Gilmer and D. Ielmini, "Resistive Switching by Voltage-Driven Ion Migration in Bipolar RRAM - Part I : Experiemental Study," *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2461-2467, 09 2012.

[23] S. Larentis, F. Nardi, S. Balatti, D. C. Gilmer and D. Ielmini, "Resistive Switching by Voltage-Driven Ion Migration in Bipolar RRAM-Part II: Modeling," *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2468-2475, 2012.

[24] A. D. Polyanin and A. V. Manzhirov, "Equations Solved for the Derivative. Simplest Techniques of Integration," in *Handbook of Mathematics for Engineers and Scientists*, Boca Raton, FL 33487-2742, Chapman & Hall/CRC, 2007, p. 456.

[25] P. Meuffels and R. Soni, "Fundamental Issues and Problems in the Realization of Memristors," 31 July 2012. [Online]. Available: https://arxiv.org/abs/1207.7319. [Accessed 09 2014].

[26] Y. N. Joglekar and S. J. Wolf, "The elusive memristor: properties of basic electrical circuits," *Eur J Phys*, vol. 30, no. 4, pp. 661-675, 05 05 2009.

[27] Z. Biolek, D. Biolek and V. Biolkova, "SPICE Model of Memristor with Nonlinear Dopant Drift," *Radio Eng*, vol. 18, no. 2, 2009.

[28] F. Corinto and A. Ascoli, "A Boundary Condition-Based Approach to the Modeling of Memristor Nanostructures," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 11, pp. 2713-2726, 11 2012.

[29] Z. Biolek, D. Biolek and V. Biolková, "Analytical Solution of Circuits Employing Voltage- and Current-Excited Memristors," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 59, no. 11, pp. 2619-2628, 11 2012.

[30] D. Biolek, Z. Biolek and V. Biolkova, "Differential Equations of Ideal Memristors," *Radio Engineering,* vol. 24, no. 2, pp. 369-377, 2015.

[31] F. T. Shao Tang, F. G. Marlasca, P. Levy, V. Dobrosavljević and M. Rozenberg, "Shock Waves and Commutation Speed of Memristors," *Phys. Rev. X,* vol. 6, 2016.

[32] The International System of Units (SI), 9 ed., Bureau International des Poids et Mesures.

[33] I. Abraham, "Quasi-Linear Vacancy Dynamics Modeling and Circuit Analysis of the Bipolar Memristor," *PLoS ONE 9(11),* p. 13, 29 09 2014.

[34] I. Abraham, "An Advection-Diffusion Model for the Vacancy Migration Memristor," *IEEE Access,* vol. 4, pp. 7747-7757, 16 10 2016.

[35] R. Haberman, "The Method of Characteristics for Quasilinear Partial Differential Equations," in *Applied Partial Differential Equations with Fourier Series and Boundary Value Problems,* 4 ed., Prentice and Hall, 2004, pp. 561-581.

[36] E. W. Weisstein, "Heaviside Step Function," From Mathworld-A Wolfram Mathsource, [Online]. Available: http://mathworld.wolfram.com/HeavisideStepFunction.html. [Accessed 02 12 2019].

[37] E. W. Weisstein, "Sigmoid Function," [Online]. Available: http://mathworld.wolfram.com/SigmoidFunction.html. [Accessed 4 April 2018].

[38] D. B. Strukov and R. S. Williams, "Exponential ionic drift: fast switching and low volatility of thin film memristors," *Appl Phys (A),* vol. 94, no. 3, pp. 515-519, 03 2009.

[39] N. Gergel-Hackett, J. L. Tedesco and C. A. Richter, "Memristors with flexible electronic applications," *Proceedings of the IEEE.,* vol. 100, no. 6, pp. 1971-1978, 2012.

[40] Y. Halawani, B. Mohammad, D. Homouz, M. Al-Qutayri and H. Saleh, "Embedded memory design using memristor: Retention time versus write energy," in *Electronics, Circuits, and Systems (ICECS), 2013 IEEE 20th International Conference on*, Abu Dhabi, 2013.

[41] J. Yao, Z. Sun, L. Zhong, D. Natelson and J. M. Tour, "Resistive switches and memories from silicon oxide," *Nano Letters,* vol. 10, no. 10, pp. 4105-4110, 2010.

[42] W. Lu, K.-H. Kim, T. Chang and S. Gaba, "Two-terminal resistive switches (memristors) for memory and logic applications," in *Proceedings of the 16th Asia and South Pacific Design Automation Conference,* 2011.

[43] I. Abraham, S. Ren and R. E. Siferd, "Logistic Function Based Memristor Model," *IEEE Access,* vol. 7, pp. 166451-166462, 2019.

[44] V. Saminathan and K. Paramasivam, "Missing fourth element memristor modeling with new window function derived from sigmoid logistic equation," *Int. J. Adv. Engg. Technol.*, vol. 1, no. 1, pp. 384-386, 2016.

[45] A. Ascoli, S. Slesazeck, H. Mahne, R. Tetzlaff and T. Mikolajik, "Nonlinear Dynamics of a Locally-Active Memristor," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 62, no. 4, pp. 1165-1174, 2015.

[46] B. Muthuswamy and L. Chua, "Simplest Chaotic Circuit," *Int. J. Bifurcation Chaos*, vol. 20, no. 5, pp. 1567-1580, 2010.

[47] C. Li, J. C. T. Wesley, H. C. I. Herbert and T. Lu, "A memristive chaotic oscillator with increasing amplitude and frequency," *IEEE Access,* vol. 6, p. 12945–12950, 2018.

[48] S. F. Wang, "Dynamical analysis of memristive unified chaotic system and its application in secure communication," *IEEE Access,* vol. 6, p. 66055–66061, 2018.

[49] I. Petras, "Fractional-Order Memristor-Based Chua's Circuit," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 57, no. 12, pp. 975-979, 2010.

[50] M. Shi, Y. Yu and Q. Xu, "Window function for fractional-order HP TiO2 non-linear memristor model," *IET Circuits, Devices Syst.,* vol. 12, no. 4, p. 447–452, 2018.

[51] E. Miranda, "Compact Model for the Major and Minor Hysteretic I–V Loops in Nonlinear Memristive Devices," *IEEE Trans. Nanotechnol.,* vol. 14, no. 5, pp. 787-789, 2015.

[52] E. Miranda, B. Hudec, J. Suñé and K. Fröhlich, "Model for the current– voltage characteristic of resistive switches based on recursive hysteretic operators," *IEEE Electron Device Lett.*, vol. 36, no. 9, pp. 944-946, 2015.

[53] F. Corinto and M. Forti, "Memristor Circuits: Flux—Charge Analysis Method," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 63, no. 11, pp. 1997-2009, 2016.

[54] F. Corinto and M. Forti, "Memristor Circuits: Bifurcations without Parameters," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 64, no. 6, pp. 1540-1551, 2017.

[55] S. Kvatinsky, M. Ramadan, E. G. Friedman and A. Kolodny, "VTEAM : A General Model for Voltage-Controlled Memristors," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol. 62, no. 8, pp. 786-790, 2015.

[56] S. H. Strogatz, "Logistic Map: Numerics," in *Nonlinear Dynamics and Chaos*, Perseus Books Publishing, LLC, 2000, p. 353.

[57] R. M. May, "Simple mathematical models with very complicated dynamics," *Nature*, vol. 261, pp. 459-467, 1976.

[58] R. Naous, M. Al-Shedivat and K. N. Salama, "Stochasticity Modeling in Memristors," *IEEE Trans. Nanotechnol.,* vol. 15, no. 1, pp. 15-28, 2016.

[59] M. Al-Shedivat, R. Naous, G. Cauwenberghs and K. N. Salama, "Memristors Empower Spiking Neurons With Stochasticity," *IEEE Trans. Emerg. Sel. Topics Circuits Syst.*, vol. 5, no. 2, pp. 242-253, 2015.

[60] I. Abraham and S. Ren, "Memristor based multifunction oscillator," in *MWsCAS 2019*, Dallas, TX, 2019.

[61] M. Mahvash and A. C. Parker, "A memristor SPICE model for designing memristor circuits," in *Circuits and Systems (MWSCAS), 2010 53rd IEEE International Midwest Symposium on*, 2010.

[62] R. Berdan, C. Lim, A. Khiat, C. Papavassiliou and T. Prodromakis, "A Memristor SPICE Model Accounting for Volatile Characteristics of Practical ReRAM," *IEEE Electron Device Lett.,* vol. 35, no. 1, pp. 135-137, 2014.

[63] M. A. Zidan, H. Omran, A. G. Radwan and K. N. Salama, "Memristor-based reactance-less oscillator," *Electronics Letters,* vol. 47, no. 22, pp. 1220-1221, 27 10 2011.

[64] D. Yu, H. H.-C. Iu, A. L. Fitch and Y. Liang, "A Floating Memristor Emulator Based Relaxation Oscillator," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 61, no. 10, pp. 2888-2896, 2014.

[65] R. K. Ranjan, S. Sagar, S. Roushan, B. Kumari, N. Rani and F. Khateb, "High-frequency floating memristor emulator and its experimental results," *IET Circuits, Devices and Systems,* vol. 13, no. 3, pp. 292-302, 2018.

[66] M. E. Fouda, M. A. Khatib, A. G. Mosad and A. G. Radwan, "Generalized Analysis of Symmetric and Asymmetric Memristive Two-Gate Relaxation Oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 60, no. 10, pp. 2701-2708, 2013.

[67] F. Corinto, A. Ascoli and M. Gilli, "Nonlinear Dynamics of Memristor Oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 6, pp. 1323-1336, 06 2011.

[68] A. D. Polyanin and A. V. Manzhirov, "Abel Equations of the first kind," in *Handbook of Mathematics for Engineers and Scientists*, Chapman & Hall/CRC, 2007, p. 462.

[69] R. Palmer, "DC Parameters: Input Offset Voltage (VIO)," Texas Instruments, 2001.

[70] X. Hu, M. J. Schultis, M. Kramer, A. Bagla, A. Shetty and J. S. Friedman, "Overhead Requirements for Stateful Memristor Logic," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 1, pp. 263-273, 2019.

[71] Y. Li, Z. Wang, R. Midya, Q. Xia and J. J. Yang, "Review of memristor devices in neuromorphic computing: materials sciences and device challenges," *J. Phys. D: Appl. Phys.*, vol. 51, 2018.

[72] F. Gul, "Circuit Implementation of Nano-Scale TiO2 Memristor Using Only Metal-Oxide-Semiconductor Transistors," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 643-646, 2019.

[73] L. Chua, "The Chua Lectures: Part 3; 10 Things you didn't know about memristors," Chua Memristor Center.

[74] C. Walczyk, D. Walczyk, T. Schroeder, T. Bertaud, M. Sowinska, M. Lukosius, M. Fraschke, D. Wolansky, D. Tillack, E. Miranda and C. Wenger, "Impact of Temperature on the Resistive Switching Behavior of HfO2-Based RRAM Devices," *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 3124-3131, 12 07 2011.

[75] P.-H. Hsieh, M.-L. Tang, S.-Y. Hsu, M.-H. Lin and Y.-H. Chen, "Design and Implementation of a Memristor-Based Oscillator," in *Proc. IEEE Int. Symp. Circuits Syst.*, Sapporo, Japan, 2019.

[76] Y. Hong and Y. Lian, "A Memristor-Based Continuous-Time Digital FIR Filter for Biomedical Signal Processing," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 62, no. 5, pp. 1392-1401, 2015.

[77] A. D. Polyanin and A. V. Manzhirov, "Abel Equations of the Second Kind," in *Handbook of Mathematics for Engineers and Scientists*, 2007, p. 464.

[78] E. W. Weisstein, "Lambert W-function, From MathWorld-A Wolfram Web Resource," [Online]. Available: http://mathworld.wolfram.com/LambertW-Function.html. [Accessed 27 Sep 2019].

[79] L. Chua, "If it's pinched it's a memristor," *Semiconductor Science and Technology*, vol. 10, p. 29, 2014.

[80] Y. Babacan, A. Yesil and F. Gul, "The Fabrication and MOSFET-Only Circuit Implementation of Semiconductor Memristor," *IEEE Trans. Electron Devices,* vol. 65, no. 4, pp. 1625-1632, 2018.

[81] F. Corinto and A. Ascoli, "Memristive diode bridge with LCR filter," *Electronics Letters,* vol. 48, no. 14, 2012.

[82] A. Ascoli, F. Corinto and R. Tetzlaff, "A class of versatile circuits, made up of standard electrical components, are memristors," *Int. J. Circ. Theor. Appl.,* 2015.

[83] R. Kiyama-Armendariz and I. Abraham, "Analysis of nonlinear passive pinched hysteresis generator circuits," in *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, Dallas, TX, USA, 2019.

[84] I. Abraham, "The case for rejecting the memristor as a fundamental circuit element," *Scientific Reports,* vol. 8, pp. 1-9, 2018.

[85] G. F. Oster, "A note on memristors," *IEEE Trans. Circuits Syst.*, vol. 21, no. 1, p. 152, 1974.

[86] Y.-F. Lam, "Formulation of normal form equations of nonlinear networks containing memristors and coupled elements," *IEEE Trans. Circuit Theory*, vol. 19, no. 6, pp. 585-594, 1972.

[87] S. Adee, "The Mysterious Memristor," *IEEE Spectrum,* 01 May 2008.

[88] S. Vongehr and X. Meng, "The Missing Memristor has Not been Found," Nature, 2015.

[89] D. B. Strukov, G. S. Snider, D. R. Stewart and R. S. Williams, "Memristor: The Fourth Fundamental Passive Circuit Element," in *HP TechCon 2008,* 2008.

[90] J. M. Tour and T. He, "The fourth element," *Nature: News & Views,* vol. 453, pp. 42-43, 2008.

[91] M. D. Ventra and Y. V. Pershin, "On the physical properties of memristive, memcapacitive and memductive systems," *Nanotechnology,* pp. 1-7, 2013.

[92] K. M. Sundqvist, D. K. Ferry and L. B. Kish, "Memristor Equations: Incomplete Physics and Undefined Passivity/Activity," *Fluctuation and Noise Letters,* 2017.

[93] K. M. Sundquist, D. K. Ferry and L. B. Kish, "Second Law based definition of passivity/activity of devices," *Physics Letters,* pp. 3364-3368, 2017.

[94] D. Jeltsema, "Memristors : The Rise and the Fall (?)," in *21st International Symposium on Mathematical Theory of Networks and Systems*, 2014.

[95] H. Kim, M. P. Sah, C. Yang, S. Cho and L. O. Chua, "Memristor Emulator for Memristor Circuit Applications," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 59, no. 10, pp. 2422-2431, 2012.

[96] J. Kalomiros, S. G. Stavrinides and F. Corinto, "A two-transistor non-ideal memristor emulator," in *2016 5th International Conference on Modern Circuits and Systems Technologies (MOCAST),* 2016.

[97] C. Sanchez-Lopez, J. Mendoza-Lopez, M. A. Carrasco-Aguilar and C. Muniz-Montero, "A Floating Analog Memristor Emulator Circuit," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol. 61, no. 5, pp. 309-313, 2014.

[98] "A Simple Model of Double-Loop Hysteresis Behavior in Memristive Elements," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 60, no. 8, pp. 487-491, 2013.

[99] M. E. Fouda, A. S. Elwakil and A. G. Radwan, "Pinched hysteresis with inverse-memristor frequency characteristics in some nonlinear circuit elements," *Microelectronics Journal,* vol. 46, pp. 834-838, 2015.

[100] K. M. Sundquist and L. B. Kish, "Memristors and thermal noise: Is the memristor indeed the missing passive circuit element?," in *2017 International Conference on Noise and Fluctuations (ICNF),* 2017.