Gated Hall and Field-Effect Transport Characterization of E-mode ZnO TFTs

Jason C. Anders
Wright State University

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GATED HALL AND FIELD-EFFECT TRANSPORT CHARACTERISTICS OF

E-MODE ZNO TFTS

A dissertation submitted for the partial fulfillment of the requirements for the
degree of Doctor of Philosophy

JASON C. ANDERS.
M.S., Wright State University, 2014
B.S., Tennessee Technological University, 2012

2021
Wright State University
I HEREBY RECOMMEND THAT THE DISSERTATION PREPARED UNDER MY SUPERVISION BY Jason C. Anders ENTITLED Gated Hall and Field-Effect Transport Characterization of E-mode ZnO TFTs BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Doctor of Philosophy

__________________________
Marian Kazimierczuk, Ph.D., D. Sci.
Dissertation Director

__________________________
Fred Garber, Ph.D.
Interim Chair, Department of Electrical Engineering

__________________________
Barry Milligan, Ph.D.
Vice Provost for Academic Affairs
Dean of the Graduate School

Committee on
Final Examination

__________________________
Marian Kazimierczuk, Ph.D., D. Sci.

__________________________
Michael Schuette, Ph.D.

__________________________
Yan Zhaung, Ph.D

__________________________
Saiyu Ren, Ph.D.

__________________________
Ray Siferd, Ph.D.
ABSTRACT

Anders, Jason C. Ph.D., Department of Electrical Engineering, Wright State University, 2021. Gated Hall and field-effect transport characterization of e-mode ZnO TFTs.

Amorphous and nano-crystalline metal oxide semiconductors are an important class of materials under continuing investigation for emerging technologies. Accurate measurements of electron mobility in these materials is critical for furthering overall device development. This is complicated due to the fact that device measurements such as current response, transistor input and output characteristics, as well as mobility are affected by transport-limiting factors, such as charge trapping effects at the dielectric / active layer interface, and restriction of electronic transport across grain boundaries.

In this work, we focus on the binary metal oxide thin film transistor (ZnO TFT), a normally-off (e-mode) transistor with a positive threshold voltage ($V_{th}$) and a large ($>10$ MΩ) sheet resistance at gate voltage below threshold ($V_G < V_{th}$). Field-effect and Hall (extrinsic and intrinsic mobilities) were measured on the same device at the same time (concurrent mobility measurements of our gated Hall system) at device relevant dimensions (25 nm Al₂O₃, gate dielectric, 50 nm ZnO active layer), at typical transistor gate and drain bias device operating conditions ($V_G < 10$ V and $V_D$ biased in the linear region), on the same device ($100 \times 100 \ \mu$m Van der Pauw). The large sheet resistance ($R_S$) of the material requires electrostatic doping (by gate bias) in order to modulate resistance and increase Hall test current. However, as $V_G$ interacts with $V_D$ and $V_S$, resulting vertical electric fields $E_{GS}$ and $E_{GD}$ must remain below dielectric breakdown ($E_{BD}$). The result of meeting these test requirements led to a fully automated gated Hall test system capable of making measurements and comparisons of mobility across the allowable test bias spectrum ($V_G$ and $V_D$). A design of experiment in which test wafers were compared between in situ deposition and exposure to clean room ambient air between the dielectric and active layer was used to examine interface effects. Post temperature oven annealing was used to compare differences in grain boundary effects by increasing grain size. A simple model of two transport regimes was developed (localized and non-localized transport) to fit several contradictory trends observed in the measured data sets.
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Acknowledgement

I would like to thank my family for their support of my academic journey. I appreciate their willingness to allow me such personal growth.
1 INTRODUCTION

In 2004, a research group in Japan began writing a series of papers on the development of metal-oxide thin film transistors [45, 37, 32, 25]. These papers introduced a broad audience to the electronic and material characteristics of these nano-crystalline and amorphous materials. Since that time, these transparent, wide band gap, n-type materials have been investigated for use in an array of emerging technologies [40]. ZnO-TFTs, along with indium-doped ZnO (IGZO-TFTs), have been deposited using a range of techniques; including pulsed laser deposition (PLD) [61], RF sputtering [28], and atomic layer deposition (ALD) [42, 10].

Companies that were developing technologies in the 90s for increasingly larger displays were forced to turn to alternative material design. One of the original leaders was amorphous silicon. Amorphous silicon was prepared at room temperature, over wide sheets. Dangling bonds from the process were a problem in the beginning, until it was discovered that hydrogen was effective in assisting transport. However, one trade off of this new material was its mobility, which dropped from over a thousand, to around 1 cm$^2$/Vs. Later, Hosono and his team in Japan would put forward a metallic doped zinc oxide material, indium gallium zinc oxide (IGZO), as a new generation candidate for these low temperature process, amorphous materials. Even as the large panel display technology companies began to incorporate this new material, many questions about the nature of the material arose. Could amorphous materials be described by the same set of transport equations, that came out of the physics of crystalline solids? What would be the methods of obtaining physical level material data such as Hall? We explore these questions through the body of this work.

1.1 Origin of unique transport mechanisms in metal oxide semiconductors

Thin-film transistors (TFTs) based on Zinc Oxide (ZnO) and related materials such as indium gallium zinc oxide (IGZO) have found applications in displays [31], as well as other areas requiring transparency, flexibility [32], and low-temperature fabrication of active circuitry [40]. Despite early studies published almost 20 years ago considering IGZO TFTs as a replacement for amorphous silicon TFTs in display technology [48], electronic transport properties of this family of post-transition
metal oxide semiconductors are still not well understood [56], and extraction methods are subject to controversy.

The amorphous material, indium gallium zinc oxide (IGZO) has been used in room temperature deposition of active layers in thin film transistors. Transparent electronic devices formed on flexible substrates are expected to meet emerging technological demands where silicon-based electronics cannot provide a solution [48]. It has been used as a novel material to replace amorphous silicon (a-Si) in large screen displays. This is due to IGZO’s order of magnitude higher mobility compared to that of a-Si (10 cm²V⁻¹s⁻¹ for IGZO compared to 1 cm²V⁻¹s⁻¹ for a-Si). Also, the low mobility of a-Si is due in part due to its chemical (sp3 hybridized) bonding (FIG. 1 c). Electron transport is restricted to hopping between localized tail states (does not reach the conduction band) due to the variation in bond angle alignment in these disordered films. Conduction band transport is possible in amorphous oxide semiconductors due to overlapping of ns orbitals in the distribution of metal ions through the material (FIG. 1 d).

The distribution of potentials surrounding the metal ions, in a non-uniform distribution generate a (bumpy) conduction band minimum (FIG. 4). Electron transport is defined in three primary
regions in these materials in the literature. These three primary regions consist of:

1) Forbidden region. This region consists of states within the bandgap, or bandtail region. The principle mode of transport is trap to trap.

2) Conduction band minimum. This region consists of electron transport through a distribution of potential barriers, generated from the random distribution of ions through the material. The primary means of conduction is percolation as electrons wind their way through the particular lowest energy landscape available.

3) Conduction band. This region consists of electron transport that is free-electron-like, or conduction band transport.

These materials are compared by their primary transport characteristics and band gap in FIG. 2.

1.2 Early development of metal oxide semiconductors: Hosono and large screen display technologies

In 1996 a group of scientists from the Tokyo Institute of Technology began work on electrically conducting amorphous oxides [26]. Amorphous semiconductors were classified as either tetrahedral systems, such as amorphous silicon, used in thin film transistor applications for liquid crystal dis-
plays, or chalcogenide systems. Chalcogenide glasses being a group of inorganic glassy materials containing S, Se, or Te, with electropositive elements such as As, and Sb.

Amorphous materials were made with mobilities larger than that of amorphous silicon. The working hypothesis was that TECAMs had mobilities from 5 to 12 cm$^2$/Vs, due to the large overlap between the ns orbitals which constituted the bottom of the conduction band for these n-type materials.

Possible candidates for elements for heavy metal cations were drawn from the 11th through the 15th columns of the periodic table. From this list, several were removed quickly due to prohibitive price or toxicity, silver and mercury respectively.

Three materials were investigated: a – AgSbO$_3$, a − Cd$_2$PbO$_4$, and a − Cd$_2$GeO$_4$. It was shown that the mobilities in these materials were the same in both the crystalline and amorphous states, in accordance with their working hypothesis. Early materials demonstrating the transparent conducting oxides were single crystal (indium tin oxide) annealed at high temperature [21].

Polycrystalline zinc oxide (ZnO) was a material of interest, but the mobility of around 3 cm$^2$/Vs was considered too low for development of large area electronics. The group developed a solid-phase epitaxy (R-SPE) technique to deposit single crystal InGaO$_3$(ZnO)$_5$ [49]. This superlattice structure consisted of InO$_2$ layers and GaO(ZnO)$_5$ blocks along the $\langle 0001 \rangle$ axis.

The process involved PLD deposition of ZnO at 700$^\circ$C on a (111) single crystal yttria-stabilized zirconia substrate. Though properties such as the mobility and transparency of the material were good, electron mobility was measured at around 80 cm$^2$/Vs, the process itself would not lend itself to the kind of low temperature amorphous deposition that would be necessary for large area electronics or for wide displays. An overview of the transparent conducive oxides (TCOs) at the time was given in [24]. This process was also used in the development of all oxide metal-insulator-semiconductor field effect transistors (MISFETs), with HfOx gate insulator [45]. The benefits of using this material over silicon and GaAs were: large band gap ($\approx$ 3.0 eV), and high temperature stability.

Polycrystalline IGZO was grown on single crystal substrates as a comparison to the single crystal IGZO [46]. An Arrhenius plot of the conductivity $\sigma$ for single crystal IGZO (of varying carrier concentrations) showed an optimal fit for log $\sigma$ vs $T^{3/4}$ compared to a fit with $T^{-1}$. The representation of $\sigma = \sigma_0 \exp \left( \frac{-A}{T^{1/4}} \right)$ interpreted as variable-range hopping (VRH), caused by localized states
Figure 3: Crystal and polycrystal activation energy a) and conduction band minimum comparisons b) (from [46]).
in disordered semiconductors. Here, the group suggested that another mechanism obeying the $T^{1/4}$ relation is percolation conduction with a potential barrier height described by a Gaussian distribution. They suggested that the randomness in the distribution could come from the Ga$^{3+}$ and Zn$^{2+}$ ions in the GaO(ZnO)$_5$ layer. This similar to Anderson localization in which structural disorder forms localized tail states below the conduction band edge. The conclusion was that this model did not hold because the electronic states above some threshold energy $E_{th}$ were in the degenerate delocalized state, while below the threshold, the electronic states were in analogous tail states in a percolation regime formed from the random distribution of the ions. Comparisons of crystal to polycrystal activation energy and band conduction band minimums are shown in FIG.3.

Hosono and the Tokyo group introduced amorphous IGZO to a broader audience with their 2004 Nature paper [45]. This paper presented the metal oxide metal cation orbital overlap theory of the conduction mechanism in the bottom of the conduction band for crystalline and amorphous IGZO. Also, the a-IGZO was deposited using PLD at room temperature, using a polycrystalline InGaZnO$_4$ target.

Tuning the partial oxygen pressure during deposition was important in determining the carrier concentrations and electrical conductivities. Partial oxygen pressure of $> 6$ Pa yielded carrier concentrations of $< 10^{14}$ cm$^{-3}$. A plot of oxygen pressure from 7 Pa to 0.1 Pa showed an increase of carrier concentrations from around $10^{15}$ to $10^{20}$ with an increase in measured Hall values.

Device performance was documented. $I_D$ reached 0.02 mA at 5V $V_G$. Pinch off and saturation
typical of field-effect transistors was seen. The field effect mobility was estimated at 5.6 cm$^2$/Vs. Threshold voltage $V_{th}$ was around 1.6 V. Off current at $10^{-7}$ A, with on-off ratio around $10^3$. The transistor was bent as well, in keeping with interest in transparent, conformal, large, transparent circuit technology.

A paper on the transport properties of amorphous IGZO examined the temperature dependence of the carrier concentration and the Hall Effect [59]. Carrier concentration did not change for values of $N_e > 10^{17}$. This suggested that the Fermi level had exceeded the mobility edge. However, the Hall mobility showed thermally activated behavior in the range of $10^{17} < N_e < 10^{19}$. This would suggest the presence of potential barriers. These barriers were the uneven potential surface of the bottom of the mobility edge. To adjust the Fermi level above the fluctuations in the bottom of the mobility edge created delocalized high mobility transport across the device.

1.3 Advantages of metal oxide semiconductors over existing silicon technologies

Possible advantages of amorphous oxide semiconductors in emerging technologies have been cataloged [31]:

1) Processing temperature at or near room temperature allows deposition on a broad range of existing substrates, including existing fabricated layers

2) TFT characteristics (such as high crystallization temperatures) can be changed by altering the stoichiometry of the material.

3) TFT mobilities higher (> 10 cm$^2$/Vs) than existing a-Si technology.

4) Low operation values as evidenced by small subthreshold swing ($S$) of 0.1 V/decade, along with low operation voltages of < 5 V (FIG. 5 b).

5) Compatibility with a broad range of gate insulators, such as SiO$_2$, SiN, SiON, Y$_2$O$_3$, HfO$_2$, Al$_2$O$_3$.

6) Low off current.

7) High material uniformity and surface flatness provides better overall transport across large-area mass produced films. Such as those encountered in flat screen televisions.

8) Due to the previous characteristics, ease in large scale fabrication of these devices.

Comparisons of material and deposition conditions have been given [51] in FIG. 6.
Figure 5: Transistor input and output characteristics with subthreshold swing (from [31])

Figure 6: Comparison of material and deposition conditions (from [51])

<table>
<thead>
<tr>
<th>Structure</th>
<th>Process cost</th>
<th>Process complexity</th>
<th>Process temperature (°C)</th>
<th>Large-area scalability</th>
<th>Device type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal oxide semiconductors</td>
<td>Low</td>
<td>Low</td>
<td>RT to 350</td>
<td>High</td>
<td>Mainly n-type</td>
</tr>
<tr>
<td>Amorphous silicon</td>
<td>Low</td>
<td>Low</td>
<td>150-300</td>
<td>High</td>
<td>N-type</td>
</tr>
<tr>
<td>Low-temperature poly-crystalline silicon</td>
<td>High</td>
<td>High</td>
<td>350-500</td>
<td>Low</td>
<td>N- and p-type</td>
</tr>
<tr>
<td>Organic semiconductors</td>
<td>Low</td>
<td>Low</td>
<td>RT to 250</td>
<td>High</td>
<td>Mainly p-type</td>
</tr>
</tbody>
</table>

Table 1.1: Comparison between metal oxide semiconductors and other established flexible TFT technologies [1, 9, 14, 17].
1.3.1 Large electron mobility of metal oxide semiconductors

It was long believed that transport characteristics of amorphous semiconductors would be significantly degraded, based on the comparison of mobilities of crystalline to amorphous silicon ($\mu_{\text{Si,crystalline}} \approx 1500 \text{ cm}^2/\text{Vs}$, while $\mu_{\text{Si,amorphous}} \approx 1 \text{ cm}^2/\text{Vs}$). The strained chemical bonds in the disordered silicon samples generate deep and high-density localized states below the CBM and the VBM. In fact, the CBM of metal oxide semiconductors, consist of spherical $s$ orbitals of metal cations that are much less sensitive to structural disorder than their silicon counterparts.

Definite Hall voltages and electron mobilities are observed in a-IGZO samples. Also, it has been shown that Hall mobility increases by carrier density (FIG. 4 a). This trend is opposite that shown in crystalline semiconductors.

One possible explanation of the proportionality of Hall mobility to carrier concentration comes from percolation theory. Potential barriers are present within the conduction band, along the CBM, limiting the electron mobility as electrons are forced to move through these restrictive pathways. Increasing temperature raises the energy level of the electrons within the band into regions less dominated by barriers. Increasing temperature lowers the activation energy, and increases the mobility of the electrons within the material.

1.3.2 Low operation voltage of metal oxide semiconductors

Values for mobility calculated from measured devices are smaller than the ideal case. This is in part due from losses caused by electrons becoming trapped in the subgap density of states (DOS). This reduction in field-effect mobility ($\mu_{FE}$) is given by:

$$\mu_{FE} = \mu \frac{N_{GS} - N_T}{N_{GS}}$$

(1)

where $N_T$ is the total DOS of the unoccupied subgap DOS, and $N_{GS}$ is the electron density induced by the gate voltage $V_{GS}$, where:

$$N_{GS} = C_G(V_{GS} - V_{th}).$$

(2)
Subgap density of states assist in defining the region of transistor operation from the off state to the on state. This value ($S$, the subthreshold swing) is extracted from measured current-voltage characteristics:

$$S = \frac{dV_{GS}}{d \log I_{DS}} = \ln 10 \frac{k_B T}{e} \left(1 + \frac{eD_{sg}}{C_G}ight)$$

(3)

where $D_{sg}$ is the sub gap density of states at a given Fermi level ($E_F$). Subthreshold slope in these materials can be as low as 100 mV/decade. Interestingly, the best values for $S$ has been given by Hitachi, by reducing the active layer to 6nm and the gate dielectric to 15nm. This tends to suggest an important parameter in the design of the gated Hall system, the ability to take measurements at device level thicknesses.

Values for the subthreshold swing in IGZO materials have been reported by Kamiya and Hosono [31] shown in FIG. 5. These values are compared to ZnO TFT material deposited by our group [5] are shown in FIG. 7.

In amorphous oxide semiconductors, the non-bonded metal cation electron orbitals are considered oxygen vacancies ($V_o$). These vacancies act as shallow donors along the CBM. At the same time, due
to the ionic, rather than covalent overlap, the oxygen vacancies do not act strongly as trap centers.

1.3.3 Investigating transport limits

There have been reports of amorphous and nano-crystalline TFTs with mobilities over $100 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. These reports have been considered to be unreliable. The reason for the high mobility most likely resides in unaccounted for factors in measurement. These factors include the contribution of gate leakage current to the measurement of drain current. They also include fringing effects from non-uniform test structures. Contributions also include calculation of field-effect mobility from an underestimation of the gate insulator capacitance.

In order to estimate reasonable mobility limits in these materials, analytical equations were used and the results plotted [56], using an estimated conduction band state distribution ($g_{TA}$) of:

$$g_{TA}(E) = N_{TA} \exp \left( \frac{E - E_C}{W_{TA}} \right) \tag{4}$$

where the density of states ($N_{TA}$) is given by:

$$N_{TA} = \frac{1}{2\pi^2} \left( \frac{2m_e^*}{\hbar^2} \right). \tag{5}$$

These methods were used to generate a plot of mobility versus Fermi level for several materials (FIG. 8).

Using the expression of the total number of states ($n + n_T$):

$$n + n_T = \left( \frac{C_G V_G}{q} \right)^{3/2} \tag{6}$$

where $C_G$ is the gate insulator capacitance per unit area. In the case of this estimation, values for 100 nm of SIO$_2$, and $V_G$ is the gate voltage, an estimation for mobility versus applied gate voltage was derived and plotted (FIG.9).

One of the main conclusions of this work is that the reason that a-IGZO mobilities are much higher than a-Si is due to significantly less band tail disorder in the a-IGZO devices. This conclusion matches the general description of the difference in conduction mechanisms between the two materials.
Figure 8: Mobility vs. Fermi level (from [56])

Figure 9: Mobility vs. Applied gate voltage (from [56])
presented in the original work done by Hosono. A final note on this study is that all results are for electron transport (not holes) at room temperature and are not valid otherwise.

1.4 Primary gaps the thesis addresses

Gated Hall measurements of metal oxide semiconductors have been used to investigate the role of contact resistance in Hall mobility results, apparent mobility degradation at high gate bias [65], and in collecting data for comparison to amorphous oxide semiconductor transport theories, from free electron band-like mobility, to hopping [54]. Test structures used in these studies have thick gate insulators ($d \approx 100$ nm) which can help to prevent pinhole defects from limiting dielectric breakdown field. However, thicker dielectric material increases the gate voltage swing needed to turn the device on ($V_G = 100$ V). Measurement of Hall mobility for TFTs with gate insulator scaled to circuit-relevant dimensions ($< 25$ nm for $< 10$ V gate swing) is more challenging and requires greater care to prevent excess electrical stress.

Field-effect mobility is important in characterizing electrical charges in field-effect transistors, but is valid only in the linear region of the $I_D-V_D$ plane. Hall effect mobility describes the device geometry-independent intrinsic mobility of the material, but is limited by the measurement noise floor in high resistance films, and is often only collected at a single DC operating point. We have developed a technique to measure both mobilities concurrently on the same device, at the same time, at practically relevant dimensions (thin gate dielectric, reduced gate swing), and across the safe operating area of the device or test structure. Such simultaneous, yet independent measurements can provide in-situ verification of underlying assumptions which are often, and should be, subject to scrutiny.

We have addressed this gap with the design features of our gated Hall test system, where careful control of all potentials during testing is maintained to avoid electric field breakdown of thin dielectric layers. Concurrent measurements are performed using a computer controlled switch matrix to continuously reorient the test equipment to the device under test (DUT). Test routines were written to lower device stress, manage transients, and collect error statistics. Data is collected with all values (measured, forced, and calculated), directly comparable to one another for each device operating point ($V_G; V_D$), enabling data to be represented in novel ways.
Our gated Hall system is designed to use high precision source and measurement units when taking measurements. Gate bias and device bias is supplied by a Keithley 2636B 2-channel SMU. Current is sourced by a Keithley 6220 supply. Voltage measurements are taken using a Keithley 2182A nanovoltmeter. The device under test is connected to all sources and measurement units through a Lakeshore 775 digital switch matrix, with all connections triax up to the device probes. All instruments are connected via daisy chained GPIB, and controlled by software we have written in LabVIEW. All resultant data is processed in our Python code. We have attempted to design the test sequence in as rigorous a method possible, to reduce the myriad of subtle material effects that are known, and those currently unknown.

1.5 Thesis organization

This thesis addresses three primary topics:

The first topic is the development of the gated Hall system, along with background information to understand the challenges in measuring these materials.

The second topic consists of verification of the gated Hall system. This includes comparisons of measured transport data to published results of similar material. It involves important design results such as test repeatability, close observation of detrimental conditions such as heating effects, unreal drain current values based on large gate leakage, and observation of any measurement noise floor.

The third topic involves using the results of the gated Hall system for a design of experiment. This set of experimental conditions are to be used to make direct comparisons, in as rigorous method as possible, to matching analytical theory presented in the literature.
2 LITERATURE

2.1 Current challenges in gated Hall measurements of ZnO TFTs

2.1.1 Measurement irregularities caused by non-uniform test structure

Some of the unique challenges involved in measuring low mobility films were addressed in a paper from a group in Luxembourg [64]. Using standard Hall effect measurement techniques on their Cu(In,Ga)Se$_2$ thin films, they noticed a large degree of variation in the Hall mobility. The paper addresses many topics related to non-gated Hall effect measurements. They rely on changing the stoichiometry of deposited films to effectively dope the material within test range.

The primary topic of the paper is the development of a correction scheme for a misalignment offset factor. This due in large part from measurements taken on their disordered material on a
non-uniform test structure. They faced a slight drop in potential across the Hall probes (shown in FIG. 10). They defined this factor ($\alpha$) in relation to potential by:

$$R_{c,d} = \frac{V_{c,d}}{I} = R_s (\mu B + \alpha_{c,d})$$  \hspace{1cm} (7)

The clean room photolithographic processing at the Air Force Research Laboratory produces well defined, highly symmetric devices. These resources assist in removing additional contributions to test error such as non-symmetric electronic fields, and fringing effects, during measurements.

### 2.1.2 Unrealistic device layer thickness for ZnO TFT testing

It has been considered that field-effect mobility should increase with increasing gate-induced charge carrier concentration in disordered semiconductors [65]. Two primary transport mechanisms have been identified. First, transport primarily occurs through thermally activated hopping. Carriers hop from one localized state to another. Increasing thermal energy increases the hopping rate, increasing mobility. Secondly, Increasing carrier concentration (through application of a gate bias

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Figure 11: Improvement of high electric field mobility degradation by UV treatment (from [65])
potential) raises the Fermi energy level. This effectively decreases the average barrier height seen by electrons moving through the disordered material. However, at a given high potential, a degradation in mobility has been measured. These transport mechanisms, consisting of electron hopping in the band tail below the conduction band, and free, band-like transport above the conduction band floor, in the extended states, are shown in FIG. 12.

Application of UV ozone treatment was shown to increase the mobility in the degradation region from 23 to 30 cm$^2$/Vs. The suggestion is that defect concentration is significantly reduced by the treatment.

However, gate voltage swing of 80 V is an unrealistic voltage swing for an operating transistor. Again, this is due to the necessity of testing material at large thicknesses (100s of nA) in order to avoid measurement breakdown. This is a central topic in which our gated Hall system addresses.

2.2 Dielectric / active layer interface effects

Metal oxide thin film transistors (MOTFTs) such as zinc oxide (ZnO) and indium gallium doped ZnO (IGZO) have been investigated extensively for their use in display technology [25, 48]. These
devices have been shown to have electrical instabilities based on stress from light, current, and gate voltage bias [12, 29]. These instabilities originate from two sources. In the first, oxygen vacancies near the surface of the back channel form an additional density of states (DOS) above the valence band maximum. In the second, additional states arise from the absorption and desorption of molecules on the ambient exposed active layer [66]. These two effects are shown in FIG 92. Here, under positive bias stress, oxygen atoms are drawn from exposure to ambient conditions, to the dielectric semiconductor interface. At the same time water molecules are driven out of the material. Passivation by deposition of a thin organic film over the exposed active layer has been investigated [41, 33, 44, 63].

Metal oxide semiconductors are a favorable material for meter long scaling of the substrate. This is due to their ability to be deposited at room temperature by RF/DC sputtering. At the same time, operation of these devices suffers from several environmental effects [31]. They are sensitive to the atmosphere. This includes exposure to oxygen, moisture, and hydrogen. Post process annealing generates oxygen deficiencies that act as shallow donors, generating mobile electrons. The changing landscape of adsorption and desorption of oxygen, moisture, hydrogen, and oxygen vacancies generate unwanted instability in the output of the device.

Figure 13: Positive Gate Bias electrical instability (from [12]).
Figure 14: Comparisons of $\Delta V_{\text{th}}$ under PBS (from [33])
2.2.1 Positive bias stress

Results from positive and negative bias stress (PBS) on IGZO have been presented [12]. Measured transfer characteristics from continuous application of gate voltage for $1 \times 10^4$ s show a positive shift in $V_{th}$ (FIG. 13). Also shown is that the sub-threshold swing (SS) is relatively unaffected. The field-effect mobility calculated from the given transfer curves remains relatively constant for PBS, while $\Delta V_{th}$. Charges ($Q_{it}$) accumulate at the dielectric semiconductor interface under gate bias. The $\Delta V_{th}$ shift is due to negative charge screening of $V_G$ during PBS testing.

2.2.2 Device encapsulation

Results from encapsulation of IGZO in the polymer parylene has been presented [33]. Comparisons of $\Delta V_{th}$ between ambient exposed devices, and those covered in Parylene, show better stability for passivated devices (FIG. 14). Conclusions drawn from this paper suggest that positive $\Delta V_{th}$ shift with unchanged values for the sub-threshold swing under PBS is explained by a charge trapping mechanism modelled by a stretched exponential time dependent model commonly used to describe charge screening:

$$\Delta V_{th} = V_0 \left(1 - \exp \left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right)$$

(8)

where $V_0 = |V_{th}|$ at infinite time, $t$ is the stress time, $\beta$ is a dispersion parameter, and $\tau$ is a characteristic time that measures how fast the threshold voltage moves with time.

2.2.3 Negative bias stress

The term negative bias stress is usually associated with negative bias illumination stress (NBIS). This refers to electronic instabilities that occur under exposure to light. A group has investigated negative bias stress (without additional light stress) [12]. While the field-effect mobility remained unchanged under PBS, it was shown to increase from around 4 cm$^2$/Vs to around 8 cm$^2$/Vs as shown in FIG. 15.

One possible simple explanation of the change in mobility due to NBS is that this type of stress is removing the accumulated interface charge ($Q_{it}$) at the dielectric semiconductor interface. The
Figure 15: Change in mobility by positive and negative voltage stress (from [12])

opposite of the charge screening effects of PBS with an associated shift of $\Delta V_{th}$ toward more negative voltage values.

Band bending in the MOS structure (FIG. 16) has been suggested as a possible reason behind the rise of $\mu_{FE}$ from NBS [Xiao2013]. Donor-like states below the Fermi level are neutral. Donor-like states above the Fermi level are positively charged. Before NBS is applied, the Fermi level is above the neutral donor states at the dielectric semiconductor interface. When negative gate voltage is applied, the donor energy states rise, resulting in electron de-trapping. The electrons

Figure 16: Band bending in IGZO TFT (from [12])
enter the channel and the donor states become positively charged. The positive charge then screens the applied gate voltage, generating the $\Delta V_{th}$ shift in the negative direction.

2.3 Grain boundary effects

2.3.1 Modeling of grain boundary barrier modulation in ZnO

Experimental results from this paper showed a non-linear increase of drain current and gradual enhancement of field effect mobility with increasing gate bias [27]. A single grain boundary was modelled as:

$$N_{\text{gras}}(E) = N_{tg}\exp\left[-\left(\frac{(E_{t1} - E)}{(E_{t2})}\right)^2\right]$$

where $N_{\text{gras}}(E)$ and $E$ are the density of defect states and corresponding trap energy inside the band gap. $N_{tg}$, $E_t$, and $E_2$ are the total density of trap states, peak energy, and characteristic decay energy. The grain boundary profile around the grain boundary forms a double Schottky barrier. A 3D band bending profile was developed demonstrating the modulation of transport through grain boundary barriers by three applied gate bias voltages (FIG. 17-19).

2.3.2 Nano column structure of PLD ZnO TFTs

Columns of nano crystalline ZnO form closely packed arrangements in self-aligned nano crystalline ZnO thin films, so that boundaries between nano columns are parallel to each other and perpendicular to the growth surface (FIG. 20). By this structure electrical current flows from source to drain across the boundaries. Due to this arrangement grain boundary effects are summed across the channel in this material [6].

Nano column grain diameters were shown to vary both by deposition and post deposition conditions such as post deposition annealing. Increase in post deposition annealing temperature was shown to increase grain size. X-ray diffraction (XRD) of these ZnO thin films showed (FIG. 21) a hexagonal wurtzite structure with preferred [002] orientation.
Figure 17: Gate bias modulated grain boundary effects $V_g = 0V$ (from [27]).

Figure 18: Gate bias modulated grain boundary effects $V_g = 5V$ (from [27]).
Figure 19: Gate bias modulated grain boundary effects $V_G = 10\, \text{V}$ (from [27]).

Figure 20: Nano column structure of PLD deposited ZnO (from [6]).
3 THEORETICAL

3.1 Mobility

3.1.1 Extrinsic mobility: field-effect mobility

A metal oxide semiconductor (MOS), or surface field-effect transistor, modulates current across the source and drain contacts, by opening and closing an inversion region (channel) between the contacts in the semiconductor region near the metal gate.

A differential slice of the drain current ($I_D$) flowing through the channel (in the x direction) is given by [18]:

$$I_D \, dx = \mu_n W |Q_n(x)| \, dV_x$$  \hspace{1cm} (10)

where $\mu_n$ is the surface mobility, $W$ is the channel width, and $Q_n$ is the mobile charge.
Integration of all the small differential slices between the source and drain leads to an expression of the full drain current ($I_D$):

$$I_D = k_N \left[ (V_G - V_{th}) V_D - \frac{1}{2} V_D^2 \right] \quad (11)$$

where:

$$k_N = \frac{\mu_n W C_{ox}}{L} \quad (12)$$

where $V_G$ is the applied gate bias, and $V_{th}$ is the threshold voltage for on characteristics of an n-type device, $C_{ox}$ is the oxide capacitance of the dielectric layer, and $L$ is the gate length. The value for oxide capacitance is given by:

$$C_{ox} = \frac{\varepsilon_r \varepsilon_0 A}{d} \quad (13)$$

where $\varepsilon_r$ is the relative permittivity of the Al$_2$O$_3$ gate dielectric, $\varepsilon_0$ is the permittivity of free space, $A$ is the capacitive area of the gate dielectric, and $d$ is the dielectric thickness (25 nm in our ALD films).

The value $k_N$ is a parameter that determines the conductance and transconductance of the n-channel MOSFET.

The value for the device conductance ($g$) in the linear device bias range ($V_D < (V_G - V_{th})$), with the device in the on state ($V_G > V_{th}$), and experimentally referred to as transistor input characteristics, is given by [31]:

$$g = \frac{\partial I_D}{\partial V_D} = \frac{W}{L} C_{ox} (V_G - V_{th}). \quad (14)$$

The transistor output characteristics, the relation between drain current and gate voltage (IV characteristics) is used to determine the transconductance ($g_m$) of the device. The transconductance (in the linear operating region, $g_{m,lin}$) is given by:

$$g_{m,lin} = \frac{\partial I_D}{\partial V_G}. \quad (15)$$
The field-effect mobility ($\mu_{FE}$) is derived from these relations:

$$\mu_{FE,\text{lin}} = \frac{Lg_m}{W C_{ox} V_D} (\text{cm}^2/\text{Vs}).$$ \hspace{1cm} (16)

All of our current Hall mobility testing occurs within our region of interest. This region restricts all measurements to the linear operating range. For completeness, the expression for field-effect mobility in the saturation operation range ($\mu_{FE,\text{sat}}$) is given:

$$\mu_{FE,\text{sat}} = \frac{2L}{W C_{ox}} \left( \frac{\partial \sqrt{I_D}}{\partial V_G} \right)^2.$$ \hspace{1cm} (17)

### 3.1.2 Intrinsinc mobility: Hall effect mobility

In 1879 Edwin Hall brought forward a series of relations describing an electric current flowing through a transverse magnetic field. The Hall mobility is measured using a square test structure called a Van der Pauw structure (FIG. 34). Current is forced across the diagonals of the device. This forced measurement current $j_x$ is generated by the external electric field $E_x$ applied by the current source. The average rate of motion of free electrons through $E_x$ is defined as the drift velocity ($v_x$). In a steady state electric field [34]:

$$v_x = -\frac{e\tau}{m} E_x$$ \hspace{1cm} (18)

where $e$ is the electron charge, $m$ is the electron mass, $\tau$ is the electron mean free path, and $E_x$ is the electric field.

When a current along this path $j_x$ encounters a transverse magnetic field, $B_z$, the electrons are subject to the Lorentz force. The Lorentz force acts in the direction of the mathematical cross product of the current and magnetic field. The sum of the forces acting on the electrons from both the electric and magnetic fields (expressed by the vector $\mathbf{F}$)is given by:

$$\mathbf{F} = -e \left( \mathbf{E} + \frac{1}{c} \mathbf{v} \times \mathbf{B} \right)$$ \hspace{1cm} (19)

The Lorentz force pushes electrons to one side of the device. This buildup of electrons on one
side develops a potential across the opposite diagonal contacts from which the measurement current is forced. The resulting electric field is given (in the preceding reference frame) by:

\[ E_y = -\frac{eB_z \tau}{mc} E_x \]  

(20)

where \( c \) is the speed of light.

This voltage, the Hall voltage (\( V_{Hall} \)) is often expressed as:

\[ V_{Hall} = \frac{R_H IB}{d} \]  

(21)

where \( R_H \) is the Hall coefficient, \( I \) is the forced test current, \( B \) is the supplied external transverse magnetic field, and \( d \) is the sample thickness.

Turning back to the original notation, \( R_H \) is expressed by:

\[ R_H = \frac{E_y}{j_x B_z} \]  

(22)

It is also given by:

\[ R_H = \pm \frac{r}{qn} \]  

(23)

where \( r \) is the Hall scattering factor. This scattering factor varies according to the influence of scattering rates in the material. In our work we use the convention of setting \( r = 1 \), which is the condition of a degenerate semiconductor. Through out the Hall calculations, values for \( d \) cancel out.

We define carrier concentration (\( n \)) and resistance as sheet carrier concentration and resistance. Final values for mobility are considered sheet quantities as well.

Further insight into the physical properties embedded into \( R_{Hall} \) can be gained by expanding out the \( j_x \) term. The electric current density can be expressed as:

\[ j_x = ne^2 \tau E_x / m. \]  

(24)

where \( n \) is the number of electrons in the current flow. The expression for electrical conductivity
(\sigma) is given by:

\[ \sigma = \frac{ne^2\tau}{m} \]  

(25)

In this manner, Ohm’s law is expressed:

\[ j = \sigma E \]  

(26)

The Hall coefficient, generated from known forced measurement current \( (j_x) \), value in Teslas of the external magnetic field \( (B_z) \), and the directly measured Hall voltage \( (V_{Hall,y}) \) can be used to solve for the carrier concentration \( (n) \):

\[ R_H = -\frac{eB_z\tau E_x/mc}{ne^2\tau E_x B_z/m} = -\frac{1}{ne} \]  

(27)

For non-symmetric test structure geometries (or to test variation across measurement positions) current and magnetic field reversal and averaging can be an effective method of determining more accurate results. Current reversal averaging is given by:

\[ V_{Hall,ave} = \frac{1}{2} \text{abs} \left| V_{1,\text{meas},(+I)} = V_{1,\text{meas},(-I)} \right|. \]  

(28)

Field reversal averaging is given by:

\[ V_{Hall} = \frac{1}{2} \text{abs} \left| V_{\text{Hall,ave}(+B)} - V_{\text{Hall,ave}(-B)} \right| \]  

(29)

Measured Hall voltage, leading to calculation of the Hall coefficient, is one half of the information needed to calculate Hall mobility. The other half is measuring sheet resistance. Sheet resistance \( (\rho_S) \) can be measured along two separate sets of contact positions \( (R_1 \text{ and } R_2) \):

\[ \exp \left( -\frac{\pi R_1}{\rho_S} \right) + \exp \left( -\frac{\pi R_2}{\rho_S} \right) = 1 \]  

(30)

or solved with a numerical factor \( f \):
\[ \rho_S = \frac{\pi}{\ln 2} \frac{R_1 - R_2}{2} f. \]  

(31)

Having determined the values for the Hall coefficient \( R_H \) and the sheet resistance \( \rho_S \), the Hall mobility \( \mu_{Hall} \) can be calculated:

\[ \mu_{Hall} = \frac{R_H}{\rho_S} \]  

(32)

3.1.3 Increase of ZnO TFT mobility by sheet carrier concentration

The relationship of Hall mobility increasing by sheet carrier concentration in IGZO TFTs [59], and the \( N_s \) dependence of \( \mu_{Hall} \) has also been observed in our material (FIG. 82). Here the results for both \( \mu_{FE} \) and \( \mu_{Hall} \) for all values across the safe operating area are displayed. The graph shows outliers at low \( N_s \) and low mobility correspond for test conditions of \( (V_G < 4 \text{ V}) \), the Hall measurement noise floor.

3.2 Conduction limiting effects

3.2.1 Disorder in material

In Anderson localization, electrons propagate cohesively with minimal obstructions through an ideal crystalline material. The distance the electron wave function remains coherent is defined as the mean free path \( (l) \). Impurities, vacancies, and crystal dislocations are all considered defects in a crystal. These defects create local scattering sites for the electron wave function. In an amorphous material there are localized areas where the bond length, bond angle, and coordination may change. When an electron travels through the amorphous material at high energy or temperature, it moves through band-like regions with a maximum mean free path. When these electron wave functions encounter disorder in the structure, the disorder acts as scattering sites. The result is a reduction in the mean free path of electrons in the local disordered regions [38]:
where \( l \) is the mean free path, and \( a \) is the lattice length.

A term that describes the energy level for an electron in a single well, in a crystal lattice. When potentials become non-uniform, an extra term for potential \( (U) \) is added to the quantum well potential, \( W_0 + 1/2U \). The total number of arrangements of potentials is described as a statistical ensemble, \( \langle U^2 \rangle = U_0^2 \), where \( U_0 \) is an expectation value. \( U_0 \) represents the degree of disorder of the overall potential distribution.

The fixed lattice parameter \( a \) is related to the electron mean free path \( L \):

\[
a/L = (U_0/I)^2/16\pi
\]

where \( I \) is the overlap integral, \( I = e^{-\alpha R I_0} \).

Values of \( L \) close to \( a \) produce non-localized states, while values of \( L < a \) produce localized states. If there is no overlap of wave functions in the localized states, their only means of movement is from hopping from state to state. If the states are far apart from one another then the hopping probability is decreased. These concepts are demonstrated [38] in FIG. 22.

The Anderson density of states model describes a critical energy \( (E_C) \) that separates the extended and localized states (band tail). The relation of the energy of the system \( (E) \) to the critical energy
(E_C) involves the DC conductivity of the system \( \langle \sigma_E(0) \rangle \) at temperature \( T = 0K \):

\[
\langle \sigma_E(0) \rangle = \begin{cases} 
0 & \text{for } E < E_C, \\
\neq 0 & \text{for } E > E_C.
\end{cases}
\] (35)

Wave functions in the extended states \( E > E_C \) are thought of as extending through the lattice. The density of states at the band tail is lower than that through the central part of the band. The states with the same energy are dispersed randomly through the material. With a large separation of localized electrons in the band tail, the probability of tunnelling is small.

Mott presented three primary theoretical concepts describing the electrical properties of amorphous semiconductors:

1). The density of states is a valid concept for both crystalline and amorphous semiconductors. The primary factors are atomic coordination number and interatomic distance. If these two parameters are similar between an amorphous and crystalline phase of a material, then their density of states will be similar.

2). The wave number \( k \) is not a good quantum number in amorphous materials.

3). In amorphous semiconductors, localized states exist in the bandgap. \( E_C \) describes the separation of the localized and extended states.

The Kubo-Greenwood formula is a tight-binding approximation for electron wave functions [11]:

\[
\sigma_E(0) = \frac{2\pi e^2 h V}{3m^*} \langle |k'|p|k|^2 \rangle N(E)^2
\] (36)

where \( \sigma_E(0) \) is the DC electrical conductivity, \( V \) and \( N(E) \) are the sample volume and density of states, and the expression in bracket, presented in Dirac notation, describes the current, averaged quantum mechanical state of the system. In this notation \( |k> \) represents a plane wave (a description of an electron wave). A plane wave is represented by \( e^{i(kr)} \). This expression is valid for a wave functions in a crystal lattice satisfying proper boundary conditions. These conditions are infinite periodicity (perfect crystal structure). Here, the wave functions is represented by the Wannier function, \( e^{ikR_n} \), where \( R_n \) is the position of the \( n^{th} \) atom.

One feature of Wannier functions \( \theta(R) \) is that they are localized around the point \( R \) and fall
off rapidly away from $R$. The expression for DC conductivity can be arranged:

$$\sigma_E(0) = \frac{2\pi e^2 \hbar^3 a \lambda^2}{3m^2} N(E)^2$$

where $\lambda \approx 1$. The density of states changes by the variation in local potential ($V_0$) as:

$$N(E) = \frac{1}{a^3 V_0}.$$  

(38)

The Drude formula uses the Boltzmann conductivity $\sigma_B$ [14]:

$$\sigma_B = \frac{ne^2 \tau}{m}$$

(39)

where $n$ is the electron density, $\tau$ is the relaxation time, and $m$ is the electron mass. The description of transport given by the Drude model and Boltzmann conduction breaks down near the mobility edge in amorphous materials, due to electron scattering. Using an additional scattering probability state $e^{i(k_F)^R}$ and a wave functions superposition expression for the wave functions at Fermi energy level, $|k_F>$, along with the scattered wave functions, $a_0|k_F> + \Sigma a(q)|k_F + q>$, and expression for conduction at the mobility edge can be derived:

$$\sigma = \sigma_B \left[ 1 - \frac{1}{(k_F l)^2} \right]$$

(40)

where $l$ is the electron mean free path, and the expression for the conduction floor by the Ioffe-Regel rule is $\sigma = 0$ when $k_F l = 1$.

In the effective medium approximation, the effective longitudinal drift conductivity $\sigma_e$ in a disordered system under a weak external electric field, $E = E, 0, 0$ can be calculated by the effective medium approximation (EMA) [57]:

$$\left\langle \frac{\sigma(\epsilon_m) - \sigma_e}{\sigma(\epsilon_m) + (d-1)\sigma_e} \right\rangle = 0$$

(41)

where $\sigma(\epsilon_m)$ is the local conductivity at the band edge, and $d$ is the spatial dimension. The charge-carrier contribution from the extended states are greater than that of the hopping charge mobility.
from the localized states. Neglecting the contribution from localized states, the concentration of the mobile charge carriers is given by:

\[ n(\epsilon_m) = D_{C0} \int_{\epsilon_m}^{\inf} \sqrt{\epsilon - \epsilon_m + \left( \frac{N_m}{D_{C0}} \right)^2} \frac{1}{1 + \exp \left( \frac{\epsilon - \epsilon_F}{k_B T} \right)^2} \]  

(42)

The drift conductivity is given by:

\[ \sigma(\epsilon_m) = e\mu_0 n(\epsilon_m) \]  

(43)

with an intrinsic, band-like drift charge carrier mobility of:

\[ \mu_0 = \frac{e}{m^*} \langle \tau \rangle \]  

(44)

where \( e \) is the elementary electron charge, \( m^* \) is the effective mass, and \( \langle \tau \rangle \) is the average scattering time.

Part of the work from the Japanese group including Hosono and Nomura involved ab initio calculations [47]. Ab initio calculations begin with a simple unit cell of IGZO. This unit cell is replicated into a molecular dynamics MD supercell of 1890 atoms. The MD method simplifies interatomic forces between atoms, allowing computer simulated temperature to rise to 5500 K, then cooled to 1 K at a rate of 12.5 K / s. This method, known as thermal melt and quench, is commonly used to reproduce amorphous molecules.

Once the large molecule is frozen in place from the computationally cheap MD process, it is reduced to 84 atoms for the computationally expensive ab initio quantum mechanics simulations. Each atom in this process is modelled by a local-density approximation (LDA) code. As computationally intensive as these models are, they are a tremendous side step, solving for a quantum mechanical bottom-up approach for molecule sized arrangements without solving the untenable multi body Schrödinger wave functions. The primary benefit to this process is that descriptions of fundamental characteristics of molecules can be described, such as arrangement of bond angles, electronic density distributions in three dimensions, and band structure.

An interesting observation from these simulations answers the question, how disordered are these
amorphous materials. Disorder is not expressed as a fully chaotic arrangement. Part of the statistics from the software lists the overall bond length by coordination number. Where the coordination number represents adjacent atoms through the molecule. That is, for a highly random arrangement of atoms, overall bond angle variation would be thought to be large. In fact, overall variation of adjacent bond length is not large. This is due to the fact that even though the material has been heated to 1000's of degrees Kelvin, the interatomic (Lennard-Jones) potentials are greater. The variation of bond length to coordination number for Indium atoms in the amorphous structure are shown in FIG. 23. This demonstrates that even in amorphous material, inter atomic variation can be close to their crystalline counterparts.

### 3.2.2 Percolation conduction in the conduction band

Measured mobility typically falls off at increasing sheet carrier density for crystalline, covalent bonded, semiconductors due to an increase of scattering effects as the total number of electrons moving through the material becomes large.

The conduction band minimum of metal oxide semiconductors has been modelled [31] by a
bumpy, uneven, potential surface FIG. 4, with an observed relation between mobility and sheet carrier concentration opposite to that of crystalline films. The reason given for this behavior involves the available lowest energy pathways of mobile electrons moving through the landscape of potential barriers. At the lowest supplied energy to electrons (moving laterally across the potential landscape under the influence of an external electric field, the device bias) move from valley to valley across the potential landscape. When additional energy is supplied to the electrons (thermal, or in our case, adjustments to energy made by electrostatic doping from gate contacts) electron pathways become available above the lowest regions of the potential landscape. These percolation pathways include pathways that are less restrictive than the lowest energy routes. This causes an overall decrease in the total distance that mobile electrons travel across the device. As the device is further biased, the reduction of the overall percolation pathway distance is reflected in a measured increase in mobility under increasing gate modulation, even as the sheet carrier concentration continues to rise.

3.2.3 Grain boundary effects

Grain boundary and inter grain scattering effects in polycrystalline semiconductors restrict mobility [55]. Though field emission and thermionic field emission contribute to mobility reducing effects, the primary mechanism is thermionic emission (FIG. 24). This figure shows two routes for electrons: one, passing over the potential barrier by thermionic emission, and two, thermally activated tunneling at $E_m$ and tunneling at the Fermi level.

Polycrystalline (and nano crystalline) materials consist of small crystalline grains separated from one another by grain boundaries. This large amount of disordered region in the material can trap electrons. Trapping can involve the development of potential barriers at grain interfaces acting as scattering sites for mobile electrons. The height of the potential barriers can be understood in terms of the grain boundary height ($E_B$), doping concentration ($n_D$), along with the lateral grain size ($L$) [55]:

$$E_B = \frac{\varepsilon^2 L^2}{8 \varepsilon_0 \varepsilon_r} n_D + E_C,$$

(45)

for $LN_D < Q_t$. Here, the product of the grain size and the doping concentration are less than the
Figure 24: Individual grain boundary effects (from [55]), where \( E_C \) and \( E_F \) designate the energy level of the conduction band and the Fermi level. \( E_B \) is the barrier height.

The density of occupied traps per area at the grain boundaries (\( \varepsilon_0 \) and \( \varepsilon_r \) are the vacuum permittivity and the dielectric constant). Traps are only partially filled and grains are completely depleted of electrons. For the opposite trend, \( Ln_D > Q_t \), traps are completely filled with electrons and the grains are partially depleted:

\[
E_B = \frac{\varepsilon^2 Q_t^2}{8\varepsilon_0 \varepsilon_r n_D} + E_C
\]  

(46)

### 3.2.4 The dielectric / active layer interface

Interface trap density calculated from the subthreshold swing.

### 3.2.5 Discrete trap model

The discrete trap model is used to simplify mathematical analysis and to provide insight into traps on TFT performance [23]. The rate of conduction band trapping is a function of the empty trap density \( (N_T) \) and the density of electrons present in the conduction band. While the rate of emission from the trap states to the conduction band is a function of the filled trap density and the conduction band...
electron density when the Fermi level ($E_F$) is equal to the ionization energy ($E_T$). The conduction band electron density ($n_1$) is given by:

$$n_1 = N_C e^{(E_F/k_BT)}$$  \hspace{1cm} (47)

where $N_C$ is the effective density of states of the conduction band and $k_B$ is Boltzmann’s constant.

When considering charge effects in TFTs ($Q = C \times V$), total charge in the channel upon application of gate voltage is distributed through both conduction band and trap states:

$$q(\Delta n_C + \Delta n_t) = q[(n_c + n_t) - (n_{c0} + n_{t0})] = \frac{C_G}{\hbar} [V_{GS} - V(y)]$$  \hspace{1cm} (48)

where $n_{c0}$ and $n_{t0}$ are initial, zero-bias densities of free conduction band electrons and trapped electrons. The degree to which these trap states affect threshold voltage ($V_{th}$) expressed as the ON voltage ($V_{ON}$) is given by:

$$V_{ON} = -\frac{qh}{C_G}(n_{c0} + n_{t0})$$  \hspace{1cm} (49)

## 4 METHODOLOGY

The primary goal of developing the gated Hall system was to find a way to measure disordered metal oxide semiconducting material. Meeting this goal required carefully managing device potentials during measurement. This goal was expanded into developing automated testing across the allowable bias landscape. It also included both field-effect and Hall mobility, at the same time, and on the same device, across all allowable bias conditions as well.

### 4.1 TFT device fabrication

#### 4.1.1 Pulsed laser deposition of zinc oxide

Zinc oxide was deposited using a pulsed laser deposition process. Pulsed laser deposition is a versatile technique in which an incident laser beam generates energy. This energy is passed through a window into a high vacuum deposition chamber. Nano second laser pulses, trained on a disc of wafer material,
ablate material in stoichiometric proportions, onto a prepared substrate. This process is shown in FIG. 25. PLD techniques allow a wide range of deposition temperatures, and in situ gasses during thin film deposition [36]. Our films were deposited by a Neocera Pioneer 180 pulsed laser deposition system with a KrF excimer laser (Lambda Physik COMPex Pro 110, \( \lambda = 248 \text{ nm} \), pulse duration of 10 ns) with a base chamber pressure of \( 4 \times 10^{-8} \text{ Torr} \). The laser energy density was 2.6J/cm\(^2\). The repetition rate was 30 Hz. The deposition temperature was 350-415 °C. The wafer was rotated at a constant speed of 20 °/sec and the target was rotated at a constant speed of 40 °/sec. The deposition rate was 0.3 nm/sec. The target was a 50 mm diameter by 6 mm thick sintered ZnO ceramic disc (99.999%) [5]. After deposition, the wafers were placed in a 400 °C ceramic oven in clean room ambient air for 1 hour.

4.1.2 Atomic layer deposition of zinc oxide

ALD meets the needs for atomic level control as well as conformal deposition through self limiting surface reactions [17]. This process is shown in FIG. 26. This process has been used to deposit continuous pin hole free films in thin film dielectrics with low leakage current in the nanoamps.

Atomic layer deposition of ZnO films were prepared in a Cambridge Nanotech Fiji F200 ALD system at 250° C. ZnO depositions used diethyl-zinc and water as the zinc and oxygen source, respectively, yielding a growth rate of 1 Å/cycle. Argon was used as a precursor carrier gas and
purge gas [6].

4.1.3 Photolithographic process

A two-step clean room photolithographic process was designed to provide high quality Van der Pauw test structures for use in gated Hall testing. Two sets of chrome on glass photomasks were designed using AWR software. The first mask involves patterning for a subtractive process in which the dielectric and active layers were separated from one another between areas of bare silicon substrate. The second mask involved in creating openings in resist on top of the mesas in which to evaporate Ti/Pt/Au metal contacts.

The prepared wafer before photolithography is shown in FIG. 27. In the first processing step, 1813 photoresist was spun on to the deposited 3 inch, oven annealed, zinc oxide wafers. The resist was baked 100 °C. The wafer was then placed in a MA6 mask aligner and exposed at 10 mW/cm² for 5 seconds, using the mesa process mask. The wafer was then developed using 300 MIF in order to expose areas of active layer/dielectric to be removed. The wafer was then placed in an ICP-RIE etch chamber to remove the unprotected regions. This was followed by an acetone resist lift off process, completing the mesa step. This processing step is shown in FIG. 28.

Deposition of the ohmic contact began with spun on LOL 2000 and SPR resist baked at 100 °C. The wafers were then exposed on the contact aligner for 5 seconds. The patterned resist was
Figure 27: Wafer prepared for photolithographic processing

Figure 28: Photolithography: mesa process
developed using 300 MIF. The open regions of resist were then exposed to metal evaporation of 200 angstroms of titanium, 300 angstroms of platinum, and 3500 angstroms of gold. This was followed by a spray liftoff process for the remaining photoresist and oxygen plasma exposure to assist in surface cleaning. This processing step is shown in FIG. 29.

The final, working transistor is shown in FIG. 30.

4.1.4 Test structure design

A number of test structures were designed for use in the gated Hall system. This wafer was designed in order to ease testing across multiple test benches, and especially to provide a photolithographically
well defined Van der Pauw test structure for gated Hall. The full test die is shown in FIG. 31. A photograph of the complete, finished wafer with all devices is shown in FIG. 32.

The Van der Pauw (VDP) test structure (FIG. 33) consists of a $100 \times 100\mu m$ square section, with ohmic contacts tracing from large contact pads, to sharp points at the corners. The well defined VDP device structure removes possible additional sources of fluctuation in electrical measurements. This is important in Hall measurements of high resistance oxide materials, in which the Hall voltage becomes vanishingly small under low bias conditions.

A scanning electron microscope (SEM) top down image of our VDP structure is shown in FIG. 34. An oblique SEM image with laser cut trench shows device layering in FIG. 35.

The two finger FET test structure (FIG. 36) doubles total transistor width, increasing output current characteristics. It can be used to generate field-effect mobility calculations, as well as transistor input and output characteristics.

The transmission line test structures (FIG. 37) are useful in obtaining data plots of contact resistance. They also offer a simple set of structures to test transistor properties.

The capacitor test structures (FIG. 38) are useful not only in measuring capacitance, but also provide large area pads in which to measure other types of electrical properties by DLTS.
Figure 32: Photograph of completed wafer with all devices

Figure 33: Gated Hall Van Der Pauw die
Figure 34: Top down SEM image of our VDP structure

Figure 35: Oblique SEM image of our VDP structure
Figure 36: Gated Hall two finger die

Figure 37: Gated Hall TLM
4.2 Hall mobility test requirements of zinc oxide TFTs

4.2.1 Addressing the primary problem: understanding the vertical electric field

Each test structure is isolated from its neighbor through a mesa process (isolated vertical stacks). Potentials between the drain and the gate are shown. As the device turns on ($V_G > V_{th}, V_{DS} > 0$), two transverse potentials are formed across the gate dielectric: $V_{GD}$ and $V_{GS}$. These potentials acting over the thickness ($d = 25 \text{ nm}$) of the dielectric layer generate two vertical electric fields: $E_{GD} = V_{GD}/d$ and $E_{GS} = V_{GS}/d$. The field induced dielectric breakdown is the primary limiting factor of testing. A non destructive test requires $E_{max} < E_{BD}$, informing $V_{max}$ for both $V_{GD}$ and $V_{GS}$.

The vertical electric field across the gate dielectric (25 nm) at a drain bias of $V_D = 0.3 \text{ V}$, and
a gate bias of $V_G = 9$ V becomes $E_{GS} = 3.6$ MV/cm and $E_{GD} = 3.48$ MV/cm. Similar values for the maximum field, $E_{BD,Al_2O_3}$ have been reported [20]. Since the source side of the drain voltage ($V_{DS}$) is connected to ground ($V_S = 0$ V), $V_{GS} = V_G$. Positive drain bias cannot reduce the potential, or resulting electric field, across the gate dielectric. For this reason, $V_{GS}$ limits the allowable gate voltage that can be applied during testing. The electric field across the gate dielectric can be compared to the lateral electric field between contacts. At $V_D = 0.3$ V, and a Van der Pauw (VDP) distance between contacts of 100 µm, the lateral electric field across the device is $E = 0.00003$ MV/cm.

These calculations show that the electric field across the gate dielectric is much larger than the electric field across source and drain contacts ($E_{GS} >> E_{DS}$) during measurement. These values satisfy a requirement for the gradual channel approximation (GCA) for power law approximation of the field-effect mobility [22, 23] used in EQ. (57). Calculation of field-effect mobility from measured device transfer curve characteristics contains many hidden contributions that are not explicitly expressed in the final value for mobility. For instance, it is not known precisely how electrons move through the channel of the TFT device [60, 16].

### 4.3 Components of the gated Hall system

The fabrication process follows that described in [2], although material repeatability may be responsible for the relatively lower material values reported here. Floating-gate sheet resistance is in the hundreds of MΩ range, so electrostatic doping (gating) is needed to obtain Hall transport parameters of practical use.

#### 4.3.1 Physical layer: GPIB connections

Our gated Hall system (FIG. 40 is designed to use high precision source and measurement units when taking measurements. Gate bias and device bias is supplied by a Keithley 2636B 2-channel SMU. Current is sourced by a Keithley 6220 supply. Voltage measurements are taken using a Keithley 2182A nanovoltmeter. The device under test is connected to all sources and measurement units through a Lakeshore 775 digital switch matrix, with all connections triax up to the device probes. All instruments are connected via daisy chained GPIB, and controlled by software we have written.
Figure 40: Gated Hall system measurement bench

in LabVIEW. All resultant data is processed in our Python code. We have attempted to design the test sequence in as rigorous a method possible, to reduce the myriad of subtle material effects that are known, and those currently unknown. The physical layer of the gated Hall system is comprised of a series of electronic sources, source measurement units, and an automated Hall test bench. Sources and measurement units are shown in FIG. 40.

These connections are shown in (FIG. 41). The two channel SMU is shown at top right. Notice one of the yellow triaxial cables runs directly to the group of cables running toward the left of the image. The gate voltage supply is not connected to the digital switch matrix (shown in the center of the image). It connects directly to the conductive platform on which the sample sits during measurement. The current source, second voltage supply channel, and high precision voltage measurement unit are all connected to the digital switch matrix. The series of yellow triaxial cables bundled together are the switch output connections that connect each source and measure unit to a specific contact position on the VDP device under measurement. These triax cables are converted to coaxial cables at the converted NanoMetrics test bench (shown in FIG. 42). Here, the coaxial cables are converted to clip-like probes. One probe for the conductive test bench floor, and four others connected to each VDP probe. The movable, reversible, magnet is shown in the home position.
Figure 41: Back of gated Hall system showing triaxial cable connections
Figure 42: Converted NanoMetrics test bench
4.3.2 Software layer: LabVIEW interface

The software layer of the gated Hall system is comprised of a stand alone computer running LabVIEW code, connected to all source and meter units by daisy-chained GPIB cables. Each unit is identified in the network by a PCI GPIB instrument number (FIG. 43). An example of one software process is writing the position into the digital switch matrix (FIG. 44). User interface to such processes are greatly improved by design of a friendly user interface (FIG. 45). In this example, the software provides one instance of equipment connections through the digital switch matrix (FIG. 46). Keeping in mind that the process of setting the switch into a single position is one of thousands of iterative switch settings that constitute the automated testing cycle of the gated Hall system.

4.4 Testing methodology in the gated Hall system

4.4.1 Determination of test current: the gated Hall test cycle

The gated Hall system is fully automated. At each test point \( (V_D, V_G) \) it takes a series of three measurements. This is done while maintaining vertical electric field conditions of \( (E < E_{BD,Al_2O_3}) \), continuously monitoring for signs of gate dielectric breakdown, and terminating at the onset of gate
Figure 44: LabVIEW code to write next position to digital switch matrix

Figure 45: LabVIEW front panel. User interface for complicated software control
current. The gated Hall system takes each of the three measurements for mobility within three discrete measurement envelopes.

Inside each test envelope, the gate voltage is turned on first. Sources (voltage or current) are turned on next, within a second of the gate voltage turning on. A variable delay time, one second for our current measurements, is built in before voltage is measured. This ensures sufficient settling time for the measured response. Voltage measurements complete within a second. Once the measurement is complete, the source unit is turned off. Finally, the gate voltage is turned off. The overall measurement time for each individual test envelope is a couple of seconds. The order of each operation is rigidly enforced to ensure a current or voltage source is never applied to the material in a high resistance state ($V_G = 0$ V). Between measurements all equipment is powered off for a full minute to reduce testing strain and any possible heating effects. This reduced duty cycle is important in our gated Hall system. High resolution testing can take 50 hours or more to complete.

In the first measurement envelope a digital switch matrix connects contacts to the source-measure units in the transistor (field-effect) configuration, shown in FIG. 39. Forced drain bias across contacts C1 and C2 results in the drain current ($I_D$). This measurement generates a point on a current-voltage plane ($I_D, V_G$). The collection of these points swept across $V_G$ (device input characteristics) is used to calculate the field effect mobility.

The second and third measurement envelopes are used to measure sheet resistance and Hall
voltage. Current is forced across adjacent contacts (for example C1 and C2) and the resulting voltage is measured (C3 and C4) for $\rho_s$, or current is forced across diagonal contacts (C1 and C3) and voltage measured across (C2 and C4), while the device is submerged in a transverse magnetic field, for $V_{\text{hall}}$. In these measurements, current is often fixed, and the bias voltage is allowed to float. For our material, we cannot allow the drain voltage to float. A floating drain voltage results in the development of destructive electric fields across the gate dielectric. To set a drain voltage maximum at each Hall measurement point, the test current must be allowed to change.

The solution to this problem is to use the measured current from the first test as the forced current for the second and third tests. Each given device bias position ($V_D, V_G$), has a unique drain current ($I_D$). Since $V_D$ and $V_G$ are both set, it is possible to ensure that $V_{GD}$ and $V_{GS}$ are below $V_{\text{max}}$ for $E_{\text{max}}$. Forcing the measured current for a Hall measurement generates Hall results at the same device bias. In this manner, both field-effect and Hall mobilities can be directly compared on the same test device. This is what we refer to as concurrent device measurements.

4.4.2 Experimental test routine and duty cycle

1) All units begin each cycle turned off from an adjustable inter iteration delay. For our material, typically several minutes.
2) Switch position is set for transistor measurement (FIG. 47).
3) The first step begins with the first set of bias conditions ($V_{G,1}, V_{D,1}$) identified as allowable based on accumulation of bias potential ($E_{GS} < E_{BD}$) across the thin dielectric.
4) First gate bias voltage is forced through switch ($V_{G,1}$). Gate voltage reduces large sheet resistance as $V_G$ approaches and exceeds $V_{th}$.
4) The first drain bias voltage ($V_{D,1}$) is forced within the limit that the VDP transistor is operating within the linear device region.
5) While both voltage sources are on, the corresponding drain current ($I_{D,1,\text{meas}}$) is measured. This provides a single point of measurement. As the bias conditions are iterated, these single points are sorted together to form the current-voltage characteristics.
6) The gate bias is always turned on first, and turned off last for each measurement point. Here the drain bias is turned off first, followed by the gate bias.
7) The switch is turned off and the test setup is set on variable delay with all units powered off until next test set.

8) Switch is set to Van der Pauw (sheet resistance) measurement position.

9) As always, the gate voltage is forced first. It is set to the same voltage as in the previous test ($V_{G,1}$).

10) This time, current is forced, instead of voltage, for the resistance measurement. The question is, what current? The previous measurement gives that answer. For a given set of bias conditions ($V_{G,1}, V_{D,1}$), $I_{D,1,\text{meas}}$ is measured. If that current ($I_{D,1,\text{meas}}$) is then forced on the same device, its value is pinned at the same operating point as that from which the transistor data was acquired.

11) While under gate bias and forced current, the voltage across the opposite terminals of the VDP structure ($V_{VDP,1,\text{meas}}$) is measured. This is a four point probe resistance measurement used to calculate sheet resistance.

12) Forced current ($I_{D,1,\text{meas}}$) is turned off, followed by the forced gate bias. The switch is disconnected, and the test waits during a variable delay for the next test step.

13) The switch is then set to the Hall measurement position (FIG. 48).

14) The same gate bias ($V_{G,1}$) is forced. The same current as the last measurement ($I_{D,1,\text{meas}}$) is forced across diagonal VDP contacts.

15) The Hall voltage ($V_{\text{Hall},1,\text{meas}}$) is measured across the opposite diagonals. This measurement is repeated after the sample is submerged in an external magnetic field (the magnet comes out from the test bench and covers the sample). The difference between the two is the Hall voltage ($V_{\text{Hall}}$).

16) The forced test current ($I_{D,1,\text{meas}}$) is powered off, followed by the gate bias. The switch is disconnected and the system waits in the power off state.

17) The next device operating point is selected based on allowable bias conditions ($V_{G,2}, V_{D,1}$) for $V_{G,i}, V_{D,j}$ through all the $i^{th}$ and $j^{th}$ iterations of the full test spectrum.

4.4.3 Removing heating and stress effects: low duty cycle

The gated Hall system is fully automated. At each test point ($V_{D}, V_{G}$) it takes a series of three measurements. This is done while maintaining vertical electric field conditions of ($E < E_{BD,Al_{2}O_{3}}$), continuously monitoring for signs of gate dielectric breakdown, and terminating at the onset of gate
current. The gated Hall system takes each of the three measurements for mobility within three discrete measurement envelopes.

Inside each test envelope, the gate voltage is turned on first. Sources (voltage or current) are turned on next, within a second of the gate voltage turning on. A variable delay time, one second for our current measurements, is built in before voltage is measured. This ensures sufficient settling time for the measured response. Voltage measurements complete within a second. Once the measurement is complete, the source unit is turned off. Finally, the gate voltage is turned off. The overall measurement time for each individual test envelope is a couple of seconds. The order of each operation is rigidly enforced to ensure a current or voltage source is never applied to the material in a high resistance state ($V_G = 0$ V). Between measurements all equipment is powered off for a full minute to reduce testing strain and any possible heating effects. This reduced duty cycle is important in our gated Hall system. High resolution testing can take 50 hours or more to complete.

In the first measurement envelope a digital switch matrix connects contacts to the source-measure units in the transistor (field-effect) configuration. These connections are shown in FIG. 47. Forced drain bias across contacts C1 and C2 results in the drain current ($I_D$). This measurement generates a point on a current-voltage plane ($I_D, V_G$). The collection of these points swept across $V_G$ (device input characteristics) is used to calculate the field effect mobility.

The second and third measurement envelopes are used to measure sheet resistance and Hall...
Figure 48: Schematic for Hall effect measurements

voltage. These connections are shown in FIG. 48. Current is forced across adjacent contacts (for example C1 and C2) and the resulting voltage is measured (C3 and C4) for $\rho_s$, or current is forced across diagonal contacts (C1 and C3) and voltage measured across (C2 and C4), while the device is submerged in a transverse magnetic field, for $V_{\text{hall}}$. In these measurements, current is often fixed, and the bias voltage is allowed to float. For our material, we cannot allow the drain voltage to float. A floating drain voltage results in the development of destructive electric fields across the gate dielectric. To set a drain voltage maximum at each Hall measurement point, the test current must be allowed to change.

An alternative graph shows the important connections of the current source and gate voltage source to the same ground. This is an important feature in the gated Hall system design, in that it both assures the proper sourced gate voltage (relative to the same ground). It also ensures the lack of ground loops that become a source of internal error in measurements. It also clearly shows the method in which gate leakage current is continuously measured. The graph for the Van der Pauw test (the test for sheet resistance) setup is given in FIG. 49. The graph for Hall voltage measurements is shown in FIG. 50.
Figure 49: Cartoon of gated Hall system cabling for VDP testing

Figure 50: Cartoon of gated Hall system cabling for Hall voltage testing
4.4.4 An example of LabVIEW software control: generation of the test routine and duty cycle

Part of the design of the gated Hall system involves the wafers full of VDP test structures. These structures are designed to be measured using and existing automated test bench for current-voltage characteristics while still in the clean room. This pre-scan of the fitness of the devices on the wafer is an important screening process that can reduce time searching for viable test structures. However, over time, the fitness of devices can change. It can take extended searching through the test wafer to find devices that do not fail. A special, five point, two minute pre-scan was developed to test a new device on drain current modulation by gate bias, and gate leakage across the same set of gate bias points. This scan allows many devices that will be unfit to take complete measurements to be sorted and removed quickly. The performance qualities that are searched for are shown in FIG. 51.

LabVIEW software was used to send low level commands across the GPIB connected device measurement matrix. An example of the test routine from the preceding chapter is given here in a series of snapshots of code. These individual frames are part of a single, continuous flow of actions generated by the software. The given example is a Hall measurement test routine. A field-effect test routine would look different.
Figure 52: LabVIEW code: preparing the gate voltage and test current sources

Figure 53: LabVIEW code: turning on the source units in order

Figure 54: LabVIEW code: measuring the Hall voltage and gate leakage current
In the first frame (FIG. 52), the gate bias and current source are primed. Each unit is provided a generic, low-level code example from LabVIEW. In our gated Hall system, we cut snippets from low level code, and paste them into custom designed control. In the second, follow on frame (FIG. 53) information flows along lines from left to right into a sequence block. Here, the gate is shown to turn on first. A timer records the time for each process to be analysed later. A variable delay is set between each operation. Every LabVIEW block has an error state output, shown as the black and yellow wire at the bottom. Interior LabVIEW control protocols attempt to process as many blocks of operations as possible. This can lead to what is known as race tracking. One line of process can race forward, while a parallel process falls behind. This is not allowable in the strict order of operations for our gated Hall measurements. An error message, including (no error) is always sent by all operational blocks at all times in LabVIEW. When two error streams are connected to a Boolean block (AND), no further progress can be made until all streams converge to be compared. In this manner, we force all processes to catch up with one another as operations unfold.

In the third frame (FIG. 54) the Hall voltage is measured, along with the gate leakage current. In the fourth frame (FIG. 55) the current source and gate voltage are turned off. An important concept in LabVIEW is that of the state machine. The state machine performs blocks of code based
on a given input state. Once that block has been performed, depending on the results, an output state is given. The flow of information about what state the system is in, is circular. A change flowing from the output state, flows back into the state machine, and changes based on that state, to a new block of instructions. In this manner, a complicated series of instructions can be nested in a small footprint. Also, those operations can be stated clearly in words (such as, move out the magnet) to better understand process flow. A small static snippet of this code is shown in (FIG. 56). The wires flowing into the rectangular block are data being written into an output file. During operation, data flows continuously at each given point. Test conditions and results are appended to a specified .csv file line after line across a swath of data columns.

4.4.5 Transport calculations: Python code

Along each LabVIEW test frame, data is collected and written to a central .csv text file (FIG. 57). As each frame is iterated along the automated test routine, data is continuously appended to this central file. A short snippet of code from Pandas in Python running on a Jupyter notebook is shown in FIG. 58. After which data is used in the standard mobility calculations, such as the sheet resistance (FIG. 59). Keeping in mind that this is one small example of a suite of measurements used in mobility calculations, and expressed in both standard (two dimensional) graphs, as well as the expanded (3 dimensional) graphs presented.
Figure 57: LabVIEW frame of write to file command

```python
In [2]:
    MachineData = pd.read_csv('EXP_2019_4_23.csv')
    display(MachineData.head())

<table>
<thead>
<tr>
<th></th>
<th>VG</th>
<th>VD</th>
<th>ID</th>
<th>VM</th>
<th>IG</th>
<th>BP</th>
<th>BM</th>
<th>POS</th>
<th>TEST</th>
<th>ITER</th>
<th>NEW</th>
</tr>
</thead>
<tbody>
<tr>
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<td>1.000</td>
<td>22.000</td>
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<td>1.000</td>
<td>4.000</td>
<td>0.000</td>
<td>NaN</td>
</tr>
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<td>1.000</td>
<td>27.600</td>
<td>NaN</td>
<td>-23.200</td>
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<td>4.000</td>
<td>0.000</td>
<td>NaN</td>
</tr>
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<td>-19.500</td>
<td>NaN</td>
<td>NaN</td>
<td>1.000</td>
<td>4.000</td>
<td>0.000</td>
<td>NaN</td>
</tr>
</tbody>
</table>
```

Figure 58: Short snippet of converted .csv raw data file into Pandas on Python

```python
In [22]:
    SheetResistance = pd.DataFrame(np.abs(Resistance['mean'])*np.pi) / (np.log(2))
    SheetResistance.loc[:, 'VG'] = SheetResistance.index

    plt.figure()
    plt.scatter(SheetResistance['VG'], SheetResistance['mean'], s=150, color='k')
    plt.ticklabel_format(style='sci', axis='x', scilimits=(0,0))
    plt.ylabel('Sheet Resistance ($\mu$W/m$^2$ per square')
    plt.xlabel('Gate Voltage (V)')
```

Figure 59: Sheet resistance: an example of Python calculations of processed data from gated Hall system
As shown in the previous section, measurements at each data point are appended to a large, single matrix of information stored in a .csv file. Pandas for python is used to parse the large amount of data used in calculations. The raw input file is shown in FIG. 60.

Notice that the values for current are negative, and within a sub nano-amp range. These are measurements beginning at both bias conditions set to zero. Technically, they are within the safe range, but are also well below the acceptable noise floor. The test number is assigned based on field-effect measurement, Hall measurement without magnetic field, and Hall measurement with magnetic field.

The engine that transforms all of the data into the calculated values is short and succinct. It is shown in FIG. 61. The results for all calculations are filtered by an initial noise parameter. The data generated from FIG. 61 becomes the data shown in FIG. 62. The three primary test conditions are given by the drain and gate bias (vd, and vg) along with the measured/forced drain current (id). All voltage measurements are included under the (vm) column. Drain current is shown under (id). Three point contact resistance is shown under (res), while sheet resistance is shown under (rho).
cnt = 0
for idx, frame in table.groupby(['vg', 'vd']):
    vg, vd = idx[0], idx[1]
    m = (1,-1,vg,vd)
    n = (1,0,vg,vd)
    p = (1,1,vg,vd)
    if frame['vm'].shape[0] == 3:
        # Raw resistance
        res = np.abs(frame.at[m, 'vm']/frame.at[n, 'id'])
        # Resistivity
        rho = np.abs(res*np.pi*np.log(2.0))
        # Hall voltage
        vh = np.abs(frame.at[p, 'vm'] - frame.at[n, 'vm'])
        # Hall coefficient
        rh = np.abs(vh/np.abs(frame.at[m, 'id'])**6.486)
        # Hall mobility
        mnh = rh*rh
        # Add to hall table
        for k,v in zip([res, rho, vh, rh, mnh], [res, rho, vh, rh, mnh]):
            table_hall.at[(vg, vd), k] = v
        # Display
        if cnt < 3:
            display(frame)
        cnt += 1

Figure 61: Python code used to convert raw data to calculated values

Figure 62: Display of calculated values indexed by gate and device bias conditions
Hall voltage and Hall coefficient are shown under (vh and rh). The calculated Hall mobility is shown under (muh). In the first column, $\mu_{Hall}$ is shown to be 63.9 cm$^2$/Vs. This value is anomalously high. It is well within the noise floor, as attested to the low bias values. The device has not yet been turned on. the linear and saturation values for the transconductance are shown under (gmlin and gmsat). These are used in two separate calculations of field-effect mobility under linear and saturation modes (mufelin and mufesat).

In this work, we have chosen to narrow our focus to the linear regime. This is the operating regime of interest for development of our thin film transistors as switching, rather than power applications.

One last note. Each row of information contains information about field-effect mobility, resistance, Hall mobility, and sheet carrier concentration as well. All these data points are indexed according to bias conditions. This is what we refer to as concurrent mobility measurements. In accumulating data in this way, we are able to compare all measurable quantities, apples to apples, across our test matrix.

Finally, one more point of interest in the Python code is the presentation of the data including...
the relation of \( V_D, V_G \), and \( \mu_{FE}, \mu_{Hall}, \) and \( N_S \) (sheet carrier concentration) on the same graph. This is handled by using Triangularization methods of indexing data to be graphed onto a third parameter (shown in FIG. 63). Application of this process generates a mesh object (FIG. 64 that can be used to generate the more complicated graphs of mobility comparisons. Any independent variable, such as mobility, must be mapped to a mesh, if it is to be shown to be dependent on more than one variable.

4.5 Concurrent measured mobility relation to trap density and sheet carrier concentration

Our gated Hall system takes concurrent measurements of current-source characteristics, and Hall characteristics on the same device, at the same time. Hall effect mobility and sheet carrier concentration are related directly to measured Hall voltage. Field-effect mobility and interface trap density are related directly to the current-voltage characteristics of the transconductance and sub-threshold slope respectively. These relationships are shown as follows:

The Hall coefficient \( R_H \) is proportional to the Hall voltage \( V_{Hall} \), the measured potential
generated by the displacement of mobile electrons diverted by an external magnetic field:)

\[ R_H = \frac{V_{Hall}}{I_D B} \] (50)

where \( B \) is the lateral magnetic field strength, and \( I_D \) is the forced drain current.

The Hall mobility is also proportional to \( V_{Hall} \) through the Hall coefficient:

\[ \mu_{Hall} = \frac{R_H}{\rho_S} \] (51)

where \( \rho_S \) is the sheet resistivity measured in the Van der Pauw configuration.

The sheet carrier concentration is inversely proportional to \( V_{Hall} \):

\[ N_S = \frac{I_D B}{eV_{Hall}} \] (52)

where \( e \) is electron charge.

The field-effect mobility is given by the current-voltage characteristics, proportional to the transconductance \( (g_m = \partial I_D/\partial V_G) \):
\[ \mu_{FE} = \frac{g_m L}{C_{ox} V_D W} \]  

(53)

where \( V_D \) is the device bias, \( C_{ox} \) is the capacitance of the dielectric layer, \( L \) and \( W \) are the device length and width.

The interface trap density \( N_{it} \) is also related to the current-voltage characteristics, proportional to the sub-threshold slope (\( SS = \partial \log I_D / \partial V_G \)):

\[ N_{it} = \left( \frac{\log(e) SS}{kT/q} - 1 \right) \frac{C_{ox}}{q}, \]  

(54)

where \( k \) is Boltzmann’s constant, \( T \) is temperature, \( q \) is the fundamental electric charge.

4.6 Evaluation of the gated Hall system

4.6.1 Testing limitations

One major limitation of the gated Hall system is the presence of noise in Hall mobility values. This happens when the device is modulated in a high resistivity state. When the device is under little to no device bias (\( V_G < V_{th} \)). This sharp spike in resistance is shown across device and gate bias conditions in FIG. 67.

The primary region of interest for mobility measurements for our devices has been in the device linear region. Though it is possible to use an analytical expression for data taken from the device saturation region, we chose to avoid this region in our compiled data sets.

Limitations are set on measurements for device and gate bias conditions set a potentials that generate vertical electric fields across the device. Maximum gate-to-source voltage is limited to the electric field across the gate dielectric less than breakdown. Gating is necessary to take mobility measurements on the device.

4.6.2 Summary of the gated Hall design

Based on the specific needs of measuring high resistivity oxide thin-film transistors we had to monitor all potentials building within the device at time of measurement, and design an automated test rou-
tine that could generate large amounts of data from the device without destroying it. We wrote the test protocols for concurrent measurements to obtain data from both field-effect and Hall mobilities, on the same device at the same time. This enabled direct comparisons of transport parameters, not only at single device operating points \((V_D, V_G)\), but across the entire safe operating area. We also rigorously tested the equipment and results, including investigation into the correlation between the two mobilities. We determined the limitations of each of the methods used to derive the mobility, and compared them in a series of novel visualizations. We present our gated Hall system as a new method of gaining better insight into electronic transport of high resistance films.

5 RESULTS

5.1 Validation of gated Hall system

Testing conditions for IV characteristics and field-effect mobility calculations are straightforward and yields quality, repeatable results. IV curves have been catalogued for linear (FIG. 65) and log (FIG. 66) current values. Modulation of the large off state resistance by gate voltage is shown in FIG. 67. For each data point, for forced values, there is a clear corresponding value. For this reason,
the results from the field-effect mobility calculations are stable through the region in which the Hall mobility becomes unstable, all the way down to \( V_G = 0 \) V. Due to this, the discussion of validation techniques revolve around Hall measurements.

5.1.1 Current-voltage characteristics across both adjacent and diagonal Van der Pauw contacts

Values for current-voltage characteristics were prepared by taking a series of measurements across adjacent VDP contacts (the method we used) and comparing them to the difference in measurements across the diagonal contacts. The results showed a slightly higher value for current measurements across adjacent contacts than diagonal. These comparisons for the input and output transistor characteristics are shown in FIG. 69 and FIG. 70.

5.1.2 Repeatability testing

Sheet resistance measurements in gated Hall measurements are rock solid and highly repeatable (FIG. 68).

The primary contribution to error (above the measurement noise floor) in Hall measurements
Figure 69: Comparison of adjacent to diagonal VDP measurements for device input characteristics

Figure 70: Comparison of adjacent to diagonal VDP measurements for device output characteristics
Figure 71: Fluctuation in repeated measurement of the Hall voltage in our material is the Hall voltage. The Hall voltage can become vanishingly small under increasingly resistive material. This is due to limitations set on the forced test current, reducing the number of electrons forced across the diagonal contacts of the VDP device under magnetic field.

As the Hall voltage becomes smaller, naturally occurring small variations in the potential become magnified. These magnified variations then lend themselves to variation of the final calculations of the Hall mobility, or more specifically, the contribution of the Hall coefficient to the Hall mobility. Tests on the measured voltage repeatability with and without the influence of an external magnetic field, for a single device, have shown this variation (FIG. 71). The difference between the values, with and without the external magnetic field (B) is the measured Hall voltage ($V_{Hall}$), shown in FIG. 72. For testing under the limits of maximum field conditions on the gate dielectric, our ALD deposited Al$_2$O$_3$ gate material has been shown to be consistently reliable in suppression of gate leakage (FIG. 73).

We have shown that by sufficient delay time (and by better results afforded by higher mobility films) that these fluctuations in Hall voltage are insignificant sources of error in the final Hall mobility results.
Figure 72: Fluctuations in the measured Hall voltage in our sample

Figure 73: Low gate leakage for our ALD deposited Al₂O₃ thin film dielectrics
5.1.3 Space charge layer accumulation under continuous testing conditions

Our metal oxide thin film transistors are electrostatic doped into lower resistance materials through the application of a gate voltage bias across the gate dielectric. This process builds charge at the dielectric / active layer interface. A common problem in these devices is the buildup of a remainder of charge after the device is turned off. This charge (space charge layer) can persist to following measurements, reducing the effective gate voltage supply by the amount of charge remaining from the last test cycle.

Continuously repeated testing over a 120 minute interval at 5 V gate bias and 1 V drain bias for a given high resistance material, resulted in a fat tail exponential graph commonly seen in the literature describing space charge accumulation (FIG. 74).

Under the effects of additional charge layer screening, subsequent values of the gate voltage are reduced. This reduction yields an apparent right shift in the threshold voltage. We identified this trend in this particular material from FIG. 74 by taking drain current profiles before and after the 120 minute test routine. These results are shown in FIG. 75. The same results are rescaled to better
Figure 75: Apparent threshold voltage shift after 120 min. continuous testing of high resistance sample.

These results came from deposited material with high resistance and low mobility. Subsequent tests of lower resistance, higher mobility material did not exhibit a significant change in values after testing. The large amount of time given to each test point in our automated gated Hall system was designed, in part, to reduce these possible measurement effects. Testing of $V_{meas}$ for repeated measurements with significant delay time between measurements (5 minutes) did not show signs of these space charge effects.

5.1.4 Stretched exponential function

The stretched exponential function is used to fit data involving the accumulation of trap centers at the dielectric semiconductor interface. The function has been used to describe the random distribution of transport and trapping sites of electrons in disordered media [58]. The stretched exponential function is also known as Kohlrausch law.
Figure 76: Close up of FIG. 75.
The values for $\tau$ and $\beta$ can be expressed in terms of random probabilities involving electrons either moving through conductive pathways or becoming entangled in trap states as they percolate through the material. The novelty expressed in this paper is that the stretched exponential function, often used as a convenient model to fit physical data due to its rather relaxed relation to physical processes, has been shown to correlate in some manner with the way electrons move through a material. A quantity which is directly measured on the test bench.

5.1.5 Measurement sanity check: calculation of oxide capacitance

The gate oxide capacitance was independently measured by LCR meter, giving an average value normalized to test device geometry of $C_{ox} = 319 \text{ nF/cm}^2$. Using EQ. 58 and the geometry of the
capacitor test structure, the dielectric relative permittivity was determined to be $\varepsilon_r = 9$. This value of $\varepsilon_r$ was then used along with our gated Hall system Van der Pauw device geometry to determine $C_ox$ for our device. The calculated value of $C_ox$ was used in EQ. 57 along with the extracted transconductance from the device input, or transfer ($I_D - V_G$) characteristics, to determine the field effect mobility, at each device operating point ($V_D, V_G$).

Comparisons of field-effect and Hall mobility under low field conditions ($V_D = 0.3$ V) and across gate voltage ($V_G = 0.2$ V to $V_G = 9$ V in 0.2 V steps) are shown in FIG. 87. Here, mobility is shown to modulate by gate bias voltage from a value close to zero at $V_G = 0$ V to around 20 cm$^2$/Vs at $V_G = 9$ V. These values were consistent from testing individual photo-lithographically defined test structures across a series of five wafers fabricated under nominally identical conditions.

The close agreement in values for both mobilities could be the result of several factors. Measurements of the field effect mobility are generated from the same device and time, as the Hall mobility. Also, the data is collected within a narrow range of low device bias (small lateral electric field conditions). Increasing values of drain voltage do begin to show divergence between the two. However, these values push the device into saturation mode. Our goal was to concentrate on data within the
Figure 79: Restriction of forced test current during measurements based on dielectric breakdown values.
linear region of operation. We suggest, that if $\mu_{FE} \approx \mu_{Hall}$ (as shown in the linear, low-field region) that the oxide capacitance can be solved by using EQ. 57 with a substitution of $\mu_{Hall}$ for $\mu_{FE}$:

$$ C_{ox} = \frac{g_m L}{\mu_{Hall} V_D W} $$

Measurement of $C_{ox}$ using EQ. (59) is shown in FIG. 81. The value for oxide capacitance settles above the noise floor to $C_{ox} \approx 320$ nF/cm$^2$. This value is approximately equal to the independently measured value given by the LCR meter. This blending of methods used in calculation of electron mobility to find a matching solution for oxide capacitance is only possible due to the method of concurrently measuring both mobilities during testing. In this case, using both mobilities in a complementary manner acts as a system check, indicating that the relations between the mobilities shown in FIG. 87 are correct.

5.1.6 Comparisons of measured gate oxide capacitance to mobility results

The equation for field-effect mobility (in the linear operating region) is given by:
The gate oxide capacitance was independently measured by LCR meter, giving an average value normalized to test device geometry of $C_{ox} = 319$ nF/cm$^2$. Using EQ. 58 and the geometry of the capacitor test structure, the dielectric relative permittivity was determined to be $\varepsilon_r = 9$. This value of $\varepsilon_r$ was then used along with our gated Hall system Van der Pauw device geometry to determine $C_{ox}$ for our device. The calculated value of $C_{ox}$ was used in EQ. 57 along with the extracted transconductance from the device input, or transfer ($I_D - V_G$) characteristics, to determine the field effect mobility, at each device operating point ($V_D, V_G$).

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We suggest, that if $\mu_{FE} \approx \mu_{Hall}$ (as shown in the linear, low-field region) that the oxide capacitance can be solved by using EQ. 57 with a substitution of $\mu_{Hall}$ for $\mu_{FE}$:

$$C_{ox} = \frac{g_m L}{\mu_{Hall} V_D W}$$

(59)

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5.1.7 Hall mobility shown to increase by sheet carrier concentration and gate voltage

The relationship of Hall mobility increasing by sheet carrier concentration in IGZO TFTs [59], and the $N_s$ dependence of $\mu_{Hall}$ has also been observed in our material (FIG. 82). Here the results for both $\mu_{FE}$ and $\mu_{Hall}$ for all values across the safe operating area are displayed. The graph shows outliers at low $N_s$ and low mobility correspond for test conditions of ($V_G < 4$ V), the Hall measurement noise floor.
Figure 82: Comparison of mobility to sheet carrier concentration across full range of bias values. Noise floor values ($V_G < 4 \text{ V}$) shown in transparency (from [2]).

5.2 Representation of data in the gated Hall system

5.2.1 Flexibility of data representation in three dimensions

All measurable quantities are indexed according to the gate and device bias conditions. This allows flexibility in the comparisons to be generated into graphs. For instance, the measurement noise floor of the gated Hall system, as seen from the perspective of drain bias and forced current, is shown in FIG. 78. When FIG. 78 is rotated from a top down viewpoint, measurement restrictions, based on allowable development of electric field across the thin gate dielectric are clearly shown (FIG. 79). Nothing is explicitly mentioned of gate bias in these graphs. Information about $V_G$ is present, but buried in the data. Gate and device bias information in relation to mobility can be explicitly expressed (FIG. 80). However, drain current is not explicitly addressed, and becomes buried in the new data visualization arrangement.

When FIG. 80 is rotated to the top down viewpoint (FIG. 83), data is continuously present across the $V_G$, $V_D$ span. This is due to the selection of allowable measurement conditions at each bias point. A consequence of carefully selecting all measurement conditions.

In another arrangement, the bias conditions from FIG. 80 can be used as a basis of viewing the modulation of sheet resistance across the device (FIG. 84).
Figure 83: Continuous measurement spectrum across bias conditions.

Figure 84: Sheet resistance modulated by device and gate bias.
Transistor input and output characteristics are compared side by side (FIG. 85). A 2-D contour of Hall mobility is mapped onto the surface of each plot. Mobility is shown to be modulated by gate voltage, across the x-axis in \( (I_D-V_G) \), and along the \( V_G \) lines in the \( (I_D-V_D) \) plot. This is only one of many possible representations that can be used to view broad comparisons in the collected data.

### 5.2.2 Contour plots of concurrent mobility measurements

The sum of collected mobility data measured by the gated Hall system is displayed in 2-D contour plots (FIG. 86). The data consists of gate voltage steps of 0.2 V from 0 to 9 V, across lateral bias steps of 0.1 V from 0 to 4 V. Measurements of the Hall mobility are restricted by the noise floor \( (V_G < 4 \text{ V}) \), while the field effect mobility is restricted by the requirement that calculations for \( \mu_{FE} \) in EQ. (57) are valid only in the device linear region. This region is defined by \( V_D < V_G - V_{th} \), where the threshold voltage is estimated to be \( (V_{th} = 1.4 \text{ V}) \) using the constant current method [50].

The Hall mobility saturates for increasing lateral electric field, and may be expected to decrease at higher fields, due to electron scattering effects resulting from a larger electronic drift velocity in an increasing uniform electric field. If sufficiently large, contact resistance could be responsible for the lag in \( \mu_{FE} \) compared with \( \mu_{Hall} \) shown in FIG. 86. However, the contact resistivity \( (\rho_c) \) has
been calculated \cite{53} to be $\rho_c \approx 1 \times 10^{-4} \ \Omega \text{ cm}^2$, or 20 $\Omega$ contact resistance for our VDP device. This value is several orders of magnitude less than the total measured resistance $R_{\text{tot}} = 30 \ \text{k$\Omega$}$ at its lowest value, obtained at the highest gate voltage of $V_G = 9 \ \text{V}$. This suggests that contact resistance is not a significant factor in mobility calculation for our device.

5.2.3 New methods of representing mobility

As a demonstration of the flexibility of the data visualization enabled by this gated Hall system, the transistor input and output characteristics are compared side by side (FIG. 85). A contour of Hall mobility is mapped onto the surface of each plot. Mobility is shown to be modulated by gate voltage, across the x-axis in $(I_D-V_G)$, and along the $V_G$ lines in the $(I_D-V_D)$ plot. This is only one of many possible representations that can be used to view broad comparisons in the collected data.

Figure 86: Hall mobility mapped across device bias conditions.
5.3 Design of experiment: bridging the gap between experimental test results and theory

Having developed the gated Hall system to meet the measurement needs of our ZnO TFTs, along with extensive error checking of our data, we developed a design of experiment to compare trap states to measured electrical results [3]. In this experiment, we chose to deposit our films by atomic layer deposition (ALD).

Atomic layer deposition of TFT devices has been shown to have advantages over other techniques such as sputtered and PLD films [43]. ALD allows a level of control of growth conditions that are repeatable, highly tunable, at temperatures near room temperature [19]. Device stacks (such as gate dielectric, semiconductor, and encapsulation layers) can be deposited under unbroken vacuum within the deposition chamber. This allows deposition of devices with reduced exposure to possible contaminants between interfaces. Conversely, oxygen or chemical dopants can be introduced in the deposition cycle at any time [1].

Dielectric and active layer material for our devices was deposited using a Veeco Fiji F200 atomic layer deposition chamber at 250 °C, with a growth rate of 0.9 Å per cycle for each. Trimethylaluminum and diethylzinc were used as the metal source for the gate dielectric and channel layer, respectively. A remote oxygen plasma provided the oxygen source for both films. Argon served as...
We take advantage of this tight control over deposition conditions in our ALD deposited Al₂O₃ dielectric layer (25 nm) / ZnO active layer (50 nm) bottom-gated TFTs (FIG. 39), as well as post-process annealing, to investigate transport and trapping effects at the ZnO/Al₂O₃ interface. Trap states degrade carrier transport properties such as: device ON current, threshold voltage, sub-threshold swing, and both field-effect and Hall mobilities [39]. Several methods have been developed to generate estimates of interface trap densities such as fitting the change in threshold voltage under positive and negative gate bias stress [30], capacitive-voltage measurements [62], and by using the subthreshold slope (SS) [13].

In order to compare these effects, four wafers were prepared (W1-W4). In the first two wafers, the dielectric and active layers were deposited sequentially without break in chamber vacuum (in situ). The second set of wafers were exposed to clean room ambient air between depositions (ambient exposed). Following deposition, two wafers from each set were oven annealed in clean room ambient air for one hour at 400 and 700 °C respectively (FIG. 88). These test conditions are summarized in TABLE 1.

Based on previous investigation into these materials, devices made from post-anneal temperatures less than 400 °C exhibited highly degraded device properties. In order to observe maximum
Figure 89: 2-θ XRD of ALD ZnO under 400 and 700 °C anneal, in situ and ambient anneal conditions.

differences in annealed wafers, we selected the highest temperature allowable to us in our clean room air oven, of 700 °C. Post-process annealing of ALD ZnO thin films has been shown to increase grain size through 900 °C anneals [35]. Overall crystal structure was measured using a PANalytical X’pert Pro MRD x-ray diffractometer. Of the three most typical peaks for crystalline ZnO [9, 60], peaks were observed at 34.4° corresponding to (002) orientation for all wafers. XRD analysis of all wafers (FIG. 89) shows an increase in measured peak intensity, and peak width, by post-anneal temperature. This suggests an increase in average grain size (reduction in overall grain boundary effects), under increasing post-anneal temperatures, a trend that has been shown in PLD deposited ZnO wafers [8].

Transport measurements for each of the four wafers were taken on a photolithographically defined, 100×100 μm Van der Pauw (VDP) test structure (FIG. 39). Devices were measured in 250 mV steps across gate and drain bias voltages of 0 to 9 V and 6 V respectively under continuous monitoring of a gate leakage current of $I_G < 10$ nA. A subset of these values within a given device bias (250 mV) were then selected for comparisons. These comparisons include: drain current response, sub-threshold slope, field-effect and Hall mobility, interface trap density, and sheet carrier concentration, with attention primarily to subthreshold and linear device regions, using our gated Hall system [2]. These results are shown in TABLE. 3.
This work is seen to extend the capabilities of the gated Hall system not only perform standard mobility measurements, but through careful design of experiment, to fill the larger gap in connecting material theory to experimental results. In this work, we investigate interface and grain boundary effects, analyze their measured response, and develop a simple model describing underlying electronic transport in each test mode.

5.3.1 Experimental variable 1: Interface effects from exposure to ambient conditions during deposition

The first deposition condition variable is exposure to ambient air between the dielectric / active layer process, compared to wafers that remain in vacuum between those two depositions. We feel that by comparing gated Hall results for wafers fabricated under both conditions, we may be able to demonstrate correlations between experimental results and theory. The difference in electrical characteristics between two otherwise identical wafers, differing only in additional environmental exposure between the dielectric and active layers, could possibly reflect current interface state theory.

An external field can induce band bending near the semiconductor surface [67]. A simple arrangement to examine these properties is a metal-semiconductor junction with applied external voltage (shown in FIG. 90). At $V = 0$ V the energy band is flat. When a bias voltage is applied to the metal, the electric field can penetrate into the semiconducting material. Under the conditions $V > 0$ V the electric field causes electrons to accumulate near the semiconductor surface, bending the band down. For $V < 0$ V, the band bend up (FIG. 90).
Figure 91: Adsorption of acceptor molecule on surface (from [67])
Band bending can occur when an acceptor molecule is adsorbed onto the surface of an n-type semiconductor. In FIG. 91, an acceptor molecule is shown approaching a semiconductor surface. The empty outer orbital of the acceptor molecule accepts electrons from the semiconductor surface. This generates an electric field, bending the bands up near the semiconductor surface.

Investigation into exposure to ambient conditions has been explored [29]. Adsorption of ambient oxygen molecules onto the surface of the semiconductor surface has been shown to increase device instability along with the introduction of impurities (FIG. 92).

In our current work, we are interested in comparing measured results between two deposition conditions. In one set of conditions, devices are exposed to ambient conditions between the dielectric and active layer depositions. In the other, the dielectric and active layers are deposited while remaining in vacuum. The difference between the measured results of the two deposition conditions should indicate in some manner the influence directly caused by the presence of molecules from ambient conditions on the semiconductor surface.

5.3.2 Experimental variable 2: Grain boundary effects from post-annealing

The second deposition condition variable is post process oven annealing temperature. Post process oven anneals have been shown in the literature to increase grain size across the material. We search
for correlations between reduction in overall grain boundaries (increase in grain size) to measured
gated Hall system results.

Grain boundaries in nano-crystalline ZnO leads to defects in the band gap. These defects are
charged by carriers from the grains [15]. Charge balance at the grain level generates a depletion
zone of energetic barrier height \( (E_b) \) to charge carriers moving through the material. Models for
carrier transport in polycrystalline silicon have been used to model grain effects in ZnO. A model
for an effective mobility \( (\mu_{eff}) \) dominated by thermionic emission across grain boundaries (with
grain-centric energy barriers \( E_g \) is given by:

\[
\mu_{eff} = \mu_0 \cdot \exp\left(\frac{-E_b}{kT}\right) \tag{60}
\]

Two expressions for barrier height can be derived. Each depends on the charge carrier trap
density \( (Q_t) \):

\[
E_b = \frac{e^2Q_t^2}{8\varepsilon\varepsilon_0 n_D} \tag{61}
\]

For \( Ln_D > Q_t \)

\[
E_b = \frac{e^2L^2n_D}{8\varepsilon\varepsilon_0} \tag{62}
\]

For \( Ln_D > Q_t \)

where \( Q_t \) is the charge carrier trap density at the grain boundary, \( \varepsilon\varepsilon_0 \) is the static dielectric constant,
\( n_D \) is the carrier density in the bulk of the drain, and \( L \) is the grain size.

When \( Ln_D > Q_t \), the trap states are not completely filled, and the nano-crystalline grains are
completely depleted. When \( Ln_D < Q_t \), the grains are only partially depleted and the traps are
completely filled. \( E_B \) increases with \( n_D \) until a maximum at \( Ln_D = Q_t \), then decreases by \( 1/n_D \). A
value for the trap density of ZnO grown by PLD is \( Q_t = 1.5 \times 10^{13} \text{ cm}^{-2} \) [15].

Three possible electronic transport paths across grain boundaries (FIG 24) include thermionic
emission, thermionic field emission, and field emission [55]. Field effect emission involves the quan-
tum mechanical tunneling of electrons through potential barriers.
5.3.3 Design of experiment results

In a first step of deposition condition comparisons between wafers, we focus on drain current modulation in transistor output characteristics at maximum measured gate bias \((V_G = 9 \, \text{V})\) at a given device bias \((V_D = 250 \, \text{mV})\). These results, along with measured transistor input characteristics are shown in FIG. 93. Drain current density has been shown to be an important device parameter in these materials when comparing device performance across material deposition processes [7]. Increase in current density by post annealing has been shown in ZnO TFTs [4]. Our results show that, grouped by temperature, \(I_{D,\text{max}}\) doubled for the 400 °C anneal series (7.4 to 15.3 µA), from in situ to ambient deposition conditions. However, \(I_{D,\text{max}}\) fell by half (51.8 to 26.9 µA) from the 700 °C anneal series, in situ to ambient. Overall, drain current increased from 400 to 700 °C anneal temperature: 150% increase for in situ, and 55% increase for ambient exposed wafers.

In a second step of deposition condition comparisons, we compare mobility as well as sheet carrier concentration. In calculating field-effect mobility, values for current and voltage used to determine transconductance (EQ. 53) are well defined from device on conditions, down through the subthreshold region toward the device biased into the off state. The results follow a clear path across values within the linear operating regime in which they are valid. All wafers follow a trend in increasing mobility and sheet carrier concentration under increasing positive gate bias voltage, similar to our previous results from PLD deposited ZnO TFT wafers [2]. Field-effect and Hall mobility are calculated using two separate methods. Field-effect mobility is derived from current-voltage characteristics, in which each set of forced bias conditions \((V_D \text{ and } V_G)\) generate a clear result for current. Hall mobility is derived partially by mobile electrons deflected by a magnetic field \((V_{\text{Hall}})\). When \(V_{\text{Hall}}\) becomes small, values for \(\mu_{\text{Hall}}\) become erratic.

A measurement noise floor in \(\mu_{\text{Hall}}\) and \(N_S\) is observed in our gated Hall system for devices biased in the subthreshold region \((V_G < V_{\text{th}})\). In this region (shaded in FIG. 94), sheet resistance becomes large \((\rho_S > 250 \, \text{MΩ})\). Large values for sheet resistance quickly generate large vertical electric fields \((E > 4 \, \text{MV/cm})\) from the applied gate voltage to the device bias source and drain, across the gate dielectric, during device testing [2]. In order to keep these electric fields below the electric breakdown of the gate dielectric, Hall test current becomes vanishingly small \((I_D < 10 \, \text{nA})\).
Figure 93: Transistor input (inset) and output characteristics for ZnO-TFT fabricated as indicated in-situ or with ambient exposure and after either 400 °C or 700 °C post deposition anneal.
Low allowable test current results in low measured Hall voltage ($V_{Hall} < 10 \mu V$ at $V_D = 250 \text{mV}$). These small values for Hall voltage in the sub-threshold region generate noise in Hall mobility and sheet carrier concentration results. Values for $\mu_{Hall}$ and $N_S$ are included in our data to identify limitations of our Hall testing, and to compare with field-effect mobility results in this sub-threshold region.

In FIG. 94 c) and d), 700 °C annealed values for sheet carrier concentration and Hall mobility converge above the measurement noise floor while output current is reduced. However in FIG. 94 a) and b), 400 °C annealed values do not emerge from measurement continue to exhibit a large amount of noise beyond the sub-threshold region, forcing us to bin the results within two ranges, 10 to 40 ($\times 10^{12}$ cm$^{-2}$) for in situ, and 20 to 50 ($\times 10^{12}$ cm$^{-2}$) for ambient. Overall, $N_S$ increases by gate voltage (FIG. 94 a) and b)), along with output current (FIG. 93 a) and b)). At the same time that $N_S$ and $I_D$ seem to modulate by gate current, and increase from in situ to ambient deposition conditions, $\mu_{Hall}$ remains essentially flat ($\mu_{Hall} < 5 \text{cm}^2/\text{Vs}$ for both). In order to uncover the additional source of noise in our measurements of 400 °C annealed wafers above sub-threshold, we need to make additional comparisons, beginning with the relation of sheet carrier concentration to interface trap density.

When sheet carrier concentration is less than trap density the primary mode of transport is hopping between localized states. This is supported by models developed describing dielectric/active layer interface states and grain boundary traps in these nano-crystalline zinc oxide thin films generating localized states in the ZnO bandgap that are, in terms of energy, positioned in the bandgap below the conduction band minimum [60, 27]. In the 400 °C annealed wafers, sheet carrier concentration remains buried in trap states ($N_S < N_{it}$) for all values of $V_G$, with output current increasing from in situ to ambient deposition conditions. In the 700 °C annealed wafers, sheet carrier concentration emerges from trap states ($N_S > N_{it}$) at a given $V_G$ for $V_G > V_{th}$, with output current falling from in situ to ambient deposition conditions. In all cases, $N_{it}$ increases from in situ to ambient depositions; increasing ten times faster for the 400 °C annealed set than the 700 °C annealed.

The observed noise in $N_S$ beyond the sub-threshold noise floor in 400 °C annealed wafers could be the result of hopping transport of localized electrons. The Lorentz force ($F = qE + qv \times B$) is proportional to electron velocity ($v$) of non-localized electrons. Localized transport with lower $v$,
Figure 94: Mobility and sheet carrier concentration results for 400 °C post annealed material in situ and ambient exposed a) and b). 700 °C post anneal in situ and ambient exposed c) and d). Measurement noise floor in subthreshold region shown in grey.
Figure 95: Comparisons of measured $V_{\text{Hall}}$ for 400 and 700 °C wafers.

would generate lower $V_{\text{Hall}}$ (as $v \propto V_{\text{Hall}}$). Investigation into Hall effect measurements of organic semiconductor transistors, in which localized transport is the primary means of conduction have shown similar reduction in values for the Hall voltage [52]. In order to examine these results, measured values for $V_{\text{Hall}}$ for all wafers (biased at $V_D = 250$ mV) were compared (FIG. 95). In the 700 °C annealed wafers ($N_s > N_{it}$) values for $V_{\text{Hall}}$ converge above the sub-threshold region. In the 400 °C annealed wafers ($N_s < N_{it}$) values for $V_{\text{Hall}}$ remain noisy through the entire range of measurements, around an order of magnitude less than the 700 °C annealed wafers. These low values of $V_{\text{Hall}}$, caused by localized transport in the 400 °C annealed wafers generate the erratic results in $N_S$ seen in FIG. 94 a) and b).

In review, we develop a simple model to describe the measured results from our gated Hall system. Under increasing positive gate bias, the Fermi level is pushed up from within the bandgap, toward the mobility edge (the diving line between localized and non-localized transport). For our 400 °C annealed wafers, $N_{it}$ is at least two times larger than $N_S$ (across $V_G$ in $V_{D,\text{linear}}$) shown in FIG. 94 a) and b). Electron transport in this region could be dominated by the presence of traps (FIG. 96 a)), in which electrons are driven from trap state to trap state under the influence of an
Figure 96: Possible conduction mechanisms, 400 °C post annealed in situ and ambient exposed a) and b), 700 °C post annealed in situ and ambient exposed c) and d). Grey line suggests a position of the Fermi energy under $V_{G,\text{max}}$. Valence band maximum not shown.

..., external electric field ($V_D$). Additionally supplied trap states in this region, measured in part by an increase in $N_{it}$ from ambient exposed wafers could increase the number of available pathways accessible to hopping electrons (FIG. 96 b)), increasing measured current, as seen in our data (FIG. 93 a) to b)) without significantly increasing Hall mobility due to the lack of non-localized transport.

For the 700 °C annealed wafers, biased at $V_G > V_{th}$ and $V_{D,\text{linear}}$, sheet carrier concentration emerges from trap states (FIG. 94 c) and d)). As gate bias pushes the Fermi level above the mobility edge, electrons begin to populate non-localized free states (FIG. 96 c)). These additional free electrons could explain the large increase in drain current and mobility, from the 400 °C to

<table>
<thead>
<tr>
<th>Process step</th>
<th>Wafer 1</th>
<th>Wafer 2</th>
<th>Wafer 3</th>
<th>Wafer 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALD chamber vacuum</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>$\text{Al}_2\text{O}_3$ deposition</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Chamber break, ambient exposure, replace in chamber</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\text{ZnO}$ deposition</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>400 °C post process anneal</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>700 °C post process anneal</td>
<td></td>
<td></td>
<td></td>
<td>X</td>
</tr>
</tbody>
</table>

Table 1: Experimental setup
Table 2: Comparisons by wafer of maximum device characteristics ($V_{G,max} = 9$ V).

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Deposition</th>
<th>Annealing ($^\circ$C)</th>
<th>$I_{D,max} (V_{G,max})$ ($\mu$A)</th>
<th>$SS_{max}^{} (V$ dec$^{-1})$</th>
<th>$\mu_{FE} (V_{G,max})$ (cm$^2$/Vs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>W1</td>
<td>in situ</td>
<td>400</td>
<td>7.4</td>
<td>0.801</td>
<td>6.1</td>
</tr>
<tr>
<td>W3</td>
<td>ambient</td>
<td>400</td>
<td>15.3</td>
<td>0.967</td>
<td>8.8</td>
</tr>
<tr>
<td>W2</td>
<td>in situ</td>
<td>700</td>
<td>51.8</td>
<td>0.101</td>
<td>28.7</td>
</tr>
<tr>
<td>W4</td>
<td>ambient</td>
<td>700</td>
<td>26.9</td>
<td>0.153</td>
<td>14.7</td>
</tr>
</tbody>
</table>

Table 3: Comparisons by wafer of maximum device characteristics ($V_{G,max} = 9$ V).

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Deposition</th>
<th>Annealing ($^\circ$C)</th>
<th>$\mu_{Hall} (V_{G,max})$ (cm$^2$/Vs)</th>
<th>$N_{it} (V_{G,max})$ ($\times10^{12}$ cm$^{-2}$)</th>
<th>$N_{S} (V_{G,max})$ ($\times10^{12}$ cm$^{-2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>W1</td>
<td>in situ</td>
<td>400</td>
<td>&lt; 5</td>
<td>66.6</td>
<td>[10 : 40]</td>
</tr>
<tr>
<td>W3</td>
<td>ambient</td>
<td>400</td>
<td>&lt; 5</td>
<td>80.9</td>
<td>[20 : 50]</td>
</tr>
<tr>
<td>W2</td>
<td>in situ</td>
<td>700</td>
<td>24.3</td>
<td>6.7</td>
<td>17.9</td>
</tr>
<tr>
<td>W4</td>
<td>ambient</td>
<td>700</td>
<td>14.7</td>
<td>11.1</td>
<td>15.6</td>
</tr>
</tbody>
</table>

700 °C in situ annealed wafers (FIG. 93 a) to c)). Additional trap states for ambient exposed 700 °C annealed wafers could pull free-like electrons into interface trap states (FIG. 96 d)), reducing mobility from in situ to ambient exposed wafers, as seen in our data (FIG. 94 c) to d)), and drain current (FIG. 93 c) to d)).

In conclusion, our data has shown that exposure to contaminants between the dielectric/active layer interface increase total trap states; while increasing post process annealing temperature is shown to reduce trap states. Also, we observe results that drain current, field-effect mobility, and Hall mobility move together, and follow two separate trends in our wafers based on post process anneal temperature. In the 400 °C anneal set, the primary transport method is suggested to be trap to trap ($N_{S} < N_{it}$), with drain current and mobility increasing as the number of trap states increase. Transport in the 700 °C anneal set is considered to be a mixture of electrons biased into the conduction band ($N_{S} > N_{it}$), with trapping effects at the dielectric/active layer interface, where increasing trap states reduce drain current and mobility. The simultaneous current-voltage and gated Hall effect technique has provided the measurement degrees of freedom necessary to observe these effects, and this technique is expected to play an important role in electronic materials and device development going forward.
6 Conclusion

Based on the specific needs of measuring high resistivity oxide thin-film transistors we had to monitor all potentials building within the device at time of measurement, and design an automated test routine that could generate large amounts of data from the device without destroying it. We wrote the test protocols for concurrent measurements to obtain data from both field-effect and Hall mobilities, on the same device at the same time. This enabled direct comparisons of transport parameters, not only at single device operating points \((V_D, V_G)\), but across the entire safe operating area. We also rigorously tested the equipment and results, including investigation into the correlation between the two mobilities. We determined the limitations of each of the methods used to derive the mobility, and compared them in a series of novel visualizations. We present our gated Hall system as a new method of gaining better insight into electronic transport of high resistance films.
References


[25] Hideo Hosono. “How we made the IGZO transistor”. In: Nature Electronics 1.7 (2018), p. 428. ISSN: 25201131. DOI: 10.1038/s41928-018-0106-0. URL: http://dx.doi.org/10.1038/s41928-018-0106-0.


Zhen Zhang and John T. Yates. “Band bending in semiconductors: Chemical and physical consequences at surfaces and interfaces”. In: Chemical Reviews 112.10 (2012), pp. 5520-5551. ISSN: 00092665. DOI: 10.1021/cr3000626.