Fall 2011

CEG 260-01: Digital Computer Hardware and Switching Circuits

John C. Gallagher
Wright State University - Main Campus, john.gallagher@wright.edu

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Objectives and Goals
This course covers the design and analysis of basic digital circuits for computation. Topics will include number systems, basic Boolean algebra, combinational circuit design and analysis, basic Medium Scale Integration (MSI) components, basic memory devices, basic sequential circuits, and binary arithmetic. At the end of this course you should be able to design, optimize, and implement combinational logic for a variety of applications. You should also be familiar with basic MSI components and sequential circuit concepts in preparation for more advanced study of computer architecture, sequential circuit analysis, design, and optimization.

Meeting Time and Place
Tuesday and Thursday, 12:20 PM - 1:35 PM
155 Russ Engineering Center

Instructor
John C. Gallagher
352 Russ Engineering Center
john.gallagher@wright.edu (email preferred to phone)

Office Hours
Tuesday and Thursday, 1:45 - 3:00 PM and by appointment

Textbook (Required)
M. Morris Mano and Charles R. Kime
Prentice Hall, 2008
ISBN: 0-13-600158-0

Textbook (Optional Reference)
Digital Design (1st Edition)
F. Vahid
John Wiley and Sons, 2007
ISBN: 978-0-470-04437-7

Grading
Your grade will be determined by your performance on two written exams (midterm and final) and a sequence of four labs.

You will receive a grade of 0 to 100 on each of six formal class activities (two written exams and four laboratory exercises) you complete. Your course grade will be computed as a weighted average of those grades as follows:

4  Laboratory Exercises  50% (12.5% per exercise)
1  Midterm Examination  20%
1  Final Examination  30%

Letter grades will be assigned on a 10-point interval scale (A: 100 – 90, B: 89 – 80, C: 79 – 70, D: 69 – 60: F: 59 – 0). The scale may be modified if significant statistical evidence indicates that necessity. Based on previous experience in teaching this course at WSU, such curving is HIGHLY unlikely. If is safest to presume the above grade scale will be used.
IMPORTANT NOTE: Regardless of the numeric value of your composite course score. You MUST achieve a minimum average score of 60% on the four labs and you must have turned in all labs. Students not achieving the lab minimum or failing to turn in even a single lab assignment will fail the course.

Academic Integrity
It is the policy of Wright State University to uphold and support standards of personal honesty and integrity for all students. The formal university code of student academic conduct can be viewed at:

http://www.wright.edu/students/judcial/integrity.html

PLEASE BE FAMILIAR WITH THE ACADEMIC CODE OF CONDUCT. If the instructor detects infractions, he will follow the procedures outlined in the formal university policy. These policies are easily available for review. Therefore, ignorance of them is no defense.

Additional Information

Absences
Class attendance will not be a direct factor in student grades, but will strongly affect the quality of one's class experience. Students are expected to attend every class, as things may make less sense to students that do not attend classes or who arrive late. Students registering after the term begins are responsible for all missed material and should not expect that due dates will be altered for them. If it becomes necessary for you to miss an exam, please contact the instructor as soon as this is known to you (the earlier the better) so that arrangements can be made. If you miss an exam without prior notice to the instructor and wish to make it up at a later date, you will need to present proof of an unavoidable circumstance that caused the absence from the exam.

Office Hours
Office hours are not private lectures. It is expected that students attend and participate in lecture and scheduled lab sessions and use office hours for additional discussion of issues related to class topics. Related topics include clarification of lecture points, remediation advice, or expansion upon ideas discussed in class. You will get the most out of office hour visits by preparing specific questions and/or examples ahead of your visit. Make an attempt to solve problems on your own before coming to office hours even if you don't expect to solve the problem correctly. The instructor may be able to help diagnose problems in understanding or execution - but only if there are concrete examples of your work to examine.

Class Lecture Materials
Copies of the slides used in lecture, supplementary textbooks, and additional course-related information will be available on dropbox links that will be emailed to students as needed. Students can retrieve documents using any standard web browser.

Getting the Most out of the Class
Digital design and analysis is a skill. As with, for example, riding a motorcycle, there is no set of facts one can memorize to ensure success and there is no way to “cram” for examinations of skill and competence. The best, and perhaps only, way of achieving a good result in this class is to challenge yourself with design and analysis problems a little at a time, every day, and well in advance of any formal assessments (i.e. exams). In addition to presenting facts in lectures, we will also present strategies by which you can practice your skills in a self-supporting manner.
**Additional Needs**

Students with disabilities or any additional needs are encouraged to make an appointment with the instructor to discuss any accommodations that may be necessary. We enthusiastically work with the WSU Office of Disability Services (http://www.wright.edu/students/dis_services/) and strongly encourage you to consult with them as well.

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**Topic and Reading Schedule: Valid as of 9/03/11**

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<thead>
<tr>
<th>Week</th>
<th>Topics</th>
<th>Readings</th>
<th>Lab</th>
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<tbody>
<tr>
<td>1</td>
<td>Introduction to digital design, number systems, and gates</td>
<td>1.1-1.6, 2.1</td>
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<tr>
<td>2</td>
<td>Boolean algebra and combinational circuits</td>
<td>2.2-2.3</td>
<td>Lab 0</td>
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<tr>
<td>3</td>
<td>Boolean algebra and Karnaugh maps</td>
<td>2.4</td>
<td>Lab 1</td>
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<tr>
<td>4</td>
<td>Karnaugh maps and logic minimization</td>
<td>2.5</td>
<td>Lab 1</td>
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<tr>
<td>5</td>
<td>Karnaugh maps, circuit design and analysis, Technology Parameters</td>
<td>2.6-2.9, 3.1-3.5, 6.1</td>
<td>Lab 2</td>
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<tr>
<td></td>
<td><strong>MIDTERM EXAM</strong></td>
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<tr>
<td>6</td>
<td>Decoders, encoders, and multiplexers, comparators</td>
<td>3.6-3.9</td>
<td>Lab 2</td>
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<td>7</td>
<td>Comparators, adders, latches, flip-flops</td>
<td>4.1-4.4</td>
<td>Lab 3</td>
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<td>8</td>
<td>Flip-flops, Registers; Sequential Circuit Analysis</td>
<td>5.1-5.3</td>
<td>Lab 3</td>
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<td>9</td>
<td>Sequential Circuit Analysis; Binary arithmetic, adders, subtractors</td>
<td>5.4, 7.1</td>
<td>Lab 4</td>
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<tr>
<td>10</td>
<td>Binary arithmetic, adders, subtractors; Propagation delay; Programmable Logic Array</td>
<td>5.4, 6.2, 6.8</td>
<td>Lab 4</td>
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