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Design of Ultra High Speed Flash Adc, Low Power Folding and Interpolating Adc in CMOS 90nm Technology

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DESIGN OF ULTRA HIGH SPEED FLASH ADC, LOW POWER FOLDING AND INTERPOLATING ADC IN CMOS 90nm TECHNOLOGY

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Engineering

By

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2010
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I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Vinavashree Hiremath ENTITLED Design of Ultra High Speed Flash ADC, Low Power Folding and Interpolating ADC In CMOS 90nm Technology BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Engineering

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Abstract

Hiremath, Vinayashree. M.S.Egr., Department of Electrical Engineering, Wright State University, 2010. Design of Ultra High Speed Flash ADC, Low Power Folding and Interpolating ADC In CMOS 90nm Technology.

In recent years, signal processing has gained ample significance making high speed and low voltage analog-to-digital converters (ADC) inevitable in numerous applications. Two such ADCs designed in CMOS 90nm technology are presented in this thesis.

In flash ADC, thermometer to binary encoder often becomes bottleneck in achieving high speed. An encoder deploying new CMOS logic, with fewer transistors through the use of pseudo-dynamic circuits is described. This 4 bit flash ADC operates at 5GHz with an average power dissipation of 1.3mW.

Folding and interpolation significantly reduces the number of comparators used in flash architecture. A 6 bit 400MSPS low power folding and interpolating ADC that has a power dissipation of 2.17mW is presented. Output synchronization circuit is not required as folding circuits are used in both fine and coarse converters.

These can be used as building blocks in higher resolution pipeline ADC.
# Table of Contents

1. **Introduction** .............................................................................................................................................. 1  
   1.1 Basic ADC concepts and terminology ........................................................................................................ 1  
   1.2 ADC Architecture Overview .......................................................................................................................... 5  
      1.2.1 Flash ADC .............................................................................................................................................. 5  
      1.2.2 Interpolating ADC ................................................................................................................................. 7  
      1.2.3 Folding ADC .......................................................................................................................................... 9  
   1.3 Motivation and objective .............................................................................................................................. 12  

2. **An Ultra High Speed Flash ADC** ................................................................................................................ 13  
   2.1 Design of high speed comparator ................................................................................................................ 13  
   2.2 D-flip flop ................................................................................................................................................... 15  
   2.3 Encoder .................................................................................................................................................... 15  
      2.3.1 Fat tree encoder ...................................................................................................................................... 17  
      2.3.2 Direct conversion encoder using pseudo-dynamic logic gates ......................................................... 18  
   2.4 Simulation of Encoder ................................................................................................................................. 24  
   2.5 Simulation of Flash ADC ............................................................................................................................ 26  

3. **Folding and Interpolating ADC** ................................................................................................................ 30  
   3.1 Concept of folding and interpolation ........................................................................................................... 30  
   3.2 CMOS folding circuit .................................................................................................................................... 32  
   3.3 Interpolation .............................................................................................................................................. 35
3.3.1 Voltage mode interpolation ................................................................. 36
3.3.2 Current mode interpolation ................................................................. 37
3.4 Comparator .............................................................................................. 38
3.5 Cyclic thermometer code to binary encoder .............................................. 38
3.6 Architecture of proposed 6 bit folding and interpolating ADC .................. 39

4. Folding and Interpolating ADC Circuit Design in 90nm CMOS Technology ... 41
4.1 Design of CMOS folding circuit ............................................................... 41
4.2 Resistive interpolation .............................................................................. 46
4.3 Zero Crossing Detector .......................................................................... 48
4.4 XOR based encoder ................................................................................. 50
4.5 Coarse quantizer and bit synchronization ................................................. 53
4.6 Simulation of 6 bit folding and interpolating ADC ..................................... 56
4.7 Transient analysis of 6 bit ADC ............................................................... 58
4.8 Measurement of static characteristics – INL/DNL measurement ............... 60
4.9 Spectral analysis of ADC ....................................................................... 62
4.10 Summary of Folding and Interpolating ADC ............................................. 64

5. Conclusion ................................................................................................ 66

6. Future Work .............................................................................................. 68

7. References ................................................................................................ 69
List of Figures

Figure 1. Sampled signal representation of a sinusoidal signal ............................................. 2
Figure 2. Ideal input-output characteristics of an ADC .......................................................... 3
Figure 3. Block diagram of Flash ADC ..................................................................................... 6
Figure 4. Interpolating ADC with an interpolation factor of four .............................................. 8
Figure 5. Block diagram of folding ADC ................................................................................... 9
Figure 6. Folding characteristics for two bits MSB and N LSB bits ....................................... 10
Figure 7. Schematic of differential comparator ........................................................................ 14
Figure 8. Schematic of D flip-flop ............................................................................................. 15
Figure 9. Block diagram of flash ADC ..................................................................................... 16
Figure 10. Block diagram of direct conversion flash ADC ......................................................... 16
Figure 11. Schematic of Fat tree encoder ................................................................................... 18
Figure 12. Schematic of pseudo-dynamic AND-OR gate ............................................................ 22
Figure 13. Schematic of encoder using pseudo-dynamic CMOS logic gates ......................... 23
Figure 14. Simulation of direct conversion encoder ................................................................. 24
Figure 15. Schematic of 4 bit flash ADC ................................................................................... 26
Figure 16. Input signal of 100MHz overlapped with normalized decimal equivalent of output bits with Fat tree encoder ....................................................................................... 27
Figure 17. Input signal of 100MHz overlapped with normalized decimal equivalent of output bits with new encoder ....................................................................................... 27
Figure 18. Plot of FFT for an input signal of 500MHz, sampled at 5GHz ................................. 28
Figure 19. Architecture of folding ADC ................................................................................... 31
Figure 20. Folding characteristics for N1=2 and N2=4.................................................. 31
Figure 21. Transfer characteristics of the folding circuit .................................................. 33
Figure 22. Schematic of differential pair based folding circuit.......................................... 34
Figure 23. Sinusoidal transfer characteristics of folding circuit ....................................... 35
Figure 24. Intermediate voltage generation circuit ............................................................. 36
Figure 25. Resistive interpolation circuit .......................................................................... 37
Figure 26. Current mode interpolation using current mirrors ............................................. 37
Figure 27. Block diagram of 6 bit folding - interpolating ADC ........................................... 40
Figure 28. Schematic of the cross coupled differential pair based folding circuit .......... 42
Figure 29. Simulation of transfer characteristic of folding circuit ....................................... 43
Figure 30. Output of the folding circuit for a sinusoidal signal ........................................... 44
Figure 31. Simulation of transfer characteristic of folding block ........................................ 44
Figure 32. Schematic of differential resistive interpolation circuit ..................................... 46
Figure 33. Simulation of transfer characteristics of folding and interpolation circuit .... 47
Figure 34. Schematic of the zero crossing detector .............................................................. 48
Figure 35. Transient response of zero crossing detector ...................................................... 49
Figure 36. Schematic of XOR based encoder ..................................................................... 52
Figure 37. Output four LSB bits of fine ADC encoder for a 20MHz signal ...................... 53
Figure 38. Schematic of coarse bit generation circuit ......................................................... 55
Figure 39. Representation of unsynchronized output producing glitches ....................... 56
Figure 40. Top level schematic of folding and interpolating ADC ..................................... 57
Figure 41. Transient response for a 10MHz signal representing six output bits ............. 58
Figure 42. Simulation for 20MHz sinusoidal signal sampled at 400MHz ................. 59
Figure 43. Measure of DNL and INL for 20MHz signal sampled at 400MHz .......... 61
Figure 44. Folding and interpolation ADC FFT results for 20MHz ...................... 63
Figure 45. Plot of SFDR versus input signal frequency .................................. 64
List of Tables

Table 1 Classification of ADC architecture .......................................................... 5
Table 2 Design specifications of flash ADC ............................................................ 13
Table 3 Truth Table for Direct Conversion Encoder .............................................. 19
Table 4 Comparison of Fat Tree Encoder with Pseudo Dynamic based Encoder .... 25
Table 5 Performance summary of Flash ADC ......................................................... 29
Table 6 Reference voltage versus the folder block ................................................. 45
Table 7 Truth table of XOR based encoder .............................................................. 51
Table 8 Performance summary of Folding and Interpolating ADC ...................... 65
Table 9 State of the art 6 bit CMOS folding and interpolating ADCs ................. 65
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1. Introduction

Signal processing is very important in many of the system on-a-chip applications. With the advancement in technology, digital signal processing has gained significant importance in the field of telecommunication, biomedical, control systems and so on. This has necessitated the need for design of high precision data converters thereby attracting immense research in this field.

Analog to digital converters (ADCs) is a mixed signal device that converts analog signals which are real world signals to digital signals for processing the information. In the recent years, the need to design a low voltage, low power, high speed and wide bandwidth analog-to-digital converter has increased tremendously. Therefore the focus of this research is to design efficient low voltage ADCs that operate at high speed.

1.1 Basic ADC concepts and terminology

Fundamentally analog to digital conversion involves sampling the analog signal and processing the sampled signal to generate the digital output bits. The rate at which the input signal is converted to its digital form determines the conversion speed and the number of output bits represents the resolution of the ADC. Some of the basic concepts of ADC are explained below.

1. Input Signal Bandwidth

The frequency range of the input signal which can pass through the analog front end circuitry with minimal amplitude loss is called the bandwidth of input signal. For a sinusoidal signal, it is referred to as the frequency at which the amplitude is reduced by 70.7 % of original amplitude.
2. Sample Rate

The first step towards conversion of analog to digital is sampling. Sample rate or sampling frequency is defined as the number of samples of the input signal taken per second. According to the Nyquist theorem, for any band limited signal with maximum frequency $F_{\text{max}}$, the sampling frequency must be at least equal to or greater than twice $F_{\text{max}}$ in order to reconstruct the signal properly. This implies that if the sampling frequency is less than twice $F_{\text{max}}$, the signal cannot be reconstructed perfectly and higher the number of samples better would be its reconstruction. This concept is depicted in figure 1.

![Sampled signal representation of a sinusoidal signal](image)

Figure 1. Sampled signal representation of a sinusoidal signal
3. Resolution

The smallest amplitude change in the input signal that can be distinguished by an ADC is called resolution. This can be expressed in terms of full scale voltage of input, but is typically represented as the number of bits used to represent the output digital signal. Higher the number of output bits better is the resolution. For instance, a 4 bit ADC divides the input signal into sixteen levels while a 6 bit ADC divides the signal into sixty four steps consequently giving better resolution. The size of each step which is equal to LSB bit voltage is given by \( \frac{FSR}{2^N} \) where FSR is the full scale range of the input.

4. Quantization Error

While converting the analog signal to digital or in other words digitizing the analog signal, with a finite resolution ADC there exists a certain amount of uncertainty termed as quantization error or quantization noise. It is the difference between actual analog signal value and its quantized digital value. The ideal input-output characteristics of an ADC are shown in figure 2.

![Ideal input-output characteristics of an ADC](image)

Figure 2. **Ideal input-output characteristics of an ADC**
5. Signal to Noise Ratio (SNR)

By definition, SNR is the ratio of full scale value to the rms value of the quantization noise. The rms value is the root of mean of square of quantization noise. It is the measure of signal power relative to the noise power.

\[
\text{SNR} = 10 \log\left( \frac{P_{\text{signal}}}{P_{\text{noise}}} \right)
\]  

(1)

6. Effective Number of Bits (ENOB)

ENOB is a measure of actual performance of an ADC, which gives the conversion bit of an ADC. ENOB is computed as shown below

\[
\text{ENOB} = \frac{\text{SNR}-1.76}{6.02}
\]

(2)

7. Spur-Free Dynamic Range (SFDR)

SFDR is the ratio of the strength of the fundamental frequency to the strongest spurious signal in the output. It is an indicator of fidelity of an ADC. Non-linearity in the ADC generates spurious signals that affect the achievable SFDR. SFDR can be calculated using the below formula

\[
\text{SFDR} = \text{Signal (dB)} - \text{largest spur (dB)}
\]

(3)

8. Differential non-linearity (DNL)

DNL is a measure of separation between adjacent levels measured at vertical jump. DNL measures any deviation from one LSB.

9. Integral non-linearity (INL)

INL is the maximum difference between actual finite resolution characteristic and ideal finite resolution characteristics.
1.2 ADC Architecture Overview

There are several different types of ADCs available, depending on the type of application. They are usually classified into three main categories depending on their speed of operation. The three types of ADCs are low speed serial ADC, medium speed ADC and high speed ADC. Typically the serial ADCs have very high resolution which means they support high accuracy whereas high speed ADCs operate at very high frequencies but have relatively low resolution.

<table>
<thead>
<tr>
<th>Conversion Rate</th>
<th>Resolution</th>
<th>ADC Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slow</td>
<td>&gt;14 bits</td>
<td>Integrating Oversampling</td>
</tr>
<tr>
<td>Medium</td>
<td>&gt;10 bits</td>
<td>Successive approximation</td>
</tr>
<tr>
<td>Fast</td>
<td>&gt;6 bits</td>
<td>Flash Pipeline Folding and Interpolating</td>
</tr>
</tbody>
</table>

Table 1 Classification of ADC architecture

In the following section only the high speed ADC architecture is described excluding the pipeline architecture.

1.2.1 Flash ADC

Many applications require high speed ADCs with a conversion speed of one clock cycle. Of many analog-to-digital converters, flash ADC, also known as parallel ADC, holds its importance because of high speed operation. The conversion speed in flash ADC is only one clock cycle and hence is the fastest ADC architecture available and is limited only by comparator and gate propagation delays. The concept of flash ADC is straight forward. It
basically compares the analog input to a set of reference voltages and determines the threshold to which the input lies closest.

The block diagram of a typical flash ADC is as shown in Figure 3.

Figure 3. **Block diagram of Flash ADC**

In general, an N bit flash ADC consists of a resistor string, a set of comparators and a digital encoding network. The resistor string is composed of \(2^N\) resistors which are
connected between Ref+ and Ref- to produce unique reference voltage for each of the comparators as shown in figure 3. The voltage difference between these reference voltages is equal to the least significant bit (LSB) voltage. The $2^{N-1}$ comparators produce the thermometer code (TC), it is called thermometer code because as the amplitude of the analog input increases the number of ones in the output increases linearly which is similar to the mercury rise in the thermometer, and the digital encoding network converts $2^{N-1}$ inputs to N bit binary code (BC). The digital encoding network comprises 1-out-of-N code generator circuit for intermediate conversion, which is usually implemented using XOR gates or ‘01’ generator circuits, and $2^{N}$ to N bit encoder.

For example, a four bit flash ADC consists of sixteen resistors generating fifteen different reference voltages for comparators. The comparators generate a fifteen bit thermometer code, which is encoded to four bits digital output using an encoder.

The main disadvantage of the high speed architectures is that they compromise speed with area and so does the flash ADC. Unfortunately, it is the most component-intensive ADC architecture for any given number of output bits. With each additional output bit, the number of required comparators doubles. The increased transistor count increases power dissipation. This also results in significant capacitive loading and large die size which directly affects cost.

1.2.2 Interpolating ADC

The main disadvantage of flash ADC is the usage of larger number of comparators and resistors. While comparators increase input capacitance, mismatch in the resistors results in inconsistency in the output. As an improvement, interpolation is used to reduce the
number of comparators and resistors that are used to generate the reference voltage. The figure 4 shows the 4-bit interpolating ADC using an interpolation factor of four.

Interpolation can be done using resistors, current mirrors or capacitors which are respectively called voltage interpolation, current interpolation and charge interpolation. While voltage interpolation technique suffers from delay variation problem due to different resistance and the current interpolation proves to be power hungry, the charge interpolation tends to slow down the circuit due to increased capacitance. Hence the choice of type of interpolation depends mainly on the design requirement.

![Interpolating ADC with an interpolation factor of four](image)

**Figure 4.** Interpolating ADC with an interpolation factor of four
Interpolation technique provides less input capacitance along with simplified design of the comparator. Hence interpolating ADCs are faster and have higher input signal bandwidth.

1.2.3 Folding ADC

Interpolation ADC has same number of comparators as flash ADC which is almost equal to $2^N$. The number of comparators can be reduced below $2^N$ by the use of folding ADC architecture. The architecture of the folding ADC is as shown in the figure 5. This ADC is a two-stage converter where the MSB and LSB bits are generated separately but simultaneously in two different modules.

![Block diagram of folding ADC](image)

Figure 5. **Block diagram of folding ADC**

The total resolution of this ADC is $N = N_{MSB} + N_{LSB}$, where $N_{MSB}$ are bits resolved in coarse converter and $N_{LSB}$ are bits resolved in fine converter. The analog preprocessing consists of the folding circuits, which fold the input signal through several differential amplifiers. The operation of the folding circuit can be explained by its transfer characteristics as depicted in figure 6.
Assuming the circuit is a four times folder circuit, the entire input signal range gets divided into four sub regions each with a voltage range of one fourth the input signal range. This range is divided into $2^{N_{LSB}}$ levels to generate $N_{LSB}$ bits. Simultaneously, the four subranges are encoded as two MSB bits.

Figure 6. **Folding characteristics for two bits MSB and N LSB bits**

By combining the features of folding and interpolating ADC evolved a new architecture named as “Folding and interpolation ADC” which is a moderate resolution, low power ADC. Clearly, the number of comparators required in this design is significantly less when compared to that of flash ADC. The significant reduction in the number of comparators implies much less power dissipation. Besides saving power and die area, the
folding and interpolating ADC offers unit step conversion. The throughput of this architecture is same as that of flash ADC, the analog input is converted to its corresponding binary output in one clock cycle. In addition, this eliminates the need of sample and hold circuit because of one step conversion process.

This ADC architecture has some inherent problems such as timing misalignment between the coarse and fine ADC plus the limitation on the input signal bandwidth. As the folder circuit multiplies the input signal by folding factor, the internal operating frequency is much higher than the input signal. However, this ADC architecture can be designed to offer high resolution, and high speeds using some techniques.

To summarize, the folding circuit reduces the number of comparators significantly when compared to that in flash ADC. Interpolation can be used to generate additional folding waveforms. Hence the combination of folding and interpolation proves beneficial in the design of low power, high speed ADC.
1.3 Motivation and objective

In the last few decades the field of communication has evolved dramatically leading to the development of many low cost integrated circuits of which ADCs are inevitable. The need to design a low cost, low power and high speed ADC is ever increasing. The quest to build a high speed ADC has led to many innovative designs. The motivation of this thesis is to design a low voltage, low cost ADC that operates at high frequencies. In this thesis, two different ADC architectures are studied, designed and implemented in CMOS 90nm technology of which one is a low resolution ADC the other is a moderate resolution ADC.

The first ADC is the flash ADC, designed to operate at 5GHz over a bandwidth of 500MHz. The main focus of this research has been study of different encoders that can be used in flash ADCs. In this report a new encoder designed has been proposed that operates at very high speed compared to the traditional encoders.

Moderate resolution ADC with high speed and low power are used in numerous applications. There is an ever increasing demand for the low voltage ADC in embedded applications. This led to the design of a very interesting ADC architecture which is folding and interpolating ADC. Additionally, synchronization of all bits in folding and interpolation ADC is challenging. Hence, the goal is to design a well synchronized 6 bit ADC with minimal circuitry. In this thesis, design of low power folding and interpolation ADC that can operate at sampling rate of 400MSPS using few components is presented.
2. An Ultra High Speed Flash ADC

Flash ADC is being used in many applications where speed of operation is very high. In this chapter design of flash ADC which operates at 5GHz is discussed. The initial requirements of ADC are as follows.

<table>
<thead>
<tr>
<th>Table 2 Design specifications of flash ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
</tr>
<tr>
<td>Architecture</td>
</tr>
<tr>
<td>Supply voltage</td>
</tr>
<tr>
<td>Number of output bits</td>
</tr>
<tr>
<td>Input dynamic range</td>
</tr>
<tr>
<td>Resolution</td>
</tr>
<tr>
<td>Bandwidth</td>
</tr>
<tr>
<td>Sampling frequency</td>
</tr>
</tbody>
</table>

2.1 Design of high speed comparator

Comparator is the basic building block of flash ADC as it determines the speed and accuracy of ADC. For a four bit flash ADC, fifteen comparators which operate at different threshold voltages are designed. The performance of flash ADC depends on its ability to sample the input without jitter [1]. Therefore, clocked comparators consisting of a differential amplifier and a latch are used in this design. The clock signal given to the latch is same as the sampling clock of flash ADC.
Figure 7. **Schematic of differential comparator**

The comparator generates a high whenever the input voltage exceeds the reference voltage. Thereby, this acts as one bit ADC. The bias voltage and the width of transistors must be chosen carefully to ensure all transistors are in saturation. The latch also ensures that the output of all comparators arrive at the same time at the input of encoder. Therefore, the outputs from comparators are in synchronization with the sampling clock.

The output of fifteen comparators is in the form of thermometer code. This has to be converted into four bit binary using a digital encoder. There are several designs available for the encoder like ROM [2], PLA etc. The design and implementation of Fat tree encoder and the encoder designed using pseudo dynamic CMOS logic is furnished in the following pages.
2.2 D-flip flop

The design of D-latch is vital as it is used in the back end of clocked comparator. Here a very high speed and low jitter D flip-flop (DFF) is designed as shown in figure 8. This design makes use of only nine transistors thereby reducing the capacitance at the comparator output [3]. To achieve high speed, these transistors are designed with minimum channel length and are of minimum size. This design can operate up to 10GHz.

![Schematic of D flip-flop](image)

Figure 8. **Schematic of D flip-flop**

The input pin ‘Clk’ is connected with the sampling clock of the ADC while pin ‘In’ is connected to comparator outputs. By using the DFF, the output of all fifteen comparators get synchronized with the clock.

2.3 Encoder

Typical flash ADC block diagram is as shown in the figure 9. It consists of a set of comparators in the front end, followed by the thermometer code to 1-out-of-N code converter which is usually implemented using XOR gates and the encoder. Design of
each of these blocks is critical in achieving high speed. A special focus is given to the
design of encoder in this report.

The usual implementation of encoder has been ROM / PLA circuits, XOR encoder and
Wallace tree encoder. From the earlier study [4], it is evident that a Fat-tree encoder
outperforms the traditional ROM encoder. Yet, there is a scope to improve the
performance of this encoder. Here a new encoder is designed which is faster than the Fat
tree encoder. The main advantage of the proposed encoder is its direct conversion from
TC to BC as in figure 10. There is no need to convert thermometer code to one-out-of-N
code. This technique significantly reduces the number of logic gates, thereby increasing
the speed. Hence, this design becomes more suitable for high speed flash ADCs.

In this section the following two different encoder designs are discussed.
1. Fat tree encoder

2. Direct conversion encoder using pseudo-dynamic logic gates

2.3.1 Fat tree encoder

Fat tree encoder is the popular architecture that is being used in many flash ADC designs. This type of encoder requires intermediate conversion which converts the thermometer code to one-out-of-N code. It is implemented using optimized ‘01’ generator circuit [5]. The one-out-of-N code is then encoded to binary using Fat tree encoder, which consists of multiple branches of OR gates. As the number of input bits increases, the tree becomes larger. Suppose the ‘01’ generator has a delay d1 and the encoder has a delay d2 (equal to at least 3 OR gate delays for 4 bit flash ADC) then overall delay is approximately d1+d2. At times, this becomes the limiting factor for sampling frequency in the range of several GHz. Further, to improve the performance of Fat tree encoder, the OR gates are replaced with NAND and NOR logic gates using DeMorgan’s theorem.

This inverting logic Fat tree encoder circuit was designed and simulated using CMOS 90nm technology. The schematic of Fat tree encoder is shown in figure 11. The signals I0-I15 are inputs to the encoder; while a, b, c and d are intermediate signals as seen in the schematic below. The following equations define the output bits of the Fat tree encoder.

\[
\begin{align*}
\text{Bit0} &= a_0 + a_1 + a_2 + a_3 + a_4 + a_5 + a_6 + a_7 \\
\text{Bit1} &= b_0 + b_1 + b_2 + b_3 \\
\text{Bit2} &= c_0 + c_1 \\
\text{Bit3} &= d_1
\end{align*}
\] (4)
The worst case delay was measured to be equal to 0.3 ns. So, this circuit could not be used for flash ADC with 5 GHz sampling rate, as the clock period is only 0.2 ns. This limitation of Fat tree encoder led to the design of new encoder.

2.3.2 Direct conversion encoder using pseudo-dynamic logic gates

This design makes use of only the AND-OR logic gates, similar to PLA design. But the difference is that, in PLA design all the inputs are combined to generate an output bit.
While in this design only selected input combinations are used to derive an output. The main feature of this encoder is that, the thermometer code is converted to binary code without any intermediate conversion. For a four bit ADC, the equations for output binary bits are as shown below.

\[
\begin{align*}
\text{Bit}0 &= 10*\overline{I1} + 12*\overline{I3} + 14*\overline{I5} + 16*\overline{I7} + 18*\overline{I9} + 110*\overline{I11} + 112*\overline{I13} + 114 \\
\text{Bit}1 &= 11*\overline{I3} + 15*\overline{I7} + 19*\overline{I11} + 113 \\
\text{Bit}2 &= 13*\overline{I7} + 111 \\
\text{Bit}3 &= 17
\end{align*}
\]  

(5)

where \(I_n\) stands for \(n^{th}\) bit of thermometer code. The truth table for direct conversion encoder is shown in Table 3.

**Table 3 Truth Table for Direct Conversion Encoder**

<table>
<thead>
<tr>
<th>TC input I14 to I0</th>
<th>Encoder Output Bit3 to Bit0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000000000000000</td>
<td>0000</td>
</tr>
<tr>
<td>0000000000000001</td>
<td>0001</td>
</tr>
<tr>
<td>0000000000000011</td>
<td>0010</td>
</tr>
<tr>
<td>0000000000000011</td>
<td>0011</td>
</tr>
<tr>
<td>0000000000000111</td>
<td>0100</td>
</tr>
<tr>
<td>0000000000000111</td>
<td>0101</td>
</tr>
<tr>
<td>0000000000001111</td>
<td>0110</td>
</tr>
<tr>
<td>0000000000011111</td>
<td>0111</td>
</tr>
<tr>
<td>0000000000111111</td>
<td>1000</td>
</tr>
<tr>
<td>0000000001111111</td>
<td>1001</td>
</tr>
<tr>
<td>0000000111111111</td>
<td>1010</td>
</tr>
<tr>
<td>0000001111111111</td>
<td>1011</td>
</tr>
<tr>
<td>0000011111111111</td>
<td>1100</td>
</tr>
<tr>
<td>0000111111111111</td>
<td>1101</td>
</tr>
<tr>
<td>0011111111111111</td>
<td>1110</td>
</tr>
<tr>
<td>1111111111111111</td>
<td>1111</td>
</tr>
</tbody>
</table>
As seen from the equation (5), the output bits are derived directly from output of comparator or the thermometer code. Hence, this eliminates the need for ‘01’ generator circuit thereby reducing the delay of the encoder to some extent. The equations for this encoder were derived from truth table. For instance, output Bit3 is equated to input bit I7 as they have same entries in the truth table. So instead of processing the inputs to derive this output, it can directly be connected to I7. Similarly, other equations are derived using the bit patterns.

Clearly, these equations are realized using less number of gates compared to Fat tree encoder. It can be designed using static CMOS logic, pseudo NMOS logic or dynamic CMOS logic. Static CMOS logic gates have less power dissipation but cannot achieve greater speed. While dynamic CMOS logic gates have higher power dissipation but can achieve very high speed. Here, the design is implemented using a new CMOS logic called pseudo-dynamic CMOS logic.

The pseudo-dynamic CMOS circuit consists of a PMOS transistor, a bunch of NMOS transistors and an inverter. The PMOS transistor is used to pre-charge the output node and the NMOS logic is used to selectively discharge the output node. Unlike dynamic CMOS logic, there is no need for an NMOS evaluation transistor in series with NMOS logic block because the inputs to this circuit are the outputs of clocked comparators of flash ADC, which latch the output till next rising edge of clock.

For the dynamic CMOS logic to work properly it is of paramount importance that the NMOS evaluation logic is not enabled during the precharge phase. Whereas in pseudo-dynamic CMOS logic, the NMOS evaluation logic can be enabled during precharge phase as it has no influence on the output voltage due to the of the presence of inverter
i.e. during precharge phase, if NMOS logic is enabled the output settles to an intermediate voltage determined by a resistive divider of the pull-up and NMOS logic networks. It must be ensured that the voltage at inverter input does not exceed VIH (i.e. maximum voltage on the input that is considered as logic zero by the inverter). To accomplish this, the size of PMOS and NMOS transistors must be chosen carefully otherwise this leads to improper function of the logic circuit. For instance, consider the case where the NMOS logic is enabled and the clock is low. With proper sizes for the transistors, the voltage at the input of inverter will be less than VIH thus setting a high at the output of inverter. Suppose the PMOS transistor size is increased beyond the optimal value, then the intermediate voltage exceeds VIH thereby pulling down the inverter output. Therefore transistor sizing is vital in this design.

The only disadvantage with this CMOS logic is that it has non-zero static power dissipation caused by the current through PMOS and NMOS pull-down network when the clock goes low.

The schematic of an AND-OR gate implemented using pseudo-dynamic CMOS logic is shown in figure 12. It consists of a PMOS transistor driven by a clock signal and a NMOS transistor block defining the logic function. In NMOS evaluation logic the inputs to be ORed are connected in parallel branches and to AND it is connected in series.
The new encoder design implemented using pseudo-dynamic CMOS OR gates is shown in figure 13. Bit0, Bit1 and Bit2 generation circuits are shown in sub-figure (a), (b) and (c) respectively.

(a) Bit 0 generation circuit
Figure 13. **Schematic of encoder using pseudo-dynamic CMOS logic gates**

It must be noted that the PMOS transistor is driven by the same clock that is used to sample the analog input in flash ADC. As seen from the schematic, this design consists of
only three multiple input pseudo-dynamic OR gates. The complete design makes use of only 48 transistors thereby reducing delay and cost of the encoder.

2.4 Simulation of Encoder

The encoder was tested using all the input combinations from the truth table and worst case delay was measured. As the 15 bits input vary from zero to all ones, the output bits vary from 0000 to 1111 as shown in figure 14. The top signal is the clock and the bottom signals are the four output signals of the ADC. To simulate the encoder a D flip-flop was connected at each output of the encoder instead of a capacitor. Consequently, the capacitance of D flip-flop formed by the gate capacitances of input transistors acts as load to the circuit. In addition, all the outputs are synchronized to the clock and hence provide better digital output.

![Simulation of direct conversion encoder](image)

Figure 14. Simulation of direct conversion encoder
The summary and comparison of two encoder simulation results is shown in Table 3. The number of transistors in inverting logic Fat tree encoder is 128 where as the new design can be implemented using only 48 transistors. The maximum sampling frequency that can be achieved using Fat tree encoder is 2.38GHz and with new design it can go beyond 5GHz. The delay has reduced from 0.3ns to 0.08ns thereby enabling sampling frequency of 5GHz. At 2GHz, the average power dissipation of Fat tree encoder was 91.2μW and the new design consumes 142.4μW. At 5GHz, the average power dissipation was 131.6μW and 184.8μW respectively.

Table 4 Comparison of Fat Tree Encoder with Pseudo Dynamic based Encoder

<table>
<thead>
<tr>
<th>CMOS 90nM Technology</th>
<th>Fat tree encoder</th>
<th>New design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuit logic</td>
<td>Static CMOS</td>
<td>Pseudo-dynamic CMOS</td>
</tr>
<tr>
<td>Worst case delay</td>
<td>0.3ns</td>
<td>0.08ns</td>
</tr>
<tr>
<td>No of transistors</td>
<td>128</td>
<td>48</td>
</tr>
<tr>
<td>Max sampling frequency</td>
<td>2.38 GHz</td>
<td>5 GHz</td>
</tr>
<tr>
<td>Power dissipation at 2GHz</td>
<td>91.2 μW</td>
<td>142.4 μW</td>
</tr>
<tr>
<td>Power dissipation at 5GHz†</td>
<td>131.6 μW</td>
<td>184.8 μW</td>
</tr>
</tbody>
</table>

†Value not applicable for Fat tree encoder as it cannot operate at 5GHz.

The results clearly show that the new design is almost two times faster than Fat tree encoder. The cost of the encoder also reduces due to decrease in the number of transistors. If this encoder has to be used in other applications where the inputs are not clocked, then NMOS evaluation transistor has to be used.
2.5 Simulation of Flash ADC

To verify the performance of the encoder, two 4 bit flash ADCs consisting of sixteen resistors, fifteen comparators and the encoder are designed in CMOS 90nm technology. The schematic of the flash ADC is as shown in the figure 15. Here silicon resistors, which are a three terminal resistor, are used to generate the reference voltages. The comparator output is pipelined and fed to the digital encoder for better synchronization. The four output binary bits are latched using DFF.

Figure 15. Schematic of 4 bit flash ADC

The comparison of ADC with two encoders is done by sampling a sinusoidal input signal of 0.6V peak-to-peak amplitude, 100MHz frequency at a rate of 5GHZ. The simulation of
flash ADC with Fat tree encoder is in figure 16. The simulation of flash ADC with pseudo-dynamic CMOS logic gates is as shown in figure 17.

Figure 16. Input signal of 100MHz overlapped with normalized decimal equivalent of output bits with Fat tree encoder

Figure 17. Input signal of 100MHz overlapped with normalized decimal equivalent of output bits with new encoder
As seen from these plots, the ADC with new encoder has better output when compared to ADC with fat tree encoder. As the Fat tree encoder has a delay of 0.3ns, it cannot catch up with the sampling clock of 0.2ns, which ultimately leads to more errors in the output of ADC as seen in figure 16. While the new encoder, with pseudo-dynamic CMOS logic gates, has a delay of 0.08ns and can easily convert the inputs changing every 0.2ns. For this reason the output bits vary more linearly in ADC with pseudo-dynamic CMOS logic gates than with Fat tree encoder.

Fast Fourier transform (FFT) test is used to measure the dynamic parameters of the flash ADC. This analysis is performed on the ADC with new encoder designed using pseudo-dynamic CMOS logic gates. The FFT analysis for an input frequency of 500 MHz is shown in figure 18. The FFT test exhibits harmonics below the fundamental frequency. The maximal spurious free dynamic range for 500MHz is 38.08 dB. By using differential comparators, even harmonics can be suppressed and hence a higher SFDR can be achieved.

![FFT plot](image)

Figure 18.   **Plot of FFT for an input signal of 500MHz, sampled at 5GHz**
# Table 5 Performance summary of Flash ADC

<table>
<thead>
<tr>
<th>Technology</th>
<th>CMOS 90nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture</td>
<td>Flash ADC</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.2V</td>
</tr>
<tr>
<td>Number of output bits</td>
<td>4</td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>5GHz</td>
</tr>
<tr>
<td>Input dynamic range</td>
<td>0.3≤Vin≤0.9V</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>500MHz</td>
</tr>
<tr>
<td>Resolution</td>
<td>37.5mV</td>
</tr>
<tr>
<td>Vref</td>
<td>0.3375 – 0.8625V</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>1.3mW</td>
</tr>
</tbody>
</table>
3. Folding and Interpolating ADC

In recent decades, the need for compact circuit designs has increased tremendously thereby leading to downscaling of technology. In addition the feature size in CMOS technology is becoming very small resulting in increased system integration. Together with this, the supply voltage is going low and hence this necessitates the design of low power, low cost, small die sized ADC which leads to design of folding and interpolating ADC.

As explained in the earlier section, flash ADC converts the analog signal into digital by comparing it with a set of reference voltages. As the number of output bits increases, the circuit becomes bigger and the complexity of the layout increases hence this architecture becomes impractical when higher resolution is required. Folding is a technique which reduces the number of comparators significantly by means of analog preprocessing circuit. This concept was introduced by Arbel and Kruz in 1975 [6] and is proved to be efficient for moderate resolution and high speed ADC applications. Initially folding ADCs were realized in bipolar technologies, but now it is implemented in both CMOS and BiCMOS technologies.

3.1 Concept of folding and interpolation

Similar to a multi-step converter, in folding and interpolating ADC the conversion is done in two steps which comprise a coarse conversion and a fine conversion unit. Both blocks utilize lower resolution ADC to implement a higher resolution ADC. Coarse ADC converts the analog input to MSB bits and the LSB bits are generated using fine ADC. The analog preprocessing circuit converts a full scale range and divides it into subranges,
the number of subranges is defined as folding factor. Fine ADC converts this subrange into LSB bits. Suppose there are N1 MSB bits and N2 LSB bits then the first stage which is the coarse quantizer quantizes the input signal into $2^{N_1}$ binary combinations. The second stage generates the LSB bits through the use of analog preprocessing blocks. Folding circuits designed using coupled differential pair (CDP) constitutes the core of preprocessing block. The folding circuit maps $2^{N_1}$ sub ranges onto a single range. This is applied as input to the fine quantizer which is further quantized into $2^{N_2}$ values. The architecture and characteristics of folding circuit are shown in figure 19 and 20 respectively.

![Architecture of folding ADC](image1.png)

**Figure 19.** Architecture of folding ADC

![Folding characteristics for N1=2 and N2=4](image2.png)

**Figure 20.** Folding characteristics for N1=2 and N2=4
Folding reduces the number of comparator required and hence simplifies encoding as well as reduces the power consumption and area [7]. For example, a 5 bit flash ADC utilizes 31 comparators and by employing folding circuit with 2X folding, the number of comparators can be reduced from 31 to 16. In general, the analog preprocessing block with N times folding reduces the number of comparators by a factor of N.

Deciding on the folding factor (FF) is vital. Higher folding factor requires less number of comparators. On the other hand, as folder bandwidth is inversely proportional to folding factor, higher folding factor results in lower bandwidth. Also the relationship between ADC full swing voltage (VFS) and difference between successive reference voltages (ΔVref) should satisfy.

\[ VFS = FF \times ΔVref \] (6)

This equation also implies that the folding factor cannot be too high as it reduces the gate source voltage, thereby limiting the flexibility of this architecture.

The total number of folding circuits, comparators and encoder depends on the folding factor, number of folding blocks and interpolation factor. There are several combinations possible for 6 bit FIADC such as 3 coarse bits, 3 fine bits; 2 coarse bits, 4 fine bits and 1 coarse bit, 5 fine bits. It is observed that 2/4 ADC is the smallest architecture of 6 bit folding and interpolation ADC and this is implemented in the current design.

### 3.2 CMOS folding circuit

Earlier the folding technique was used as Gilbert sine wave generator [8]. Later the application of folding circuit was extended to the design of ADC as well. Basically the circuit folds the input signal by a factor of FF. An ideal circuit generates sawtooth
transfer characteristics but as it has infinite slew rate at the discontinuity, the triangular characteristics is preferred. However, it is complicated to implement circuits with piecewise linear characteristics because of abrupt discontinuity. The practical folding circuit characteristic is called “pseudo-sinusoidal” characteristics and is easier to implement. The three different types of folding characteristics are shown in figure 21.

Figure 21. Transfer characteristics of the folding circuit
The basic folding circuit is as shown in the figure 22. The folding circuit consists of cross-coupled differential amplifier i.e. the output of odd and even numbered differential pairs are cross-coupled. The inputs of the differential pairs are connected to converter input voltage and the reference voltages are generated by the resistor ladder. The number of folds depends on the number of differential amplifiers.

![Schematic of differential pair based folding circuit](image)

Figure 22. **Schematic of differential pair based folding circuit**

The output of folder circuit is differential with high common mode voltage and nominal differential voltage. The DC transfer curve of the folder circuit is as shown in figure 23. As the input is swept from 0 to Vmax i.e. maximum input voltage, accordingly the output changes in a sinusoidal manner. The differential output has zero crossing points defined by reference voltages and are independent of process and temperature variations because of differential form.
As seen from the schematic, there are odd numbers of differential pairs in a folding circuit. In order to obtain a sinusoidal curve the reference voltages must be uniformly spaced, as well as high enough to operate transistors in saturation. Although the folding operation reduces number of comparators significantly, it has a disadvantage of bandwidth limitation. The reason is that folding operation effectively increases the output frequency [9] as given in the below equation

\[ F_{\text{out}} = \sqrt{2} \cdot FF \cdot F_{\text{in}} \]  \hspace{1cm} (7)

Where \( F_{\text{out}} \) is the output frequency of the folding circuit, \( FF \) is the folding factor and \( F_{\text{in}} \) is the input frequency. Hence, there exists a severe limitation on the bandwidth of folding ADC.

3.3 Interpolation

Mathematically, interpolation is a technique of constructing new points within the range of a known set of points. As sixteen signals are required to generate four LSB bits, solely using folding circuit to generate these signals leads to a large circuit and thereby increases the cost and area. Hence interpolation circuits are used to generate the required
number of folding signals. The basic principle of interpolation is shown in figure 24. Folder circuits 1, 2 generate two fold signals $V_1$ and $V_2$ respectively. Another folding signal that lies in between $V_1$ and $V_2$ is generated using the resistor divider network. Clearly the middle voltage $V_M$ is given by equation (8), hence the intermediate voltage is derived.

$$V_M = \frac{1}{2} (V_1 + V_2) \tag{8}$$

![Diagram](image)

Figure 24. **Intermediate voltage generation circuit**

There are essentially two techniques used to interpolate the folding signals specifically voltage mode interpolation and current mode interpolation, which are described in the following section.

### 3.3.1 Voltage mode interpolation

The voltage mode interpolation is implemented using a string of resistors [10] as shown in below figure 25. This type of interpolation is also called passive interpolation. This is an uncomplicated design. However, the value of the resistors must be chosen very carefully for the reason that, if a low value resistor is used, it reduces the voltage gain of the folding circuit and if it is a high value resistor then it consumes a lot of power and also requires larger chip area. This design suffers from the problem of delay variation
which is for the reason that different RC constants are formed by different taps on interpolation resistor and the input capacitance of comparator.

Figure 25.  **Resistive interpolation circuit**

### 3.3.2 Current mode interpolation

The current mode interpolation is implemented using current dividers [13], [14]. The current mirror circuits are used to interpolate currents $I_a$ and $I_b$, referring to figure 26. This type of interpolation is also called active interpolation. Although current mode interpolation does not have delay mismatch problem, power dissipation is very high when compared to voltage mode interpolation. Hence it is not suitable for low power applications.

Figure 26.  **Current mode interpolation using current mirrors**
3.4 Comparator

The design of comparator is uncomplicated in case of folding and interpolating ADC because of the differential output characteristics. Unlike comparing the input signal with a fixed reference voltage, here the comparator compares the differential pair signals i.e. output of the folder circuit. This eliminates the need to design many different comparators like in flash ADC. This also has the advantage of high scalability. If the dynamic range of the input signal is changed, then a whole new set of comparators would have to be redesigned in case of flash ADC but in folding and interpolating ADC, the comparator is independent of the input dynamic range and can be used in other resolution or configuration of folding and interpolating ADC. Evocatively these comparators are more often termed as zero crossing detectors.

As the folding circuit behaves as a frequency multiplier, the output is a high frequency signal and hence it changes very fast compared to the input signal. Consequently, the zero crossing detectors must be very fast. In addition the absence of track and hold circuit makes this component design vital.

3.5 Cyclic thermometer code to binary encoder

In order to generate all the output bits, two encoders are required for coarse ADC and fine ADC respectively. Although these encoders operate independently, a synchronization signal is used from the fine ADC to align MSB bits with the LSB bits. Unlike the signals in flash ADC, the input to encoder in fine ADC is not in the form of thermometer code because of the folding circuit. Here the signals are of type cyclic thermometer code hence the encoder design becomes very challenging. However, the XOR based encoders can be used to generate the LSB bits.
3.6 Architecture of proposed 6 bit folding and interpolating ADC

The block diagram of the designed 6 bit folding and interpolation ADC is as shown in figure 27. It consists of analog preprocessing circuit in the form of folding circuit, interpolating block, zero crossing detectors, encoder and the coarse ADC unit. A folding circuit with folding factor of four is used as the building block of the fine ADC. Five such folding circuits are required to cover the entire dynamic range of the input signal. Adjacent folding signals are interpolated using 4X resistive interpolation. Consequently sixteen folding signals are generated which are connected to a set of zero crossing detectors to generate the sixteen bit cyclic thermometer code. The encoder converts the cyclic thermometer code to 4 bits which are the LSB bits for this ADC. The coarse bits are generated independently in different module.

Although an independent two bit flash ADC could be used, here folding circuit is used to avoid additional circuitry and to achieve better synchronization. The MSB bit is generated using a folding circuit with folding factor of two and MSB-1 bit is derived from the fine which also serves as bit synchronization signal from fine ADC. Hence, this circuit is optimized in terms of number of components, thereby leading to lesser power dissipation.
Figure 27. **Block diagram of 6 bit folding-interpolating ADC**
4. Folding and Interpolating ADC Circuit Design in 90nm CMOS Technology

A 6 bit folding and interpolating ADC is designed using CMOS 90nm technology and the schematic is captured in Cadence. Basically it consists of design of two independent modules namely fine ADC and coarse ADC.

A detailed description of individual modules along with the simulation result is furnished in the following section.

4.1 Design of CMOS folding circuit

Folding circuit is employed to reduce the number of comparators which is accomplished by corrugating the input signal along the reference voltages. The folding circuit [15], [16] is as shown in the figure 28. This is a circuit with folding factor of four. The circuit comprises of five differential pair with the output of even and odd pairs cross coupled hence, the name cross-coupled differential pair. The input signal is connected to one terminal of differential pair and uniformly spaced reference voltages Vref1, Vref2,…Vref5 are connected to the other terminals of each CDP. The output resistors are used to sum up the individual differential pair current and generate a unique folded signal.
Figure 28. Schematic of the cross coupled differential pair based folding circuit
The differential pair which has reference voltage close to the input voltage is active while the other differential pairs which are not close to the crossing point are saturated. Hence this phenomenon results in a zero crossing along the reference voltages.

The simulation of folding circuit depicting the transfer characteristics are as shown in figure 29. As the input increases linearly from zero to 1.2V, the differential output initially increases subsequently crosses zero voltage at \( V_{ref1} \), then folds back and crosses zero when input signal is \( V_{ref2} \). This repeats and eventually a fourfold signal with five zero crossings is generated.

![Transfer characteristics of folding circuit](image)

Figure 29. **Simulation of transfer characteristic of folding circuit**

The output of the folder circuit for a sinusoidal signal is shown in the next plot. As explained, the output of the folding circuit has a higher frequency as it multiplies input signal by folding factor, this can be clearly observed from the simulation result as in figure 30.
To cover the entire dynamic range of the input signal from 0.3V to 0.9V, a minimum of five folding circuits are required with the respective voltages as shown in table 6. The output of the folding block consisting of five folding circuits is shown in the figure 31.
Table 6 Reference voltage versus the folder block

<table>
<thead>
<tr>
<th>Reference Voltage</th>
<th>Folder</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.3</td>
<td>Folder 1</td>
</tr>
<tr>
<td>0.3375</td>
<td>Folder 2</td>
</tr>
<tr>
<td>0.375</td>
<td>Folder 3</td>
</tr>
<tr>
<td>0.4125</td>
<td>Folder 4</td>
</tr>
<tr>
<td>0.45</td>
<td>Folder 1</td>
</tr>
<tr>
<td>0.4875</td>
<td>Folder 2</td>
</tr>
<tr>
<td>0.525</td>
<td>Folder 3</td>
</tr>
<tr>
<td>0.5625</td>
<td>Folder 4</td>
</tr>
<tr>
<td>0.6</td>
<td>Folder 1</td>
</tr>
<tr>
<td>0.6375</td>
<td>Folder 2</td>
</tr>
<tr>
<td>0.675</td>
<td>Folder 3</td>
</tr>
<tr>
<td>0.7125</td>
<td>Folder 4</td>
</tr>
<tr>
<td>0.75</td>
<td>Folder 1</td>
</tr>
<tr>
<td>0.7875</td>
<td>Folder 2</td>
</tr>
<tr>
<td>0.825</td>
<td>Folder 3</td>
</tr>
<tr>
<td>0.8625</td>
<td>Folder 4</td>
</tr>
</tbody>
</table>

The following points have to be considered when designing the folding and interpolation circuit. Firstly, the size of MOSFETs in differential pair should be large enough for good linearity of the transfer curve and hence linearity of ADC. Larger devices help reduce the offset voltage that contributes INL and DNL. However, larger MOSFETS have larger parasitic capacitances that lower the bandwidth of the folding circuit. The size of MOSFETs is limited by speed and area. A tradeoff has to be made between operating speed and area of the ADC.
The load resistor value is also critical. It should be large to maintain adequate gain of folder circuit. But the bandwidth is inversely proportional to resistor value. Hence the resistor values must be chosen carefully. In this design, the size of MOSFET is in micrometers while the resistors value range in few kilo-ohms.

4.2 Resistive interpolation

Unlike in flash ADC where fifteen comparators are used to generate a 15 bit thermometer code, interpolation can be used to generate intermediate voltages. In order to generate additional zero-crossings either current or voltage (resistive) interpolation can be used. Current interpolation is based on the summation of currents reflected through current mirrors with different ratios so it proves to be power hungry and not very precise due to the non-idealities of the current mirrors [17]. Furthermore, the delay variation in resistive interpolation is minimal as an interpolation factor of four is used. For these reasons, resistive interpolation is preferred.

As the output of folding circuit is differential, a differential resistive interpolation [18] is implemented as shown in figure 32.

![Schematic of differential resistive interpolation circuit](image)

**Figure 32. Schematic of differential resistive interpolation circuit**
In figure 32, the signals V1 and V1n represent the differential output of a folder circuit while V2 and V2n represent the output of subsequent folder circuit. Consequently, the left resistor tree generates positive signals and the right branch generates negative signals for the differential signals produced by interpolation.

Interpolation by two generates accurate zero-crossings, but interpolation by four is used which introduces some errors which are negligible. The complete folding and interpolation circuit output is as shown in figure 33.

![Simulation of transfer characteristics of folding and interpolation circuit](image)

**Figure 33. Simulation of transfer characteristics of folding and interpolation circuit**

As expected the output of the folding circuit has folded the input signal along the reference voltages and interpolation module generates the intermediate zero crossing
signals as seen in figure 33. Over the dynamic range of the input signals i.e. from 0.3V to 0.9V, sixty-four zero crossings are generated which correspond to sixty-four distinct levels of a 6 bit ADC.

4.3 Zero Crossing Detector

The schematic of the zero crossing detector used in this design is as shown in figure 34. Basically this circuit consists of a preamplifier formed by transistors T1, T2, T3, T4 and a decision circuit constituting transistors T5 to T12. The versatile differential amplifier constitutes the preamplifier with a differential input and generates differential output.
namely V1p and V1n as shown in figure 34. The differential amplifier must have sufficient gain in order to amplify the difference between the inputs, which in this case implies to detect zero crossings of the differential input. This circuit must ensure that ample sensitivity is achieved as the input voltage is of the magnitude few milli volts.

The decision circuit basically consists of positive feedback and hysteresis. The size of each transistor must be carefully chosen to ensure accuracy and high operating speed. The transistors with bigger size can have higher current and hence improve the speed but the huge parasitic capacitance becomes a serious concern. A buffer is used to drive the output. In addition, DFF is inserted at the output to achieve better synchronization.

![Transient Response of ZCD](image)

Figure 35. **Transient response of zero crossing detector**

In this figure, the above two differential signals are input to zero crossing detector circuit and the below signal is the digital output, corresponding to the zero crossings of input.
4.4 XOR based encoder

Although the coarse ADC bits, which constitute the MSB bits, can be derived straightforwardly using appropriate comparators, as in flash ADC, and bit synchronization signal from fine ADC, the design of encoder in fine ADC is challenging because of cyclic nature of the thermometer code. The XOR based encoder which converts the thermometer code to one-out of N code and further maps it to the output bits, is implemented in this design.

Unlike the flash ADC, this encoder definitely requires intermediate conversion because of the cyclic nature of its input signals. The intermediate conversion can be done using ‘01’ generator circuit which operate at very high speed; however XOR gates have been used for simplicity of the design. It consists of fifteen XOR gates followed by four eight input OR gate. Similar design has been proposed as auto switching encoder in [19]. The truth table and schematic are furnished in this section.

As it can be seen from the truth table, the first sixteen entries are comparable to the code generated in a four bit flash ADC. The next sixteen signals are similar to the above signals but are of inverted form. These correspond to the MSB bits as 00 and 01 respectively. This pattern is repeated again for MSB bits as 10 and 11 accounting for total of sixty-four entries in the truth table.
Table 7 Truth table of XOR based encoder

<table>
<thead>
<tr>
<th>Cyclic thermometer code (T15 to T0)</th>
<th>Intermediate conversion (I14 to I0)</th>
<th>LSB bits (B3 to B0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000000000000000</td>
<td>0000000000000000</td>
<td>0000</td>
</tr>
<tr>
<td>0000000000000001</td>
<td>0000000000000001</td>
<td>0001</td>
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<td>0000000000000100</td>
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</tr>
<tr>
<td>1111111111111000</td>
<td>0010000000000000</td>
<td>1100</td>
</tr>
<tr>
<td>1111111111111000</td>
<td>0010000000000000</td>
<td>1101</td>
</tr>
<tr>
<td>1111111111111100</td>
<td>0010000000000000</td>
<td>1110</td>
</tr>
<tr>
<td>1111111111111100</td>
<td>0010000000000000</td>
<td>1111</td>
</tr>
</tbody>
</table>
The equation (9) represents output bits for the encoder.

\[
\begin{align*}
\text{Bit}0 &= I0 + I2 + I4 + I6 + I8 + I10 + I12 + I14 \\
\text{Bit}1 &= I1 + I2 + I5 + I6 + I9 + I10 + I13 + I14 \\
\text{Bit}2 &= I3 + I4 + I5 + I6 + I11 + I12 + I13 + I14 \\
\text{Bit}3 &= I7 + I8 + I9 + I10 + I11 + I12 + I13 + I14
\end{align*}
\] (9)

Figure 36. **Schematic of XOR based encoder**
Figure 37. Output four LSB bits of fine ADC encoder for a 20MHz signal

The output of the encoder for a 20MHz sinusoidal signal is as shown in the figure 37. As the input amplitude changes from 0.3V to 0.9V, the output bits vary from 0000 to 1111 every one-fourth of full scale range of input. More explicitly as the MSB bits change from 00 to 11, the LSB bits change from 0000 to 1111 along the range 0.3V to 0.45V, 0.45V to 0.6V, 0.6V to 0.75V and 0.75V to 0.9V. Thus accurate LSB encoding is ensured. It is noticeable that the four LSB bits are synchronous as they are generated using equal number of logic gates.

4.5 Coarse quantizer and bit synchronization

In folding and interpolation ADC, the coarse and fine bits are generated independently in different modules. Hence they have inherent bit synchronization problem and can be
nullified using bit synchronization, error correction or delay equalizer circuits [20]. The details of coarse ADC unit are furnished in this section.

As only two bits have to be generated from the coarse quantizer unit, the circuit is uncomplicated. This can be implemented using comparators similar to flash ADC, however to achieve better synchronization folding circuit is used to generate the MSB bits. This method is called fully folding technique [21] as folding circuits are used in both the coarse ADC and fine ADC block. This technique also contributes to lesser power dissipation. Three comparators are used to spruce the output and to generate reset and set signals. Reset and set signals are required to indicate when the input signal goes below \(V_{\text{min}}\) and above \(V_{\text{max}}\) respectively. The equations for deriving MSB and MSB_1 bits are given below.

\[
\text{MSB} = F
\]

\[
\text{MSB}_1 = \text{Sync} \times \text{RST} + \text{SET}
\]  

(10)

Here \(F\) stands for the output signal of a folding circuit with folding factor of two. The output of this folding circuit is relative to the output of comparator with a reference voltage of 0.6V but this has latency equal to the ones in fine ADC. ‘Sync’ indicates the output of the fifth folding circuit in the fine ADC block which also serves as bit synchronization signal, signals RST and SET are the output of comparator with reference voltage \(V_{\text{min}}\) and \(V_{\text{max}}\) respectively. Figure 38 illustrates scheme of coarse bits generation circuit.
The LSB bits are synchronized with respect to each other as equal numbers of gates are used to derive each output. However, achieving synchronization of LSB with MSB bits is challenging. The unsynchronized output leads to glitches in the output. It becomes critical when the MSB bits have a transition i.e. particularly when the output bits change from 001111 to 010000, 011111 to 100000 and 101111 to 110000.

The glitches introduced in the output due to imperfect timing of the output bits are depicted in the figure 39. They can be classified as positive and negative glitches depending on whether the MSB bits lead or lag in time.

Although bit synchronization circuit could be used, here delay equalization technique using the concept of pipelining is employed to achieve synchronization at lower power dissipation. Besides, the use of folding circuit in coarse ADC eliminates the utilization of...
synchronization circuit as the delay of folding circuit in coarse ADC is same as that in fine ADC. This concept of using folding circuit in both fine and coarse ADC is called fully-folding technique. This technique reduces the number of components and also helps achieve better synchronized outputs.

It is important to sample the coarse and fine ADC at the same time hence same clock is used in both the units.

![Figure 39. Representation of unsynchronized output producing glitches](image)

4.6 Simulation of 6 bit folding and interpolating ADC

The schematic captured in cadence is depicted in the figure 40. The schematic consists of analog preprocessing circuit, interpolating block, zero crossing detectors, encoder and the coarse ADC unit. It consists of five folding circuits in the front end, followed by the
interpolation block with differential resistors, XOR based encoder in the fine ADC block and the coarse ADC block with reset circuit.

Figure 40. **Top level schematic of folding and interpolating ADC**
4.7 Transient analysis of 6 bit ADC

The folding and interpolating ADC circuit designed in 90nm CMOS technology is simulated using the Cadence Analog Design Environment. The simulation of the ADC for a 10MHz sinusoidal signal is shown in the figure 41. As seen from the simulation result, errors are significantly less as the MSB bits are well synchronized with LSB bits.

![Transient Response for 10MHz input sinuoidal](image)

**Figure 41. Transient response for a 10MHz signal representing six output bits**

For better performance measurement of ADC, the output data captured during transient analysis are converted to their decimal equivalent by combining the weighted sums of the digital output as shown in the below equation.

\[
Y = V_T("LS0") + V_T("LS1")\times2 + V_T("LS2")\times4 + V_T("LS3")\times8 + V_T("MS1")\times16 + V_T("MS2")\times32
\]  

(11)

Where LS0, LS1, LS2, LS3 are the least significant bits and MS1, MS2 are the most significant bits of the ADC.
However this has to be normalized to account for the digital output of 1.2V and the offset voltage of 0.6V. Hence, the final equation that represents digitized version of the input signal is as represented below.

\[ \text{Out} = \text{Y} \times \left( \frac{0.6}{1.2} \times 63 \right) + 0.3 \]  

(12)

The result for a 20MHz input is as shown in figure 42. From time domain analysis, it can be seen that the weighted sum correlates the analog input very well. The digitized output is of same frequency and amplitude as the input signal. However this signal has certain delay which accounts to the delay of the complete circuit. Hence the signal is time shifted and overlapped with the input signal.

It must be noted that the clock frequency of 400MHz is used for this simulation.

Figure 42. Simulation for 20MHz sinusoidal signal sampled at 400MHz
4.8 Measurement of static characteristics – INL/DNL measurement

The primary characteristics that define the static performance of an ADC are differential nonlinearity (DNL) and integral nonlinearity (INL). These are measured in terms of LSBs or percent of full-scale range.

DNL error is the difference between an actual step width and the ideal value. A DNL error specification of less than or equal to one LSB ensures no missing codes. An ADC's monotonicity is guaranteed when its digital output increases with an increasing input signal. INL error is described as the deviation of an actual transfer function from a straight line otherwise ideal infinite resolution ADC. INL is sum of DNL up to that code i.e. cumulative DNL.

There are several ways in which INL/DNL are measured for an ADC such as

- Ramp signal - by using a full scale ramp signal with time period equal to product of sampling time and number of discrete output levels, as input to ADC and plotting the corresponding digitized output.

- Sinusoidal signal - a ramp signal is often replaced with a slow sinusoidal signal of few kilo hertz frequency to measure linearity parameters. The peak to peak amplitude of this sine wave must match to the full scale voltage of the ADC.

- Using Matlab – simulation results from spectre are exported to matlab and compared to the ideal set of output voltages for that particular ADC. The deviation with individual code represents DNL and the cumulative DNL provides an estimate of INL.
Here the DNL/INL analysis is performed using MATLAB as other techniques are time consuming. The set of output voltage levels are exported from Cadence Spectre as .CSV file subsequently read into MATLAB as a matrix and compared with another matrix with the ideal voltage values for a 6 bit ADC. The plots of DNL/INL are furnished in figure 43 for an input signal of 20MHz sampled at 400MHz.

Figure 43. Measure of DNL and INL for 20MHz signal sampled at 400MHz
As observed from this plot the DNL varies from 0.168 LSB to -0.137 LSB and INL is from 0.215 LSB to -0.132 LSB. This guarantees the DNL and INL values are well within the limits.

4.9  Spectral analysis of ADC

Although the performance of the ADC can be established using transient analysis, spectrum analysis provides information on dynamic characteristics of the output such as SNR, SFDR, ENOB and so on. Hence FFT analysis is performed on the output signal which is the digitized form of input signal. The number of points on the spectrum and the duration of FFT simulation are a matter of concern to achieve precise results. The following equations can be used to obtain precise FFT results.

\[ \Delta f = \frac{F_s}{N} \]  \hspace{1cm} (13)

where \( \Delta f \) represents the multiple of input frequency, \( F_s \) is the sampling frequency and \( N \) is the number of FFT samples. The duration of FFT simulation is also dependent on the sampling frequency and number of FFT samples. For instance, to perform 512 point FFT on an input signal of 10MHz, the sampling frequency can be 5.12GHz and the total duration must be 512/5.12G which is equal to 100ns.

The above discussion implies that the sampling frequency has to be a power of two to achieve good FFT results for 20MHz input signal. A sampling frequency of 512MHz is employed in order to divide the spectrum into discrete multiples of input signal frequency. The power spectrum of input sinusoid is as shown in the figure 44. The sampling frequency was slightly increased to 512MHz in order to obtain the accurate frequency representation. Considering frequencies ranging for dc to half of the sampling
frequency i.e 256MHz, the estimated SFDR for 20MHz input is almost 30dB effectively producing more than five output bits. In this measurement, the power spectrum at zero frequency is ignored as it corresponds to the DC signal content in the output signal, which is due to an offset of 0.6V in the output.

![FFT results for 20MHz](image)

**Figure 44.** Folding and interpolation ADC FFT results for 20MHz

The plot of SFDR versus input signal frequency at fixed sampling frequency of 400MHz is shown in figure 45. This folding and interpolation ADC achieves 30dB up to 20MHz and 15dB at 100MHz, respectively. It can be seen that SFDR varies about 15dB when the frequency varies from 10MHz to 100MHz.
4.10 Summary of Folding and Interpolating ADC

While a 6 bit flash ADC requires sixty four resistors in reference ladder and sixty three unique comparators to generate thermometer code, the folding and interpolating ADC can be designed using only sixteen resistors in the reference ladder and twenty comparators. This clearly implies that the designed ADC has smaller number of components and hence consumes less power and can be built on small die area. Table 7 summarizes the performance of this ADC.
Table 8 Performance summary of Folding and Interpolating ADC

<table>
<thead>
<tr>
<th>Technology</th>
<th>CMOS 90nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture</td>
<td>Folding and interpolation ADC</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.2V</td>
</tr>
<tr>
<td>Number of output bits</td>
<td>6</td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>400MHz</td>
</tr>
<tr>
<td>Input dynamic range</td>
<td>0.3≤Vin≤0.9V</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>40MHz</td>
</tr>
<tr>
<td>Resolution</td>
<td>9.375mV</td>
</tr>
<tr>
<td>Input signal frequency</td>
<td>20MHz, 40MHz</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>2.134mW, 2.169mW</td>
</tr>
<tr>
<td>SFDR</td>
<td>30dB, 24dB</td>
</tr>
</tbody>
</table>

The state of art 6 bit CMOS folding and interpolating ADC is presented here. From this table we can conclude that the designed ADC has the good performance and has the least power dissipation.

Table 9 State of the art 6 bit CMOS folding and interpolating ADCs

<table>
<thead>
<tr>
<th>Process(nm)</th>
<th>Sampling clock(MHz)</th>
<th>Input BW(MHz)</th>
<th>Power(mW)</th>
<th>Publication</th>
</tr>
</thead>
<tbody>
<tr>
<td>90nm</td>
<td>400</td>
<td>40</td>
<td><a href="mailto:2.2@1.2V">2.2@1.2V</a></td>
<td>This work</td>
</tr>
<tr>
<td>130nm</td>
<td>600</td>
<td>30</td>
<td><a href="mailto:25@1.4V">25@1.4V</a></td>
<td>IEEE, 2009 [22]</td>
</tr>
<tr>
<td>180nm</td>
<td>100</td>
<td>50</td>
<td><a href="mailto:4.5@1.8V">4.5@1.8V</a></td>
<td>IEEE, 2006 [23]</td>
</tr>
<tr>
<td>500nm</td>
<td>200</td>
<td>40</td>
<td>150@3V</td>
<td>IEEE, 1998 [24]</td>
</tr>
</tbody>
</table>
5. Conclusion

The design and implementation of two interesting ADC architectures is discussed in this thesis. Both the low resolution ultra high speed flash ADC plus the low power, moderate resolution folding and interpolating ADC were designed and successfully implemented in CMOS 90nm technology.

4 bit ultra high speed 5GSPS flash ADC

An ultra high speed 4 bit flash ADC operating at 5GSPS over a bandwidth of 500MHz is presented. As the sampling frequency of flash ADCs increases, the need to design an ultra high speed thermometer-to-binary encoder also increases. The quest for such a design has led to the development of new design which is almost two times faster than the high speed Fat tree encoders. Although the power dissipation is larger than the other encoder, it contributes to a significant improvement in performance of the ADC. This logic can be easily extended to higher number of bits, using the output bits pattern. The performance and low cost of this encoder makes it suitable for most high speed flash ADCs.

6 bit low power folding and interpolating ADC

The low power, high speed folding and interpolating ADC design is intricate. An efficient folding circuit with differential output voltage constitutes the analog preprocessing block and is core to this ADC. The design of resistor in interpolation block and the clocked comparators are vital in achieving desired bandwidth. As the coarse and fine bits are generated separately, a major challenge lies in the design of synchronization circuit to obtain accurate results. Here a 6 bit ADC which has optimum performance over a bandwidth of 20MHz and sampling frequency 400MHz is designed and simulated
successfully. The minimal usage of the comparators makes this design unique. The folding circuit used in coarse ADC block results in optimization of synchronization circuits.

The low voltage, moderate resolution ADCs find immense application in the field of communication, data storage systems and other embedded applications. Furthermore, these low resolution ADCs can be used as building blocks in pipelined ADC architectures to achieve higher resolution.
6. Future Work

The folding and interpolating ADC can be designed for high resolution i.e. the output bits can be more than six bits. Furthermore, the folding circuit along with the zero crossing detector and interpolator limits the bandwidth of input signal. Hence there exists a scope to increase resolution as well as the bandwidth of this ADC. The current interpolation circuit operating at high speed can be incorporated if the power dissipation is not a criterion. Folded cascade architectures along with output buffers can be used to increase the bandwidth. Alternately, a sample and hold circuit can be used in the front end of the circuit in order to achieve higher bandwidth. However immense attention must be given to gain, offset and timing errors.

In a multistage ADC, there exists a major timing mismatch between the output of coarse ADC and fine ADC. Although a few bit synchronization circuits exist, a much efficient encoder and synchronization circuits can be designed. An enhanced digital error correction circuits can also be designed.

Lastly, this design has been simulated at circuit level using cadence analog design environment. The layout for this circuit is yet to be designed and validated. Nevertheless it is beyond the scope of this thesis.
7. References


