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Wideband Automatic Gain Control Design in 130 nm CMOS Process for Wireless Receiver Applications

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Wideband Automatic Gain Control Design in 130 nm CMOS Process for Wireless Receiver Applications

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Engineering

By

Joseph Benito Strzelecki, B.S.
Wright State University, 2013

2015
Wright State University
I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION
BY Joseph Benito Strzelecki ENTITLED Wideband Automatic Gain Control Design in 130 nm
CMOS Process for Wireless Receiver Applications BE ACCEPTED IN PARTIAL
FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in
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Abstract

Strzelecki, Joseph Benito, M.S.Egr, Department of Electrical Engineering, Wright State University, 2015. “Wideband Automatic Gain Control Design in 130 nm CMOS Process for Wireless Receiver Applications”

An analog automatic gain control circuit (AGC) and mixer were implemented in 130 nm CMOS technology. The proposed AGC was intended for implementation into a wireless receiver chain. Design specifications required a 60 dB tuning range on the output of the AGC, a settling time within several microseconds, and minimum circuit complexity to reduce area usage and power consumption.

Desired AGC functionality was achieved through the use of four nonlinear variable gain amplifiers (VGAs) and a single LC filter in the forward path of the circuit and a control loop containing an RMS power detector, a multistage comparator, and a charging capacitor. Down conversion of the AGC output signal to a low frequency was achieved through the use of a modified quadrature Gilbert cell mixer.

The proposed AGC achieves a 63 dB practical tuning range with a settling time of 2 μs for the worst case input condition. Estimated power consumption of the circuit is 4.41 mW when operating at maximum gain. The proposed AGC suppresses DC offset corruption introduced from the mixer and minimizes undesirable variations in the steady-state response.
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I. Introduction

1.1 Automatic Gain Control Applications

Automatic gain control circuits (AGCs) are important for many RF and communication applications. An AGC is an analog circuit that amplifies a periodic input signal of varying amplitude to produce a similar output signal with a constant amplitude. In applications such as speaker or microphone systems, an AGC prevents sudden changes in audio levels that may arise from variations in the recorded sound.

In radio-frequency (RF) communications, AGCs are a common component in transceiver chains. In wireless communication, weather effects, terrain, and the distance from the transmitter to receiver can affect the strength of an incoming signal. In such unpredictable and changing environments, an AGC can compensate for variations in signal strength.

Recent advances in reducing CMOS transistor feature size have allowed for transceiver chains to be implemented as a system-on-chip (SOC) instead of system-on-package implementations (SOPs). A SOP implementation packages an individual amplifier or an individual transceiver component such as an AGC onto a single integrated circuit (IC). Multiple ICs are then connected externally to each other to perform all necessary transceiver functions. In a SOC implementation, all relevant analog and digital components are placed onto a single chip. In industry, the continued push to miniaturize electronics and telecommunications technology has required that more wireless RF components be implemented as a system-on-chip [1]. An SOC implementation allows designers to avoid the losses and RLC parasitics associated with transferring signals through external bonding.
wires between various ICs. Furthermore, packing items onto a single IC saves design space and drives down physical cost [2].

A typical receiver chain starts with an external antenna which receives a low-amplitude modulated signal. A bandpass filter can then select the desired range of carrier frequencies. The signal amplitude is then increased through a series of amplifiers. Each component in the receiver chain introduces some amount of unwanted noise that is not representative of the original signal. Because receiver chains include multiple amplifiers, the added noise from the initial components in the receiver chain have the biggest impact on reducing signal-to-noise ratio (SNR) since both the signal and noise amplitudes are multiplied in subsequent stages; moreover, since the input signal amplitude is small typically in the range of microvolts, even tiny amounts of noise can greatly reduce SNR. Therefore, a low-noise amplifier (LNA) is inserted as the initial amplifier in the chain. A LNA is a special amplifier designed with minimal noise factor (F), defined as ratio of the SNR of the input signal to the SNR of the output signal, to boost the amplitude of the received signal from the antenna.

After the LNA, an AGC maintains a desired constant signal amplitude. Typically, the amplifiers used in an AGC are not LNAs due to their increased implementation cost. In the case of CMOS integrated circuit applications, LNAs require large on-chip inductors which are prohibitive in chip area usage. A mixer then accepts the output of the AGC and a digital square-wave signal from a local oscillator. The mixer’s produces the multiplication of two input signals which have spectral content containing the sum and the difference of both
input signal’s frequencies. For the purpose of processing the signal, the first nyquist zone which contains the lowest positive frequency component is desired. The higher frequencies are removed through a lowpass filter—a process called downconversion. The data is then ready to be demodulated or converted into digital bits by an analog-to-digital converter (ADC) for signal processing. In Figure 1, a block diagram illustrates the arrangement of individual components in a typical receiver chain.

![Block diagram for a receiver chain](image)

**Fig. 1** Block diagram for a receiver chain

The ADC marks the boundary at which the circuit transitions from analog components that operate continuously across the entire range of possible operating voltages to digital logic that operates at discrete DC intervals of “1” representing the supply voltage of the circuit.
and “0” representing the DC ground. For implementing both analog and digital components onto the same chip, the type of fabrication process in the system’s implementation is of interest.

### 1.2 CMOS Process for RFIC Applications

Traditionally, expensive processes such as BiCMOS, SiGe and GaAs are used for RFIC implementations due to the potential for higher gains and lower noise figures [3]. Due to cheap fabrication costs, low power, and high density, the exclusive use of complimentary metal-oxide field effect transistors (CMOSFETs) is favorable for digital logic [4]. MOSFETs are voltage controlled devices that allow current to pass through them depending on the voltage applied to a control terminal. A CMOS process uses two specific field effect transistors, a PMOS transistor and an NMOS transistor.

PMOS and NMOS transistors are four terminal devices. These terminals are gate (g), drain (d), source (s), and bulk (b). In a PMOS and NMOS transistor, current flows from source to drain. Gate is a terminal to which voltage can be applied to control the amount of current that flows between the source and drain terminals. All MOSFET devices have a threshold voltage \( V_T \) that the gate-to-source voltage must exceed to turn the transistor on and allow current to flow. The bias applied to the bulk terminal can affect the threshold voltage. To simplify the fabrication process, the bulk terminal of all PMOS transistors is set to the highest potential supply voltage and the bulk terminal of all NMOS transistors is set to DC ground, reducing the number of masks required in device fabrication. In Figure 2, the symbols for each MOSFET device and their terminal layout are shown.
Fig. 2 PMOS and NMOS transistor symbols and terminals

The current flowing from drain-to-source ($I_{ds}$) through a transistor is dependent upon the process gain factor ($K_n$ for NMOS and $K_p$ for PMOS), the ratio of a transistor’s physical gate width ($W$) by gate length ($L$), the mode of operation as determined by the gate-to-source voltage ($V_{gs}$) and gate-to-drain voltage ($V_{ds}$), and the channel length modulation factor ($\lambda$). The process gain factor is given by

$$K_n = \mu_n C_{ox}$$  \hspace{1cm} (1)

$$K_p = \mu_p C_{ox}$$  \hspace{1cm} (2)

where $\mu_n$, $\mu_p$, and $C_{ox}$ are the mobility of electrons, mobility of holes, and the capacitance of the transistor’s gate oxide respectively.

In Figure 3, a top-down view of a MOSFET transistor is shown. MOSFETs are created from a layer of silicon with diffused dopants of another element on top of a substrate and include a polysilicon layer above that bisects the diffusion layer. The polysilicon layer acts as the gate terminal with a channel underneath that can impede or allow the flow of
electrons from one section of diffusion to another. The type of the dopants in the diffusion layer determine whether the device functions as a PMOS or NMOS transistor. On the periodic table, group V doping elements such as phosphorous provide excess electrons creating a NMOS transistor suitable for connections near ground, while group III doping elements such as boron provide excess holes creating a PMOS transistor suitable for connections near the supply voltage.

Transistors have three modes of operation. In cutoff mode, the gate-to-source voltage is below the threshold voltage. The drain-to-source current is ideally zero; however, a tiny amount of leakage current exists. In linear mode, the transistor’s gate-to-source voltage has
exceeded the threshold voltage. The transistor turns on allowing current to flow from gate to source. The drain-to-source current varies as a function of drain-to-source voltage and gate-to-source voltage. In saturation mode, the drain-to-source current remains constant ideally as the drain-to-source voltage increases; however, in practical devices, the current still increases at a reduced rate due to channel length modulation effects.

In Table 1, the drain-to-source current of a NMOS transistor is listed for each operating region. In table 2, the source-to-drain current of a PMOS transistor is listed for each operating region [5].

<table>
<thead>
<tr>
<th>Region</th>
<th>DC Drain-to-Source Current ($I_{DS}$)</th>
<th>Operating Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff</td>
<td>$I_{DS} = 0$</td>
<td>$V_{GS} &lt; V_T$</td>
</tr>
<tr>
<td>Linear</td>
<td>$I_{DS} = K_n \frac{W}{L} (V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$</td>
<td>$V_{GS} &gt; V_T, V_{DS} &lt; V_{GS} - V_T$</td>
</tr>
<tr>
<td>Saturation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>long channel</td>
<td>$I_{DS} = \frac{K_n W}{2L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$</td>
<td>$V_{GS} &gt; V_T, V_{DS} &gt; V_{GS} - V_T$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$L = large$</td>
</tr>
<tr>
<td>Saturation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>short channel</td>
<td>$I_{DS} = v_{sat} C_{ox} W (V_{GS} - V_T) (1 + \lambda V_{DS})$</td>
<td>$V_{GS} &gt; V_T, V_{DS} &gt; V_{GS} - V_T$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$L = near minimum$</td>
</tr>
</tbody>
</table>
Each transistor also possesses some parasitic resistances and capacitances that affect the performance of IC devices. For analog circuits, the parasitics affect the AC response of amplifiers. A transistor can be modelled as having capacitors that connect the various terminals of the device as shown in Figure 4. These parasitic capacitances are $C_{gd}$, $C_{db}$, $C_{gs}$, $C_{sb}$, and $C_{gb}$.
By adjusting the widths and lengths of transistors, the device currents, parasitics, and various analog and digital device parameters can be set.

1.3 IC Device Parameters

For analog devices, several criterion are used to evaluate performance. Important parameters are power consumption, area usage, operating frequency, tuning range, settling time, output isolation, noise factor, 1 dB and third order compression points. To reduce operational costs, it is desirable to minimize the power consumption. Reducing the floorplan size of the circuit, allows more components to fit elsewhere on-chip. Tuning range is defined as the range of input amplitudes that a device can accept. Settling time is defined as the length of time required for the output of a device to achieve a steady-state condition. Operating frequency is the speed at which the circuit must operate. Output
isolation is the effect that one circuit component has on the operation of another. All IC devices introduce some load on previous circuit components that slow operating speeds. In the some specific cases, added noise and signal corruption can occur. To ensure reliability, the noise generated by any circuit components must be minimized. Finally, the 1 dB compression point and third order intercept point are a measure of linearity.

1.4 Motivation and Objective
In order to drive down the cost of wireless appliances and as part of a project to develop an SOC implementation that integrates an entire IC receiver chain with large digital signal processing units, the design of an AGC in a CMOS process is necessary. Such an AGC must overcome the gain and noise limitations inherent with a CMOS process to achieve a wide tuning range and isolate itself from other components within the circuit while taking advantage of the low power and small size afforded by CMOS technology.

For this implementation of a wireless receiver chain, an AGC and mixer are required for a specific channel operating at 1.575 GHz with a 0.6 V DC offset. The channel’s input signals have amplitudes that range from 0.3 µV to 300 µV. The output of the AGC is fed into a mixer which downconverts the signal to intermediate frequency or baseband. The AGC and mixer were designed in a 130 nm CMOS process with the intent of eventually fabricating the device by using the EDA tool of Cadence Virtuoso 6.1.5.

1.5 AGC Design
A simple AGC consists of three components. A variable gain amplifier (VGA), a peak
detector, and a comparator. Two common configurations exist. The first is a feedforward AGC as shown in Figure 5a. In a feedforward AGC, a modulated sinusoidal input signal ($V_{in}$) is fed into a peak detector and a VGA. The peak detector produces a DC value ($V_{peak}$) that is indicative of the peak amplitude of $V_{in}$. $V_{peak}$ can be compared to an external DC reference voltage ($V_{ref}$). A control voltage ($V_c$) is produced with a DC voltage value that indicates whether the gain of the VGA should be increased or decreased. Since $V_{ref}$ is a constant DC value, the amplitude of the output voltage signal ($V_{out}$) of the AGC from the VGA is constant. Since the VGA’s control path runs in parallel with the amplification of the input signal, the settling time of the AGC is near-zero. A drawback to feedforward AGC designs, is that the peak detector must be highly sensitive and accurate to measure the smaller amplitude of the AGC’s input signal [6].

![AGC configurations](image)

**Fig. 5** AGC configurations: a). feedforward design and b). feedback design

In a feedback AGC as shown in Figure 5b, $V_{in}$ is fed into the VGA only. The peak detector reads the amplitude of $V_{out}$ instead of $V_{in}$. The peak amplitude of $V_{out}$ is then compared with a DC external reference signal. A control voltage signal then indicates whether the
gain of the AGC should be adjusted higher or lower to maintain a constant output amplitude. The feedback design introduces a relatively large settling time for the output amplitude of the AGC circuit to converge to the desired reference voltage. This settling time is dependent upon the propagation delay of the VGA, peak detector, and comparator. The advantage of the feedback design over the feedforward design is that peak detector reads larger amplitude signals. Measuring higher amplitudes allows the AGC to achieve a higher tuning range since the peak detector does not need to be as sensitive and allows for greater reliability since sources of noise can affect the measured amplitude of the signal.

For the proposed wireless receiver chain, the amplitude of the input signal ranges from 0.3 µV to 300 µV. The lower bound of input amplitudes cannot be measured by a peak detector reliably; moreover, the accuracy of the DC reference voltage can only be ensured to within a millivolt. Thus, a feedback AGC design is necessary.

1.6 The State-of-the-Art of CMOS Feedback AGCs

Presently, CMOS feedback AGCs are sometimes combined with feedforward designs. Fast feedforward control can digitally adjust the gain of an AGC to within some margin of error while a feedback loop can slowly fine tune the gain of the VGAs within the circuit. In Alegre et al. [7], a feedforward-feedback AGC can converge over 0.8 µs over a 12 dB range in a 0.35 µm process at 250 MHz.

Digital feedback AGCs are common in some receiver chains that require an AGC after downconversion to low frequencies by a mixer. The incoming signal is quantized and
calculations can be performed in digital bits to determine the necessary gain of the circuit. In Jeon et al. [8], a 0.18 µm process digital AGC achieved a 4.8 µs settling time over a 40 dB tuning range at 8.3 MHz while consuming 11.2 mW of power. In Li et al. [9], a 0.18 µm process, low frequency digital AGC was able to achieve a tuning range of 95 dB and settle over 1.25 µs with a power consumption of 1.71 mW.

For the category of analog AGCs of which this proposed device belongs to, the amplifiers in the circuit often operate at higher frequencies. In Ximenes and Swart [10], a 0.18 µm analog AGC that adjusts the gain of a voltage controlled LNA operating at 2.4 GHz, which feeds into a mixer to downconvert to 1 MHz and then feed into a peak detector. The feedback loop from the peak detector to LNA is capable of settling within approximately 5 µs over a 30 dB tuning range. In Wang and Liu [11], a 0.18 µm process analog AGC with a linear response achieved a settling time of 1.6µs and a 28.5 dB tuning range while consuming 43.2 mW of power. In Qianqian et al. [12], a 0.18 µm process analog AGC with a charge pump control loop was capable of achieving a 55 dB tuning range while operating at 30 MHz with a 5 mW power consumption.
II. Wireless Receiver AGC Design

In Figure 6, a block diagram of a proposed analog AGC is shown.

![Proposed AGC block diagram.](image)

The selected AGC design has a forward path containing four VGAs in series. The purpose of each VGA is to amplify a received analog signal \( V_{in} \). The gain of the forward path is set by a control loop which contains a peak detector, a comparator, and a loop capacitor. Inside the control loop, a peak detector measures the amplitude of the output signal of the last stage of the forward path. A four stage comparator then compares the measured peak signal \( V_{peak} \) with a reference voltage \( V_{ref} \) that indicates the desired output amplitude for the AGC to converge to. The output of the comparator determines whether a loop capacitor will charge or discharge. The loop capacitor stores the DC voltage \( V_c \) that adjusts the gain of the VGAs in the forward path. If \( V_{peak} \) is greater than \( V_{ref} \), the loop capacitor charges, \( V_c \) increases, and the gain of the forward path decreases. If \( V_{peak} \) is less than \( V_{ref} \), the loop...
capacitor discharges, \( V_c \) decreases, and the gain of the forward path increases. The output of the AGC’s forward path is then fed into a mixer. The proposed design measures the peak amplitude at the output of the mixer in order to reduce settling time and improve the steady-state response of the device since the time between measured peaks is smaller for higher frequencies. The design, theory, and optimization of the individual components with the AGC are discussed in the following sections.

2.1 Logarithmic Amplifier Architecture

Typical AGCs are designed with a linear or logarithmic response between the gain of the forward path amplifiers and the control voltage produced from the feedback loop. A linear or logarithmic response allows the device to be easily integrated with other components in the receiver chain since the settling time can be modelled as a simple linear function in the linear or decibel domain.

Logarithmic functions can be produced by using an operational amplifier with a npn or pnp bipolar junction transistor (BJT) inside a negative feedback loop [13] as shown in Figure 7. A BJT is a current controlled device with three terminals named collector (C), emitter (E), and base (B). If current flows through the base terminal, a proportional amount of current can flow through the emitter and the collector terminals. If an npn BJT is used in the logarithmic amplifier, the output is positive. If a pnp BJT is used, the output is negative. The output voltage of the circuit is proportional to the natural logarithm of the current through the collector of the BJT divided by the reverse saturation current of the BJT.
The logarithmic amplifier in Figure 7 possesses several undesirable characteristics. BJTs are sensitive to variations in temperature [14]. For a design that include passive resistors which are sources of thermal noise, the use of BJTs is undesirable. The design also features a single ended input. Amplifiers can accept a double-ended or single-ended input signal. A doubled-ended input accepts a two signals that are 180 degrees out of phase with each other. This differential signal can be exploited to achieve higher gains in amplifiers. Furthermore when a signal is subjected to noise, noise often affects both phase shifted signals equally. When a differential signal is applied to the input of a component, the noise on one signal is cancelled out by the noise on the other phase shifted signal. Thus due to noise considerations, for the proposed wireless receiver chain AGC, a linear response was first explored through the implementation of VGAs which can be designed to accept
differential signals.

2.2 VGA Architecture

For the implementation of the proposed AGC, a linear response simplifies the feedback loop of the AGC and reduces the overall complexity of the circuit. In Figure 8, the design of a VGA is shown. A typical differential VGA implements two passive resistors and three NMOS transistors M1, M2, and M3 acting in the long-channel saturation region. A differential AC signal with 0.6 volts DC is applied to the gates of M1 and M2 of the same width. At the gate of M3, a DC control signal is applied to control the gain of the circuit.

![VGA schematic](image)

**Fig. 8 VGA schematic**

The small signal model for the differential VGA in Figure 8 is given in Figure 9. The small signal model is a diagram displaying all relevant resistances and capacitances that affect the AC characteristics of the circuit.
Rs and Cs are the output source resistance and capacitance of the previous stage of circuitry connected to the input of the VGA. CL is the output load capacitance from next stage of circuitry connected to the VGA. All other values are internal parasitics within the VGA.

The small signal model in Figure 9 features a single capacitance Cgd1 that connects both the input and output nodes of the circuit. The effect of Cgd1 on the input and output capacitance of the amplifier can be modelled by the Miller Effect which models Cgd1 as separate effective capacitances seen by input and output nodes. The effective capacitance seen by the input of the amplifier as a result of Cgd1 is given by

$$C_{gd1\text{input}} = (1 - A_v)C_{gd1}$$

(3)

and the output component of Cgd1 is approximately Cgd1. The Miller Effect is illustrated in the revised small signal model shown in Figure 10.

Fig. 9 Differential VGA small signal model

Fig. 10 Miller Effect on differential VGA small signal model
According to the small signal model, the total input and output resistances and capacitances for the amplifier are

\[
C_{in} = C_s + C_{gs1} + (1 - A_v)C_{gd1} \tag{4}
\]

\[
C_{out} = C_{dB1} + C_{gd1} + C_L \tag{5}
\]

\[
R_{in} = R_s \tag{6}
\]

\[
R_{out} = \frac{R_Dr_{ds1}}{R_D + r_{ds1}} \tag{7}
\]

The single ended low frequency gain of the amplifier in Figure 8 is

\[
A_v = -g_{m1}r_{out} \tag{8}
\]

Parameter \( g_m \) is the transconductance of transistor M1. Using long channel saturation current equation for a NMOS transistor from Table 1

\[
I_{DS} = \frac{K_n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \tag{9}
\]

The transconductance can be achieved by

\[
g_m = \frac{\partial I_{SD}}{\partial V_{GS}} \tag{10}
\]

Ignoring the effects of channel length modulation, Equation 10 can be approximated as

\[
g_m \approx \sqrt{2K_n \frac{W}{L} I_{DS}} \tag{11}
\]

\( r_{out} \) is given by the parallel configuration of channel resistance of M1 (\( r_{ds1} \)) and passive resistor \( R_D \). If \( R_D \) is much smaller than \( r_{ds1} \), then effect of \( r_{ds1} \) can be ignored. The single ended output gain is thus

\[
A_v \approx -g_{m1}R_D \tag{12}
\]

The DC current through \( I_{DS1} \) is one half the current of \( I_{DS3} \). The current through \( I_{DS3} \) is given by Equation 13 for long channel MOSFET under saturation region.

\[
I_{DS3} = \frac{1}{2} I_{DS1} \tag{13}
\]
\[ I_{DS3} = \frac{K_n}{2} \frac{W_3}{L_3} (V_c - V_T)^2 (1 + \lambda_3 V_{DS3}) \]  

(13)

Substituting \( I_{ds1} \) into Equation 11 and ignoring the effects of channel length modulation, \( g_{m1} \) becomes

\[
g_{m1} = \sqrt{\frac{K_n^2 W_1 W_3}{2 L_1 L_3} (V_c - V_T)^2} \]  

(14)

Therefore, the single ended output DC gain can be rewritten as

\[
A_{v_s} \approx -K_n (V_c - V_T) \sqrt{\frac{(W_1/L_1)(W_3/L_3)}{2}} R_D \]  

(15)

The differential output DC gain of the design in Figure 8 is

\[
A_v \approx -2K_n (V_c - V_T) \sqrt{\frac{(W_1/L_1)(W_3/L_3)}{2}} R_D \]  

(16)

The gain of a differential VGA is therefore a linear function of the control voltage. By adjusting the resistance of the passive resistors and the widths of transistors M1, M2, and M3, the gain of the circuit can be set.

To model the gain of an amplifier at higher frequencies, the \( f_{3dB} \) frequency can be calculated. The gain of an amplifier is not constant for all input frequencies. An amplifier’s gain decreases as the frequency of operation increases. The \( f_{3dB} \) frequency as shown in Figure 11, is the frequency where the amplifier gain is three decibels less than the low frequency gain. Beyond the \( f_{3dB} \) frequency, the gain is no longer approximated as being constant.
The $f_{-3dB}$ frequency for an amplifier in Figure 8 is given by [4]

$$f_{-3dB} = \frac{1}{2\pi \sqrt{(R_{out}C_{out})^2+(R_{in}C_{in})^2}}$$ (17)

To maximize the $f_{-3dB}$ frequency, the input and output resistances and capacitances of the circuit at any adjacent stages must be minimized. The term $(1-A_v)$ in Equation 4 magnifies the input capacitance of the VGA, reducing the $f_{-3dB}$ frequency. In the interest of improving the $f_{-3dB}$ frequency the $(1-A_v)$ term can be removed through the technique of cascoding transistors.

### 2.3 Cascode VGA Architecture

In Figure 12, the schematic of a modified VGA with two additional cascode transistors M4 and M5 is shown. The addition of two cascode transistors reduces the gate-to-drain capacitance ($C_{gd}$) seen by the input of the circuit according to Miller’s Theorem.
The addition of cascode transistors M4 and M5 remove the $C_{gd1}$ direct connection between the input and output nodes of the amplifier. The gain across channel of transistor M1 becomes approximately negative one. The effective capacitance seen by the input of the amplifier as a result of $C_{gd1}$ is

$$C_{gd1_{\text{input}}} = 2C_{gd1}$$  \hspace{1cm} (18)

The small signal model for the cascode configuration is shown in Figure 13 [15].

![Fig. 12 Differential VGA schematic with cascode transistors](image)

**Fig. 12** Differential VGA schematic with cascode transistors

![Fig. 13 Cascode VGA small signal model](image)

**Fig. 13** Cascode VGA small signal model
Thus the input and output capacitance of the circuit becomes

\[ C_{in} = C_s + C_{gs1} + 2C_{gd1} \]  \hspace{1cm} (19)

\[ C_{out} = C_{dB4} + C_{gd4} + C_L \] \hspace{1cm} (20)

Since the input capacitance of the VGA no longer varies proportionally according to the gain, a larger \( f_{3dB} \) frequency can be achieved. The tradeoff is a lower gain since \( R_D \) must be reduced to maintain the same output DC offset. The output resistance is now given by

\[ r_{out} = \frac{R_D g_m r_{ds1} r_{ds4}}{R_D + g_m r_{ds1} r_{ds4}} \] \hspace{1cm} (21)

The single ended gain is thus

\[ A_{vs} = -g_{m1} \frac{R_D g_m r_{ds1} r_{ds4}}{R_D + g_m r_{ds1} r_{ds4}} \] \hspace{1cm} (22)

For the chosen technology library, obtaining long-channel saturation devices with a \( f_{3dB} \) frequency beyond 1.575 GHz with a gain larger than a few decibels is impractical for the VGA architectures in Figure 8 and in Figure 12. Adjusting transistor widths of the design to achieve a higher gain results in a lower \( f_{3dB} \) bandwidth. As the \( f_{3dB} \) frequency is further reduced below the desired 1.575 GHz frequency of operation, additional performance improvements by increasing the low frequency gain of the amplifier are cancelled out by the roll-off of the amplifier. Every amplifier architecture has a gain bandwidth product that remains constant. In order to achieve 60 dB at 1.575 GHz, a new VGA architecture with a larger gain-bandwidth product is therefore required. One such technique is to use transistors in short channel saturation by reducing the length of the gate of each transistor to minimum feature size and setting the quiescent overdrive (\( V_{gs-Vt} \)) so a sufficiently high value [16].
2.4 Nonlinear VGA Architecture

For the chosen 130 nm technology process, the maximum achievable gain for the circuit in Figure 8 is relatively small at only 12 dB. To achieve a higher gain, the differential VGA in Figure 12 can be modified to have transistors M1 and M2 operate in short-channel saturation with a smaller length and transistor M3 operate in the linear region. From the short channel saturation equation in Table 1 and by Equation 10, the transconductance of a NMOS transistor in short-channel saturation is given by

\[ g_m = \nu_{sat} C_{ox} W (1 + \lambda V_{DS}) \]  \hspace{1cm} (23)

The DC current through transistor M3 at linear region is given by

\[ I_{DS3} = K_n \frac{W_3}{L_3} \left( V_c - V_{T3} - \frac{V_{DS3}}{2} \right) V_{DS3} \]  \hspace{1cm} (24)

If it is assumed that \( I_{ds1} \) is equal to half of \( I_{ds3} \), then the following can be written

\[ \nu_{sat} C_{ox} W_1 (V_{GS1} - V_{T1}) = \frac{K_n W_3}{2 L_3} \left( V_c - V_{T3} - \frac{V_{DS3}}{2} \right) V_{DS3} \]  \hspace{1cm} (25)

For simplification, if it is denoted that

\[ a = \nu_{sat} C_{ox} W_1 \]  \hspace{1cm} (26)

\[ b = \frac{K_n W_3}{2 L_3} \]  \hspace{1cm} (27)

By substituting Equations 26 and 27 into Equation 25 and by writing Equation 25 in terms of \( V_{DS3} \), it can be shown that

\[ V_{DS3} = V_c - V_{T3} \pm \frac{1}{b} \sqrt{b^2 (V_{T3} - V_c)^2 - 2ab (V_{gs1} - V_{T1})} \]  \hspace{1cm} (28)

The relationship between \( V_c \) and \( V_{gs1} \) is linear since

\[ V_{gs1} = \frac{b}{a} \left( V_c - V_{T3} - \frac{V_{DS3}}{2} \right) V_{DS3} + V_{T1} \]  \hspace{1cm} (29)
Thus the relationship in Equation 28 shows that $V_{DS3}$ is equal to the sum or difference of a linear term of $V_C$ and the square root of a second order polynomial function of $V_c$.

Since $V_{DS1}$ is equal to

$$V_{DS1} = V_{D1} - V_{DS3}$$  \hspace{1cm} (30)

and since the gain is proportional to $V_{DS1}$ as previously mentioned in Equation 23, the response of the VGA gain to $V_c$ is a function of the sum of a negative linear term of $V_c$ plus the square root of a second order polynomial function of $V_c$. To visualize the expected response, a plot of the function

$$y(x) = -x + \sqrt{(2 - x)^2 + 5} + 2$$  \hspace{1cm} (31)

is shown in Figure 14 which is of similar form to Equation 28.

![Plot of $y(x)$ function](image)

**Fig. 14** Expected shape of VGA gain response versus control voltage

As seen in Figure 14, the response of the VGA’s gain versus control voltage is expected to be linear asymptotically for the lower bound of control voltages and flatten out to become nonlinear as $V_c$ approaches the upper bound of control voltages.
To implement a VGA as shown in Figure 12 with the response in Figure 14, the lengths of transistors M1, M2, M4, and M5 must be set to the minimum feature size ensure operation in short-channel saturation. Furthermore, to minimize the number of VGAs required to achieve a gain of 60 dB, the gain of the VGA at 1.575 GHz must be maximized while keeping the f_{-3dB} frequency beyond 1.575 GHz to ensure that lower input frequencies do not saturate the output signal of the amplifier.

The chosen transistor widths of M1, M2, M4, and M5 are 11.72 µm. To ensure that these transistors operate in saturation, a 0.79 V DC bias is applied to the gates of transistors M4 and M5. The DC offset applied to the gates of M1 and M2 are 0.6 V as given by the previous stage LNA in the receiver chain. The width of transistor M3 was set to 21.23 µm to allow the VGA in Figure 12 to accept a control voltage range from 0.6 V to the supply voltage of 1.2 V. At 0.6 V, the gain of the VGA is the largest and decreases as the control voltage approaches 1.2 V. The minimum bound of the control voltage signal is limited to 0.6 V since control voltage inputs below 0.6 V cause V_{DS} to grow too large placing transistors M4 and M5 in the cutoff region which quickly lowers the VGA’s gain. In Figure 15, a line graph displays the gain of the VGA with respect to the control voltage of the circuit according to a Cadence AC analysis. The exact gains for different control voltages with no external load can be seen in Table 3.
Table 3 VGA Gain vs Control Voltage

<table>
<thead>
<tr>
<th>Control Voltage ($V_c$)</th>
<th>Gain (Linear)</th>
<th>Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.6 V</td>
<td>7.85</td>
<td>17.90</td>
</tr>
<tr>
<td>0.7 V</td>
<td>5.16</td>
<td>14.25</td>
</tr>
<tr>
<td>0.8 V</td>
<td>3.15</td>
<td>9.97</td>
</tr>
<tr>
<td>0.9 V</td>
<td>2.40</td>
<td>7.60</td>
</tr>
<tr>
<td>1.0 V</td>
<td>2.04</td>
<td>6.19</td>
</tr>
<tr>
<td>1.1 V</td>
<td>1.84</td>
<td>5.30</td>
</tr>
<tr>
<td>1.2 V</td>
<td>1.72</td>
<td>4.71</td>
</tr>
</tbody>
</table>

Fig. 15 Plot of cascade VGA gain versus control voltage by using AC analysis

As seen in Figure 15, the simulation results match the theoretical calculations in Equation 28. For the smaller control voltages, the response of the circuit is linear and then flattens out as $V_c$ increases. To verify the accuracy of the Cadence AC simulation, Figure 16 shows a plot of the VGA’s gain for different input control voltages using a transient analysis.
The response between the AC and transient analysis is approximately the same. As seen in Figures 15 and 16, the effect of control voltage on the gain of the circuit is nonlinear. The nonlinear response, however, is advantageous for ensuring a stable AGC output signal. The control voltage applied to the VGA is not perfectly constant even when the AGC has fully settled into a steady-state condition. Since the AGC must accept a wide tuning range of 60 dB, AC output signals with small amplitudes less than a microvolt may not exhibit a constant amplitude at steady-state if the control signal increases or decreases by a few microvolts as well. If the gain of the VGA is more insensitive to changes in control voltage for smaller output amplitude signals, a high SNR can be maintained for the entire tuning range.
When $V_c$ is equal to 0.6 V, the low frequency gain of the circuit is approximately 18.0 dB with no external load, and the $f_{3dB}$ frequency is 5.314 GHz as seen in Figure 17.

Figure 17: Cascode VGA AC response for $V_c$ equal to 0.6 V

Four VGAs are required in series to achieve a decibel gain of 60 dB in the forward path of the AGC. Each VGA requires an input DC voltage of 0.6 V. The DC output voltage of each VGA varies depending on the control voltage applied to transistor M3. When a control voltage of 0.6 V is applied to M3, the output DC voltage of the VGA is approximately 0.6 V. For a control voltage of 1.2 V, the DC output voltage is lowered to approximately 0.4 V.
Applying a 0.4 V DC offset to the gates of transistors M1 and M2 can cause transistors with the VGA to operate in the cut-off region. Additional circuitry is therefore required on the output of each VGA to set the DC offset for the next stage amplifier.

### 2.5 DC Offset Correction
To eliminate the DC offset swing, a coupling capacitor can be placed on the output of each VGA. A capacitor acts a DC open circuit but allows the AC component of a signal to pass through the device, as shown in Figure 18. For this role, a single metal-to-metal capacitor (mimcap) is used on each output of the amplifier as a coupling capacitor. To minimize the effect of the added capacitance introduced by the mimcaps from affecting the f_{3dB} frequency of the VGA, the capacitance of each mimcap must be sufficiently small, which as a tradeoff increases the impedance of coupling capacitor. The DC offset becomes approximately zero once the signal passes through the mimcaps. As seen in Figure 18, the DC offset can then be adjusted through a biasing resistor and a 0.6 V DC bias signal supplied from an on-chip voltage regulator. The connection of all four VGA’s and their biasing circuitry to form the forward path of the AGC is shown in Figure 19.
The addition of the biasing circuitry in Figure 18 also acts as a highpass filter. The left corner frequency \( f_c \) of this filter is given by [17]

\[
f_c = \frac{1}{2\pi RC}
\]

(Figure 18 Cascode VGA with coupling capacitors and biasing resistors)

(Figure 19 AGC forward path consisting of four VGAs)

(Frequencies below the corner frequency are attenuated whereas frequencies beyond \( f_c \) are...
unaffected ideally. The AC response of the previous VGA amplifier when combined with the high-pass filter response of the biasing filter produces a bandpass filter AC response. By adjusting the corner frequency of the high-pass filter, the center frequency of the bandpass filter can be set to 1.575 GHz. Some attenuation occurs since the roll-off of the passive RC highpass filter is 20 dB per decade.

2.6 Forward Path Gain

In Figure 20, the simulated AC response of the entire forward path of Figure 18 is shown for $V_c$ equal to 0.6 V, 60 fF coupling capacitors, and biasing resistors of 50 kΩ to minimize the corner frequency. The resistors used to bias the circuit must be sufficiently large to prevent the AC signal fed into the gates of transistors M1 and M2 from affecting the DC bias signal. The bias signal can become corrupted because the gate-to-source current of transistors M1 and M2 varies according the AC voltage applied. AC noise can appear in the bias signal which in turn affects the operation of other amplifiers in the circuit. AC noise in the DC bias signal can modulate with the received input signal at each stage of amplification and affect the spectral content of the input signal.

As seen in Figure 20, the AC response of the last stage of the forward path containing four VGAs is centered close to 300 MHz with a gain of 57.28 dB. The addition of an external load on the output of each VGA and the attenuation by the DC biasing circuitry on the output of each VGA reduces the gain of the forward path below 60 dB at the desired 1.575 GHz frequency of operation.
Fig. 20 Last stage forward path gain versus frequency for 60 fF coupling capacitors and 50 kΩ biasing resistors.

The cause of the poor gain and frequency bandwidth performance of the circuit in Figure 20 is shown in Figure 21 which displays the AC response of the first stage amplifier before and after the coupling capacitor.
The corner frequency of the high-pass filter is sufficiently small; however, the pass-band attenuation is significant. Increasing the resistance of the biasing resistors has negligible effect and only contributes more thermal noise to the circuit. In order to reduce the stopband attenuation, the capacitance of the coupling capacitors can be increased. Figure 22 shows the AC response of the last stage of the forward path with 50 kΩ biasing resistors and a coupling capacitor of 500 fF. The larger coupling capacitors increase the passband gain and reduce the corner frequency of the highpass filter. The last stage low frequency gain surpasses 60 dB at 67.71 dB. Due to the large capacitance on the external coupling capacitor,
the $f_{3dB}$ frequency of the cascode VGAs is diminished with the gain at 1.575 GHz falling below 60 dB at 56.72 dB.

**Fig. 22** Last stage forward path gain versus frequency for 500 fF coupling capacitors and 50 kΩ biasing resistors

Further increases in the forward path gain by adjusting the highpass filter parameters are not feasible. The filter’s AC response is near unity and corner frequency is near DC. The low frequency gain of the cascode VGA in Figure 12 can be reduced to increase the $f_{3dB}$ frequency according to the gain-bandwidth product; however, the gain at the $f_{3dB}$ frequency decreases as well.
To center the AC response of the forward path, additional filters can be included; however, the gain at desired frequency of operation must already surpass 60 dB to meet the design requirements. The low frequency gain of the VGA can be increased to improve the gain at the $f_{3\text{dB}}$ frequency, but increasing the low frequency gain requires the transistor sizes of M1, M2, M3, M4 and M5 be adjusted. As a tradeoff, the range of control voltages accepted by the VGA decreases. If the range of possible control voltages is reduced, the steady-state response of the output amplitude of the AGC cannot settle to a constant value since minor changes in $V_c$ have a large effect on the gain of the VGAs. To increase the gain while maintaining M1, M2, M3, and M4 in saturation and maintaining a wide input range for $V_c$, further modifications are necessary.

2.7 Modified VGA Architecture

2.7.1 Shunt Peak Design

Several techniques allow for higher amplifier gains at the desired frequency of operation. One such technique is a shunt-peaked amplifier design. In a shunt peak design, inductors are added in series with a passive resistor as shown in Figure 23.
The added inductors increase the gain of the amplifier at a specific frequency ($f_0$). The inductance required is given by [4].

$$L = \frac{R_D Q}{2\pi f_0} \tag{33}$$

where $Q$ is the quality factor of the inductor.

By adjusting $f_0$ to be near $f_{3dB}$, the roll-off of the circuit’s AC response becomes sharper while maintaining a constant low-frequency gain. The amplifier is thus capable of amplifying signals close to the original $f_{3dB}$ frequency without significant attenuation. The improved high-frequency performance comes at a cost to area usage. On-chip inductors are relatively large devices. The dimensions of a typical inductor lie within several hundred
micrometers wide and tall. For the forward path of the AGC which implements four VGAs in series, eight inductors are required which exceeds the floorplan available. Furthermore, to achieve a maximally flat AC response with the inclusion of inductors, the inductance must be approximately 60 nH for this implementation. The size of a 60 nH inductor lies beyond the capabilities of the fabrication process. A shunt-peaked design thus proved to be unviable.

2.7.2 Active Resistor Design

Another design technique is replacing the passive resistors $R_D$ with an active CMOS transistor as shown in Figure 24. Replacing a passive component with an active component is desirable for several reasons. Passive resistors are sources of thermal noise because of the dissipation of current through heat [18]. Furthermore passive components have a larger area floorplan compared to typical MOSFETs.
For the short channel saturation operating region, the drain-to-source conductance ($g_{ds}$) of a PMOS transistor is given by

$$g_{ds} = \frac{\partial I_{sd}}{\partial V_{sd}}$$  \hspace{1cm} (34)

Using the source-to-drain current of a PMOS transistor for the short channel saturation operating region in Table 2,

$$g_{ds} = \nu_{sat} C_{ox} W (V_{SG} - |V_T|)$$  \hspace{1cm} (35)

The drain-to-source resistance ($r_{ds}$) is the reciprocal of the drain-to-source conductance.
In Figure 24, the variable gain amplifier in Figure 12 has been modified with a PMOS transistor replacing each passive resistor. These PMOS transistors M6 and M7 are biased with a gate connection to a 0.6 V DC bias. Since the voltage drop across the passive resistors in Figure 12 ranges from 0.75 V to 0.45 V, operation in saturation can be guaranteed for all practical values of $V_c$ and $V_{in}$. As seen in Equation 35, $g_{ds6,7}$ remains constant if the drain-to-source voltage changes. The constant resistance in saturation ensures that the output signal is less affected by gain compression.

The design keeps the cascoded pair of additional NMOS transistors M3 and M4 to compensate for the large gate-to-drain capacitances seen by the output node as a result of the Miller Effect. The control voltage accepted by the VGA is still 0.6 to 1.2 volts with 0.6 volts producing the highest possible gain. Transistor widths for M1, M2, M3, M4, and M5 are the same, and the bias voltage applied to M3 and M4 is still 0.79 volts. With a parametric analysis, the optimal width of transistors M6 and M7 was found to be 13.41 µm.

The small signal model for the design in Figure 24 is shown in Figure 25.
Transistor M6 does not act as an AC current source since the applied gate bias is a DC signal, and thus the gain of the amplifier is similar to Equation 8, with $r_{out}$ now equal to

$$r_{out} = \frac{g_{m4}r_{ds1}r_{ds4}r_{ds6}}{r_{ds6} + g_{m4}r_{ds1}r_{ds4}}$$  \hspace{1cm} (36)$$

As seen in Equation 38, a higher gain is achieved by the increased resistance of $r_{out}$ while maintaining the same voltage drop. The current through the amplifier is smaller as a result. The trade-off is the addition of parastitic capacitances from M6 that can reduce the performance of the circuit at higher frequencies.

2.8 Improved DC Offset Correction

To better control the DC offset swing as $V_c$ changes without the need for large passive resistors, the biasing resistors in Figures 18 and 19 are replaced by a PMOS current source and NMOS current sink as seen in Figure 26. Typical active resistors created from MOSFETs in saturation region produce larger values of resistance with much less area usage. Greatly increasing the resistance causes the corner frequency of the highpass filter created by the biasing circuitry to decrease, resulting in minor performance improvements for the high-frequency gain. The replacement of the large 50 kΩ resistors by small MOSFETs greatly reduces the floorplan of the circuit as well.
The coupling capacitors C1, C2 block the DC offset from the output of the amplifier, allowing the PMOS current source created by B3, B4 and NMOS current sink B5, B6 to set the output DC voltage to a constant 0.6 volts. Two pairs of a single active MOSFET resistor and a passive resistor B1 with R1 and B2 with R2 in separate branches set the reference current and DC bias for the current sources and sinks on the biasing circuitry of all four VGAs. Since the transistors in the current mirror and current sink contribute drain capacitances to the load of the amplifier, the widths of the transistors in the current mirrors are set to near-minimum size, and the capacitance of the coupling capacitors is set once again to 60 fF. Although the gain decreases due to the large impedance of such a small capacitor, the smaller coupling capacitor size allows the current mirror and sink to more quickly set the DC offset to 0.6 V if a change in the DC offset of the VGA’s output node occurs.
The AC response of the VGA and biasing logic in Figure 26 driving another VGA as an external load is shown in Figure 27. The low frequency gain of the amplifier is 24.46 dB and the gain at the 1.575 GHz frequency of operation is 19.45 dB. After the highpass filter created by the biasing logic, the gain at the desired frequency of operation is 16.79 dB. For four stages, 16.79 dB is sufficient to reach 60 dB.

![Modified cascode VGA AC response before and after highpass filter](image)

**Fig. 27** Modified cascode VGA AC response before and after highpass filter

As seen in Figure 28, for four modified cascode VGAs in series, the forward path low-
frequency gain is 84.83 dB. At the desired operating frequency, the gain is lower at 63.69 dB. Although the desired gain at 1.575 GHz has been achieved, the relative magnitude of the low frequency gain can amplify unwanted noise and reduce the SNR of the circuit.

![Graph](image)

**Fig. 28** Last stage forward path gain versus frequency for four modified cascode VGAs

With a gain above 60 dB at 1.575 GHz, additional filters can be included to center the response at the desired operating frequency.
2.9 LC Filtering

Since the gain of the desired center frequency of 1.575 GHz is below the low frequency gain, more filters are required to center the response of the forward path to the desired value. The addition of higher order RC filters; however, introduces undesirable zeroes into the AC response of the VGAs and greatly increase the area usage of the circuit. To overcome this limitation, in the series combination of four modified cascade variable gain amplifiers shown in Figure 24, a parallel LC filter is included in between the third and fourth VGAs of the forward path. Shown in Figure 29, an LC parallel filter with two large inductors L1 and L2 and two large parallel capacitors C3 and C4 is added before the biasing current sources and sinks. This LC filter selects a very narrow band of frequencies. The center frequency \( f_0 \) of the LC filter is given by [17]

\[
f_0 = \frac{1}{2\pi \sqrt{LC}}
\]

(37)

The LC filter is isolated from the VGA and the biasing transistors by two sets of coupling capacitors C1, C2 and C5, C6, which also contribute to setting the resonant frequency of the LC filter.
Fig. 29 Modified Cascode VGA schematic with coupling capacitors C1, C2, C5, C6, LC filter, and biasing current sources B3, B4 and sinks B5, B6

The LC filter is located after the 3rd stage and not the last 4th stage as shown in Figure 30 in order to isolate the inductors from the mixer that is attached to the output of the fourth VGA. The mixer receives a sharp digital square wave, which is not fully isolated from the output of the forward path of the AGC since the gate current drawn from the mixer is not constant depending upon the value of the square wave signal. If the LC filter is located on the output of the 4th stage, the output of the forward path becomes noisy and corrupted through resonance since inductors resist instantaneous changes in current. In Figure 31, the AC gain of the output of the final forward path design is shown for a control voltage of 0.6 V. The response of the circuit is exactly centered at 1.575 GHz with a maximum gain of 62.99 dB.
The forward path is then connected to a feedback loop. After the input signal to the AGC has been amplified by the forward path, some circuity is necessary to measure the amplitude.

2.10 Analog Peak Detection

To measure the peak voltage at the output of the forward path, a peak detector circuit is required. In Figure 32, a peak detector circuit is shown that implements a single comparator. A comparator is a circuit component that accepts two input signals fed into a positive and negative terminal. The comparator produces the voltage difference of the two signals multiplied by a large gain. The gain of the comparator is sufficiently large to ensure the
output signal saturates. If the voltage on the positive input terminal of the circuit is higher than the voltage on the negative input terminal, the comparator produces a logically high DC signal equal to the supply voltage. If the voltage on the negative input terminal of the circuit is higher than the voltage on the positive input terminal, the comparator produces a logically low DC signal equal to ground.

Fig. 32 Forward path of the AGC circuit

The peak detector circuit in Figure 32 features a single comparator that accepts the output of the VGA forward path into its positive input terminal. The output of the comparator is fed into the gates of a single PMOS transistor T2 and NMOS transistor T5. The drains of both transistors are connected to a single mimcap CM1 and fed into the negative input terminal of the comparator to form a feedback loop.

The circuit functions by storing charge on the capacitor CM1. Transistor T2 connects CM1 to the 1.2 V supply voltage, and transistor T5 connects CM1 to a 0.6 V bias. The positive
terminal of the comparator is a periodic signal. The negative terminal is a DC signal. At steady state operation, the output of the comparator becomes a square wave. As the input amplitude to the peak detector increases relative to the stored peak value on CM1, the duty cycle of the output of the comparator decreases which in turn increases the average duration that transistor T2 is on relative to T5. With each cycle, the DC voltage value stored on the capacitor CM1 is compared to the AC input signal again and adjusted accordingly. The DC output signal is thus a percentage of the amplitude of the VGA’s output signal.

To ensure that the peak detector can operate over a large range of frequencies, the comparator must have a large gain. For this implementation, the four stage design in Figure 33 was created. The first stage is an active-load, cascoded common source differential amplifier followed by three single ended input common drain amplifiers. All amplification stages are designed to share the same 0.79 V bias signal used by the VGAs in the AGC.
The high gain of the first stage can be derived by examining the current and resistance at the output node. The AC currents flowing through transistor M4 is given by

\[ i_4 = \frac{g_{m1}v_{in}}{2} \]  

(38)

and the current flowing through transistor M5 is given by

\[ i_5 = \frac{g_{m2}v_{in}}{2} \]  

(39)

where \( v_{in} = v_{inp} - v_{inn} \). Since both M1 and M2 are the same width, the two AC currents are equal but in opposite directions towards the output node. The effective resistance at the output node is given by

\[ r_{out} = \frac{g_{m5}r_{ds2}r_{ds5}r_{ds7}}{g_{m5}r_{ds2}r_{ds5} + r_{ds7}} \]  

(40)

Multiplying the AC current by the output resistance yields the output AC voltage as shown in Equation 41.

\[ v_{out} = \frac{g_{m1}g_{m5}r_{ds2}r_{ds5}r_{ds7}}{g_{m5}r_{ds2}r_{ds5} + r_{ds7}} v_{in} \]  

(41)

The small signal frequency gain of the first stage is thus

\[ A_{v1} = \frac{g_{m1}g_{m5}r_{ds2}r_{ds5}r_{ds7}}{g_{m5}r_{ds2}r_{ds5} + r_{ds7}} \]  

(42)

The subsequent stages adjust the DC output DC offset to 0.6 V. For the design in Figure 33, the gain at the desired frequency of operation is 56.8 dB when driving the peak detector’s logic. The gain is sufficient for operating in the entire tuning range of the circuit.

For most of the intended range of operation, the peak detector in Figure 32 exhibits a linear response between the output DC voltage and the input AC amplitude. A plot of the peak detector’s DC output voltage versus input amplitude can be seen in Figure 34. For the entire
60 dB tuning range, the peak detector has a DC output range of 672 mV for an input amplitude of 0.3 V to 600.1 mV for an input amplitude of 300 µV. As long as the comparator in the next stage of the AGC’s feedback loop has a sufficient gain, the output of the peak detector can be processed. Although the output of the peak detector is miniscule for small output amplitudes, for practical applications, the output of the AGC is not set to converge to amplitudes smaller than 15 mV.

Although the output of the peak detector exhibits some sawtooth behavior since T2 and T5 are constantly switching in steady state, if the capacitance of CM1 is sufficiently large, the output signal remains effectively constant. Increasing the size of CM1 to improve the steady-state response comes at the trade-off of increasing the settling time of the peak detector. For the proposed design, the capacitance of CM1 is 2 pF. The settling time of the peak detector over a sudden 60 dB change is 0.2 µs. At steady state, the DC output varies plus or minus a fraction of a millivolt.
Once the peak amplitude of the circuit has been measured, the necessary control voltage can be generated to control the forward path of the AGC.

### 2.11 VGA Control Voltage Generation

The AGC accepts an external DC reference signal $V_{\text{ref}}$. This external reference determines the value that the AGC’s output amplitude converges to. For the proposed AGC, the external reference is compared to the measured peak value from the detector circuit. As seen in Figure 35, a second comparator is added to the output of the peak detector on the negative input terminal and accepts the reference voltage on the positive terminal. The output of the second reference comparator feeds into another PMOS and NMOS transistor that connect
a mimcap to the 1.2 V supply and 0.6 bias voltage respectively. The second mimcap stores the control voltage that is applied to the VGAs in the forward path of the AGC. A resistor is then used to filter any AC distortions in the control voltage signal.

If the measured peak value of the circuit is greater than the reference voltage, the output of the reference comparator becomes logically low which causes the second capacitor to charge. A higher voltage stored on the second capacitor causes the gain of the VGAs to decrease. Conversely, if the measured peak value of the circuit is less than the reference voltage, the output of the reference comparator becomes logically high which causes the second capacitor to discharge. A lower voltage stored on the second capacitor causes the gain of the VGAs to increase.

To ensure that the control loop is stable, the peak detector’s capacitor must charge or discharge at a faster rate than the capacitor that stores the control voltage to the VGAs. For
the second capacitor, a capacitance of 20 pF was selected resulting a settling time of 0.8 µs for a sudden change between the maximum and minimum value of the peak detector.

2.12 AGC Simulation Results

In Figure 36, an entire AGC schematic circuit design in 130nm CMOS technology is shown. The proposed AGC combines four VGAs as shown in Figure 19 with the peak detector in Figure 32 and control loop shown in Figure 35. Although the circuit’s forward path is not capable of achieving 60 dB without an LC filter as previously shown in Figure 29, the AGC’s settling time can still be quickly measured.

![Proposed AGC design](image)

Figure 37 shows the simulation results for an AGC input signal kept at a constant 0.6 volts DC offset with a 300 µV amplitude sinusoid. The reference voltage is varied between 605 mV to 620 mV. As can be seen in the top plot of Figure 37, the measured peak value of the circuit converges to the reference voltage within half a microsecond. If \( V_{\text{peak}} \) is higher after \( V_{\text{ref}} \) decreases, the control voltage as seen in the second plot of Figure 37 increases to force the gain of the VGA’s to decrease. Likewise it can be seen that for when \( V_{\text{ref}} \) is suddenly higher than \( V_{\text{peak}} \), the control voltage decreases to compensate. Finally, in the third plot of Figure 37, it can be seen that the output of the AGC is constant once a steady-state condition has been reached.
In Figure 37, a simulation is shown for a constant $V_{\text{ref}}$ to the second reference comparator. The AGC input signal is alternated between a constant 0.6 volts DC offset, 3 mV amplitude sinusoid and a 0.6 V DC offset, 30 mV amplitude sinusoid with a transmission gate multiplexer.
As can be seen from the AGC’s fourth stage VGA output response in the bottom plot in Figure 38 and the convergence of $V_{\text{peak}}$ to $V_{\text{ref}}$ in the 2nd plot down, the settling time of the AGC is much larger at 4 µs rising and 2.5 µs falling. The extra delay is caused by the peak detector which requires more than one cycle to measure the change in amplitude on the forward path. The second capacitor in the control loop must sequentially wait for the capacitor in the peak detector to change value in order for the control voltage to increase or decrease. The settling time can be improved by lowering the capacitance of the peak detector mimcap and the second mimcap in the control loop; however, the ripples in the
amplitude of the output of the AGC increase in severity once in steady state. In order to improve the settling time of the AGC without compromising the steady-state response of the circuit, a faster method of peak detection is required.

### 2.13 RMS Power Detector Design

A root mean squared (RMS) power detector is a circuit which accepts an AC input signal and produces a DC output voltage that is the square root of the average of the square of the continuous time function of an AC signal. The relationship is illustrated in Equation 43

\[
V_{\text{RMS}} = \sqrt{\frac{1}{2\pi} \int_{-\pi}^{\pi} V_{in}(t)^2}
\]  

(43)

where \(V_{in}(t)\) is the continuous time function of a periodic signal.

Adapted from Gorisse, Kaiser, & Kerherve [19], a schematic for an RMS power detector is shown in Figure 39. Transistors T2 and T3 are used to convert a pre-existing 0.6 volt DC bias signal into a 0.4 volt DC bias signal for transistor T0 which is used to apply a DC offset to the node connecting the drains of T7, T4, and T5. An analog differential input signal is fed into the gates of transistors T4 and T5. The currents through T2, T4, T5, and T7 can be expressed as

\[
I_{ds4} + I_{ds5} = I_{sd2} + I_{sd7}
\]

(44)

With a gate length long enough to ensure operation in long channel saturation and by ignoring the effects of channel length modulation, the drain currents through T4 and T5 are expressed individually as
\[ I_{ds4} = \frac{k_n W_4}{2} \left( \frac{V_{in}}{2} - V_t \right)^2 \]  
\[ I_{ds5} = \frac{k_n W_5}{2} \left( -\frac{V_{in}}{2} - V_t \right)^2 \]  
\[ I_{ds4} + I_{ds5} = K_n \frac{W}{L} \left( \frac{V_{in}^2}{2} - V_t^2 \right) \]  

Since the widths of T4 and T5 are the same, the current can be rewritten as

\[ I_{ds4} + I_{ds5} = K_n \frac{W}{L} \left( \frac{V_{in}^2}{2} - V_t^2 \right) \]  

From Equation 47, it can be seen that current is proportional to \( V_{in}^2 \), which for an AC signal has a value always greater than or equal to the DC offset. Through a low-pass filter, this signal can be converted into a constant DC value indicative of the AC amplitude of the input signal. Transistors T8 and T6 are used to set the output DC voltage to 0.6 V as a baseline for a 0 V amplitude AC input.

Fig. 39 RMS power detector schematic

In Figure 40, several 0.6 volt DC signals are applied with different AC amplitudes to the
RMS power detector schematic displayed in Figure 39, the DC output voltage is shown for each input stimuli. A plot shows the response in Figure 41. As can be seen from the graph, the DC output voltage is the root mean squared of the AC input voltage.

**Fig. 40** RMS power detector DC output voltages for different AC input signals of various amplitudes
Although the RMS power detector is nonlinear, it has the advantage of a differential input. The peak detector or RMS power detector’s input is also fed directly into the mixer. The differential input signals allow some DC offset noise from the mixer to be cancelled out since transistors T4 and T5 connect to the same node in the circuit. Furthermore the RMS power detector does not require multiple cycles to converge through the use of an external capacitor. The average of an entire period of a signal is taken which assists in cancelling out brief additions of noise that do not last over a single period of the input signal. The

Fig. 41 Plot of RMS power detector DC output voltages versus input amplitudes
settling time is near instant and therefore favorable for implementation in the proposed AGC.

2.14 Final AGC Simulation Results

The final schematic for the modified AGC is shown in Figure 42. The proposed AGC includes four VGAs and the proposed DC biasing architecture shown in Figure 26 with the LC filter architecture shown in Figure 29 inserted between the third and fourth VGAs. After the forward path, an RMS peak detector as shown in Figure 39 measures the amplitude of the forward path. A comparator then compares the measured peak amplitude of the signal and a chosen external reference voltage. The control voltage stored on a large loop capacitor can then be increased or decreased to control the gain of the forward path. An increase in the control voltage reduces the gain of the forward path whereas an increase in the control voltage increases the gain of the forward path.
Fig. 42 Proposed final AGC design
For the circuit proposed in Figure 42, the power consumption is 4.41 mW for the highest forward path gain.

The gain of the forward path for various control voltages is shown in Figure 43.

As seen in Figure 43, the circuit is capable of a 71 dB tuning range from 64.17 dB to -7.07 dB with a control from 0.6 V to 1.2 V respectively. For practical receiver applications, a gain below -2 dB for \( V_c \) equal to 1.0 V is unnecessary. For the highest gain at \( V_c \) equal to 0.6 V, the noise factor of the forward path is shown in Figure 44.
As seen in Figure 44, when the AGC gain decreases, the noise factor increases since the signal’s strength is much less compared to the noise floor. To analyze the effect of the AGC on the entire receiver chain, the noise figure must be divided by the front end gain of the previous components and LNA stages.

To verify that the AGC produces the same output amplitude for a given reference voltage, in Figure 45, the response of the AGC is shown for a reference voltage that alternates between 750 mV and 610 mV and a 30 mV amplitude 0.6 V offset.
As seen in Figure 45, the output signal of the AGC’s forward path converges to the same amplitude for each value of $V_{ref}$.

In Figure 46, the response of the AGC and its control voltage are shown for a reference voltage that falls between from 810 mV to 610 mV with a 300 μV input amplitude with 0.6 V offset.
As seen in Figure 45, the response of $V_c$ rises at a rate of approximately 0.1 V per 0.41 µs. To adjust over a 60 dB range, the circuit settles over approximately 2 µs.

In Figure 47, $V_{ref}$ is kept constant at 0.65 V and the input signal the AGC is alternated between a 3 mV amplitude signal and a 30 mV amplitude signal.
As seen in Figure 47, the circuit properly functions by maintaining a constant output amplitude and converges within 1 µs. The settling time of the modified AGC design with the RMS power detector is much smaller than the 4 µs settling time seen in Figure 38 for an AGC with a comparator-based peak detector.

In Figures 48 and 49, the 1 dB compression point and third order intercept are shown.
Fig. 48 Final AGC forward path 1 dB compression point for Vc equal to 0.6 V

Fig. 49 Final AGC forward path third order intercept point
As seen in Figure 48, the 1 dB compression point is -19.95 dBm and the third order intercept point is -15.278 dBm in Figure 49. Higher values indicate that the output power versus input of the circuit is linear and thus the gain is constant at a given frequency of operation. Maximizing the 1 dB compression point ensures that the device is less affected by gain compression in which the output signal of the circuit is stretched or compressed due to changes in current drawn by the circuit components of the AGC.
III. Mixer Design

3.1 Mixer Architecture

Attached to the output of the AGC’s forward path is a mixer. A mixer is a device that multiplies two AC signals together. A quadrature mixer (differential input, differential output) can be implemented through a modified Gilbert cell. In Figure 50, the transistor schematic of a quadrature mixer is shown. The mixer accepts the differential output of the AGC denoted as $V_{RF}$ and a square wave signal denoted as $V_{LO}$ from a local oscillator. Each of the four branches of the circuit accepts a combination of one end of the two differential signals of both $V_{LO}$ and $V_{RF}$.

Typical mixer architectures implement a common mode current sink to ensure that the total current drawn by the mixer remains constant. Ensuring a steady current throughout each branch of the mixer helps to alleviate effects of gain compression to ensure that the output signal is not skewed. Implementing a shared current sink on the sources of transistors M8, M9, M10, and M11 is not feasible since an NMOS current sink would require transistors that operate in saturation. The drain-to-source voltage is too small while maintaining a 0.6 V DC offset output voltage. To accommodate, PMOS current sources M2 and M3 can be used instead. The current sources can be biased by a 0.45 V signal generated from an active PMOS resistor M1 and passive resistor R1 in series. Since the source-to-drain voltage drop across M2 and M3 is relatively large at 0.6 V, the PMOS transistors can be guaranteed to operate in saturation.
The mixer performs the multiplication of two signals. If the variables A and B represent the amplitudes of two simple sinusoids with frequencies $f_{RF}$ and $f_{LO}$ respectively, the multiplication of these signals is given by the following trigonometric identity

$$A \cos(2\pi f_{RF} t) \ast B \cos(2\pi f_{LO} t) = \frac{AB}{2} \left[ \cos(2\pi (f_{RF} + f_{LO}) t) + \cos(2\pi (f_{RF} - f_{LO}) t) \right]$$  \hspace{1cm} (48)

As can be seen from Equation 48, the resulting output signal contains the sum of both frequencies and the difference of both frequencies mirrored continuously throughout each nyquist zone. For downconversion the difference of the two frequencies in the first nyquist zone must be isolated and the other frequencies filtered out by a second order passive
lowpass filter as shown in Figure 51.

![Mixer and second order passive lowpass filter](image)

**Fig. 51** Mixer and second order passive lowpass filter

The mixer’s output before and after filtering is shown in Figure 52.

![Mixer output before and after filtering](image)

**Fig. 52** Mixer output before and after filtering

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3.2 Mixer Isolation

Since the mixer accepts a digital square wave that transitions quickly from DC ground to the supply voltage potential, a sudden change in current drawn by the gate of each transistor occurs. This can affect the response of the input \( V_{RF} \) as shown in Figure 53.

![Mixer Isolation Diagram](image)

**Fig. 53** Mixer DC offset error introduced on the analog input signal

The voltage drops seen on \( V_{RF} \) correspond to the rising and falling edges of the mixer’s digital square wave input. Since the mixer accepts a differential signal, the effect of the DC noise is cancelled out when one signal is subtracted from another as seen in Figure 53. So
long as the architecture in the AGC is balanced to provide an equal load and equal timing to the positive and negative ends of each input to the mixer, the mixer’s output is less affected. Since all the component in the AGC are differential, noise from isolation due to the mixer has a reduced impact on the AGC. The isolation of the gilbert cell mixer is improved over other mixer designs since the input signals are fed to the gates of transistors instead of intermediate drain-to-source connections between transistors.
IV. Combined AGC and Mixer

In Figure 54, a combined AGC and mixer schematic is shown. The mixer accepts the output of the AGC’s forward path in parallel with the RMS power detector.
The output of the mixer and lowpass filter can be seen in Figures 55 and 56. In Figure 55, the output of the AGC is set to produce a 200 mV amplitude sinusoid, and in Figure 56, the output of the AGC is set to produce a 2 mV amplitude sinusoid. As can be seen in both sets of waveforms, the output of the mixer is filtered to remove higher frequencies produced in the process of downconversion. Some DC offset noise is visible in the output of the AGC; however, the differential signal is able to cancel out the effects of the added noise.

![Fig. 55 Mixer output before and after down conversion for an AGC output amplitude of 200 mV](image-url)
Fig. 56 Mixer output before and after down conversion for an AGC output amplitude of 2 mV
V. Conclusion and Future Work

5.1 Conclusion

Presented is a wideband, analog AGC with a competitive settling time of 2 µs over the entire 63 dB positive gain tuning range at 1.575 GHz frequency of operation. The AGC is designed to isolate itself and minimize the DC offset corruption caused by a direct connection to a mixer. The AGC has a noise factor of 19.1 dB, which can be suppressed by a high gain LNA in the previous stage, and takes advantage of measuring the peak amplitude of the high frequency signal on the output of the AGC before the mixer to minimize errors in the output amplitude of the steady state response of the AGC and improve settling time, and is capable of tolerating a phase shift error in the received differential input signals by 4 picoseconds, which is 2.26 degrees.

For comparison, Table 4 shows the CMOS process, tuning range, settling time, and operating frequency for other analog feedback AGC designs.

<table>
<thead>
<tr>
<th>Device</th>
<th>CMOS Technology</th>
<th>Tuning Range</th>
<th>Settling Time</th>
<th>Operating Frequency</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ximenes &amp; Swart [10]</td>
<td>0.18 µm</td>
<td>30 dB</td>
<td>5 µs</td>
<td>2.4 GHz (1 MHz)*</td>
<td>30.0 mW</td>
</tr>
<tr>
<td>Wang and Liu [11]</td>
<td>0.18 µm</td>
<td>28.5 dB</td>
<td>1.6 µs</td>
<td>-----</td>
<td>43.2 mW</td>
</tr>
<tr>
<td>Qianqian et al. [12]</td>
<td>0.18 µm</td>
<td>55 dB</td>
<td>----</td>
<td>30 MHz</td>
<td>5 mW</td>
</tr>
<tr>
<td>This Design</td>
<td>0.13 µm</td>
<td>63 dB</td>
<td>2.0 µs</td>
<td>1.575 GHz</td>
<td>4.41 mW</td>
</tr>
</tbody>
</table>

*Frequency of peak detection after mixer downconversion
5.2 Future Work

For future study, the LC filter in Figure 26 can be configured to adjust its center frequency. By replacing the mimcaps inside the LC filter with varactors that can change capacitance, the AGC would be capable of switching channels as necessary in order to process data from multiple users.

Additional components in the receiver chain can be designed and integrated with the proposed AGC and mixer. Other components in the receiver chain have an impact on the performance of the AGC. The LNA in the previous stage of the receiver chain is a single ended output device. A single ended to double ended conversion must take place before the signal is fed into the AGC. The tolerance of such a conversion must fall within the specifications of the AGC; otherwise, the output of the mixer and AGC becomes corrupted. The gain of the LNA in the previous stage of the receiver chain must also be sufficiently large enough to mitigate the 19.1 dB noise figure of the AGC as measured without an amplifier driving its input.
V. References


